PHASTFlex

Photonic **H**ybrid **AS**sembly
Through **FLEX**ible waveguides

Newsletter #3 | February 2018

Contents of this newsletter:

About the PHASTFlex idea

Welcome to the third, and last, newsletter of the PHASTFlex consortium. In this issue we present some recent PHASTFlex advances, but first a reminder about the overall PIC packaging concept.

Photonic Integrated Circuits (PICs) are chips which work with light signals instead of electronic signals. They are in increasing demand, for example to help process ever-growing internet traffic flows. Photonic chips are already vital components in long-haul and metro-area telecommunication systems. What is less well known is that they also have great potential in many other application areas, for example in data centres, high performance computing, remote sensing, structural health monitoring, medical applications and metrology.

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ABOUT PHASTFLEX

PHASTFlex (Photonic Hybrid ASsembly Through Flexible Waveguides) is funded through EU FP7 (Project Number: FP7-ICT 619267).
PHASTFlex proposes the development of a fully automated, high precision, cost-effective assembly technology for next generations of hybrid photonic packages

Project End Date:
August 31st 2014. The final project duration: 44 months, and the total cost 3.9M€.

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Website: www.phastflex.eu

Development of the Chevron Actuator (TU Delft and LioniX)

The fine-alignment of the waveguides uses MEMS functionality, which is integrated into the TriPleX chip. For this purpose, the TriPleX chip needs flexible waveguide structures, actuators to bring the waveguide structures in the optimal position, and, finally, locking functions to maintain the optimal position after alignment. For the out-of-plane actuation, thermal bimorph actuators are used as described in earlier newsletters. The TriPleX material is essentially a stack of SiO_2 cladding material with Si_3N_4 waveguide cores. The thickness of this material stack is about 16µm. A typical bimorph actuator beam consists of the SiO_2 (with or without the nitride cores) with a layer of deposited poly-Si (typically 2-5µm thickness). Upon heating, for which purpose conductors and heaters are added, the beam will have an out-of-plane displacement due to the difference in thermal expansion of the two materials involved.

PHASTFlex has now developed a novel chevron actuator in combination with a lever mechanism for in-plane motion.

▶ read more...

About the PHASTFlex idea (continued from page 1)

A long standing challenge in the deployment of optical circuits based on Indium Phosphide has been the small size of the optical waveguides compared to the standard transmission medium – glass optical fibre. High-precision, sub-micron alignments are needed, which has made make packaging, achieving the coupling of the light from the PIC to the optical fibre and hence the outside world, expensive. PHASTFlex has been engaged in developments towards a fully automated, high precision (±0.1µm alignment), cost-effective assembly technology for next generation hybrid photonic packages. A two-step approach is investigated in PHASTFlex in which a machine based passive assembly step makes an initial placement of two chips, one containing the active functions, and a second interposer chip containing passive optical circuits, on a common carrier as shown in Figure 1. In a second step, PHASTFlex has explored a novel concept in which the waveguides in the interposer are part of a moveable MEMS structure, released during fabrication.

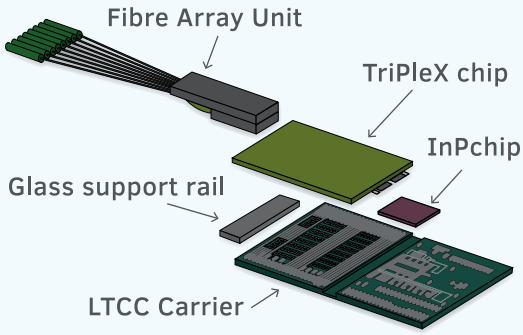

Figure 1 Exploded drawing of the assembly showing the piece parts required (from left to right): Fibre array unit, TriPleX chip with MEMS (back side view), glass rail, InP chip (back side view), LTCC (Low temperature co-fired ceramic) carrier (top view).

The idea is that the integrated MEMS actuators and fixing functions place and fix the flexible waveguides in the optimal position (peak coupled power) in a two dimensional transverse plane.

Development of the Chevron Actuator (continued from page 1)

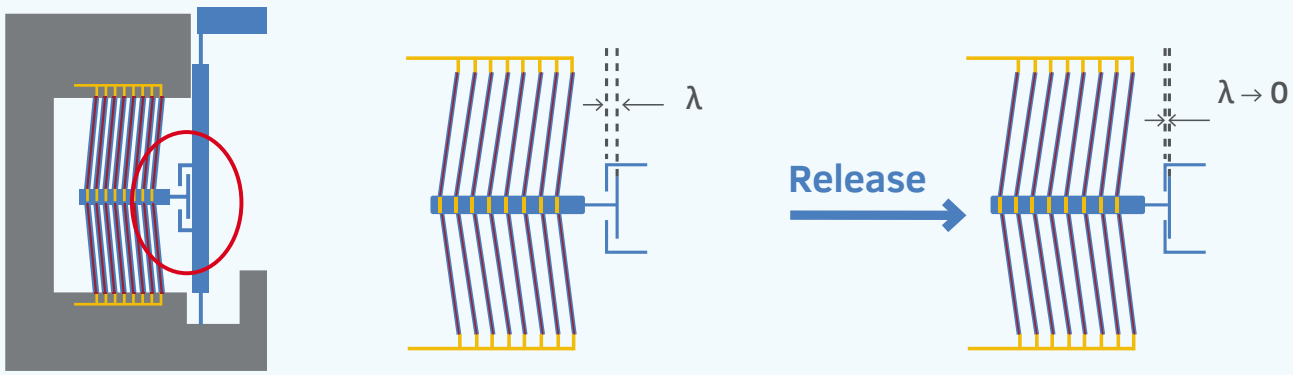

Figure 2 Design innovation: decoupled in-plane chevron actuator decoupled from lever mechanism in the mask design, gap λ closes due to post-release deformation of the chevron actuator.

Design innovation: decoupled chevron actuator

For in-plane actuation a lever mechanism is employed to amplify the short stroke available from the chevron actuators as illustrated in Figure 2. However, the significant post-release deformation of the chevron, in the order of several micrometers, in combination with its relatively high stiffness led to fracturing. Typical positions where failure occurred were the hinge of the lever or the chevron shuttle. To overcome this issue, an innovative design of the interface between

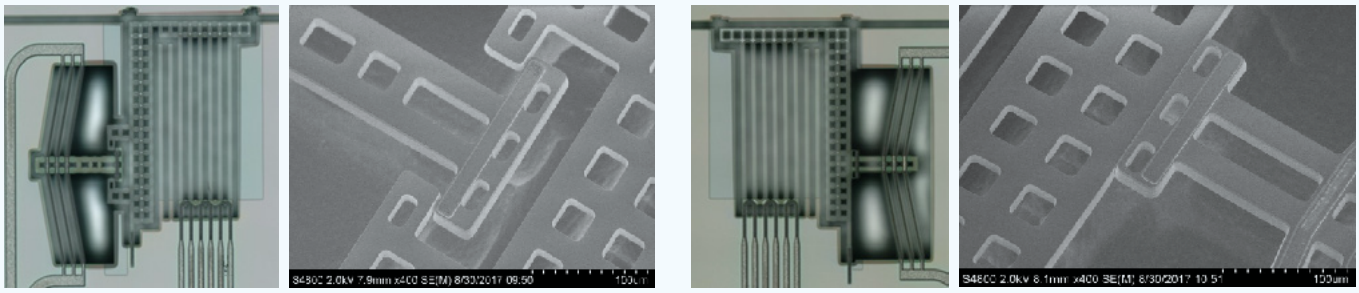

Figure 3 Fabrication results. Left: design with pulling in-plane chevron. Right: design with pushing in-plane chevron.

the in-plane actuator and the lever was introduced, see Figure 3 detail. The chevron shuttle and the lever were decoupled in the mask design. The post-release expansion of the chevron actuator is now purposefully used to close the gap during fabrication and make shuttle and lever engage.

In this schematic representation the in-plane chevron actuator was designed to pull the cross-bar and waveguide structure. Alternatively, the in-plane chevron can also be designed to push the cross-bar and waveguide system. One advantage is that this simplifies the structure at the chevron interface-lever mechanism interface. Figure 3 shows microscopy pictures of the chips fabricated at TU Delft showing both pulling and pushing in-plane chevron actuators, as well as detailed views of the engaged actuator-lever interface.

Actuator Performance | TU Delft

Figure 4 summarizes the result of an in-plane motion measurement. The graph shows that with 130mW power, about 1.8µm of cross bar motion is generated. The measured motion amplification the lever offered is ~3.3, which corresponds well with the designed lever ratio of 3.4. It is understandable that the structures show cross-sensitivities, since all the actuators are mechanically coupled in the design. Figure 5 (see next page) shows measurement results; the figure to the left shows operation of the left-side bimorph actuator, whilst the figure to the right shows the operation of the right-side actuator. In the graphs two situations are captured: one where the chevron actuator is off and one where the chevron actuator is at a certain power level. As can be expected, at the same power level, the left side actuator leads to more deformation of the corresponding beams than the right-side actuator; the latter one is closely placed to the lever and chevron actuator, which adds to the out-of-plane stiffness. When the chevron actuator is switched on, it exhibits an expected bimorph effect as well, and it lifts the entire

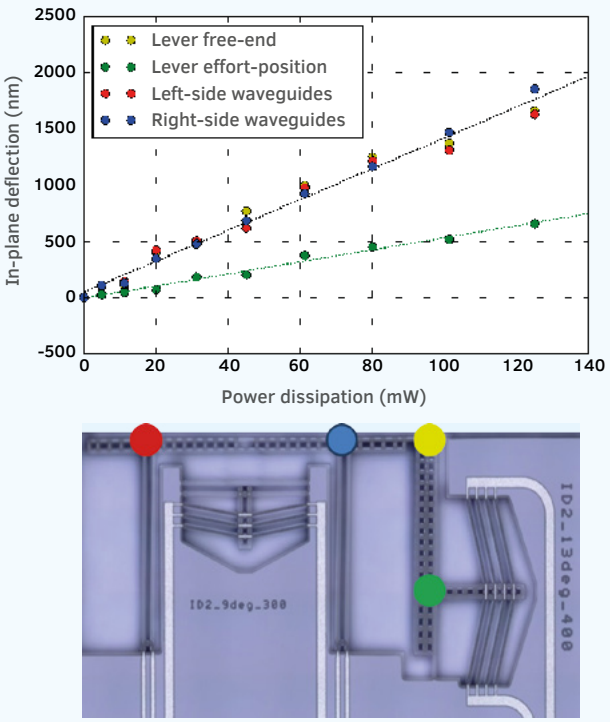

Figure 4 In-plane motion measurement: graph (top) showing motion of chevron shuttle and cross-bar (lower picture).

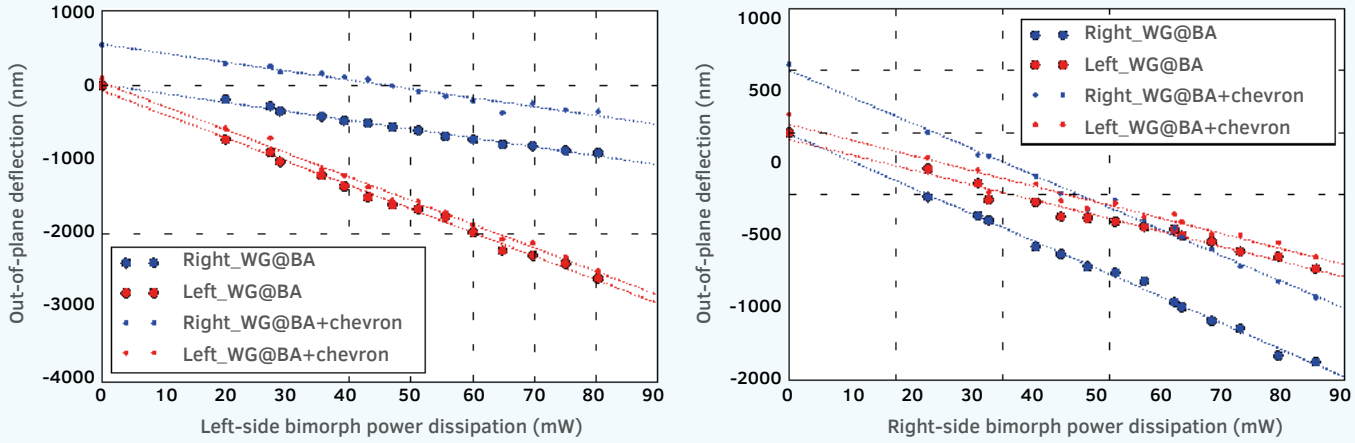

Figure 5 3D motion measurement and Illustration of cross sensitivities.

structure up. Subsequent operation of the bimorph actuators shows that the motion range that can be obtained is still available. It is clear; however, that the parasitic motion of the chevron actuator reduces the available space in which end-facets can be positioned.

Automated assembly | Ficontec and Aifotec

An automated assembly machine was designed early in the project. It is capable of oven bonding of the InP and the TriPleX chips as well as allowing active alignment of the MEMS structures of the TriPleX chip through probe cards and contact pads designed into the (Low temperature co-fired ceramic) LTCC carrier. The main motion system of the machine consists of a 4-axis manipulator, with nozzles for chip handling and sensor systems for process control. A separate high accuracy vision system allows an in-situ monitoring of the chip placement and is used to support the alignment. For performing a vision analysis, which can be done independently of the chip placement, the vision system is mounted on a separate 3-axis motion system. The machine is built to allow oven bonding of the InP and the TriPleX chips to the LTCC carrier, as well as allowing active alignment of the MEMS structures of the TriPleX chip through probe cards and contact pads designed into the LTCC. Targeting passive alignments of ±0.5µm requires this machine to be at or better than the current state-of-the-art.

A two-step approach is investigated by PHASTFlex as described earlier in this newsletter.

First, a machine based passive assembly stage makes the initial placements of a chip containing the active functions, and an interposer chip on a common carrier. The die attach is via a double solder reflow flip-chip assembly.

Secondly, waveguides in the matching TriPleX PIC are formed as part of a moveable MEMS structure, released during fabrication. The idea is that actuators and fixing functions, integrated in the same PIC, place and fix the flexible waveguides in the optimal position in the transverse plane. Given the expected travel range of the MEMS structures is a few microns, a thin film metallisation process has been chosen for the AuSn solder deposition on the LTCC because of its good bond height control.

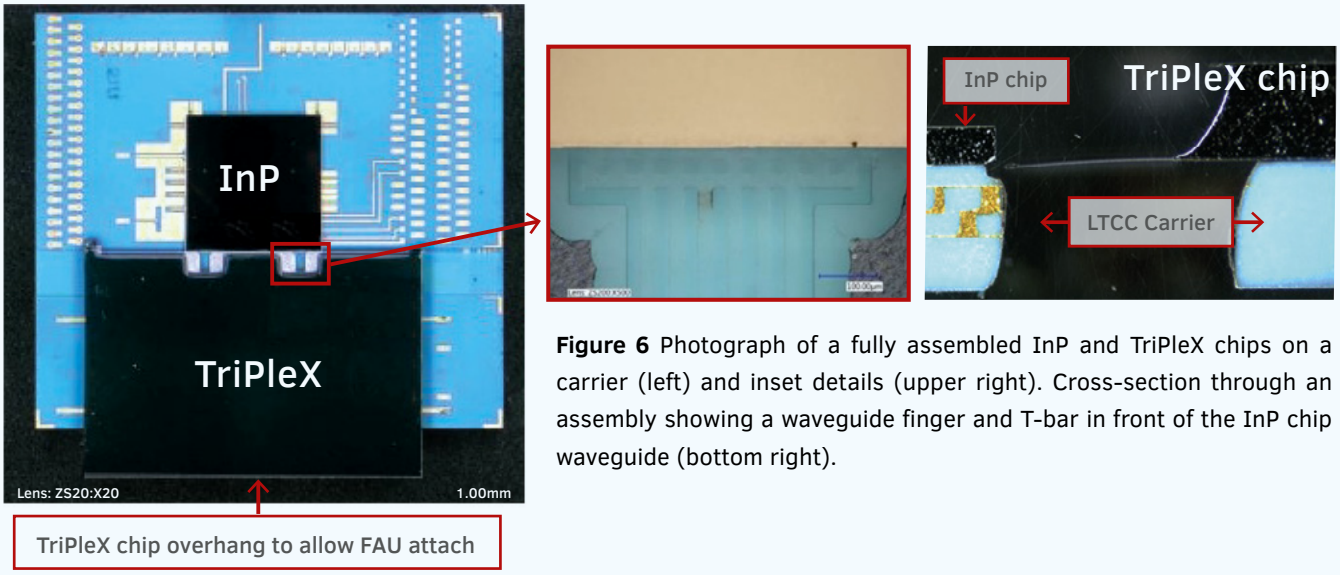

Figure 6 Photograph of a fully assembled InP and TriPleX chips on a carrier (left) and inset details (upper right). Cross-section through an assembly showing a waveguide finger and T-bar in front of the InP chip waveguide (bottom right).

An example of two chips passively aligned on the carrier in a real assembly is shown in Figure 6 (left). The image in Figure 6 (lower right) was obtained via mechanical polishing of an assembly embedded in polymer. It shows a rather visually striking image of the MEMS waveguide finger integrated in the TriPleX chip on the right, approaching the inverted InP chip on the left, and gives some idea of the scales on which PHASTFlex works. The gold vias and tracks in the multi-layer LTCC carrier are also clearly visible underneath the InP chip. The natural curvature of the waveguide fingers is used to partially accommodate for the difference in chip heights. It has been confirmed to be ~8µm in realised assemblies and the vertical position is adjustable via the MEMS over a few microns.

Automated Assembly- two chip placement accuracy | Aifotec

For PHASTFlex a two-step solder reflow was used in which the InP chip was soldered first. The alternative, to bond both chips in a single reflow, introduces great complexity into the multi-axis alignment of two chips simultaneously in the machine. In a two step solder reflow, it is necessary to protect the solder pads used in the second reflow from oxidation while soldering the InP chip, and also ensure a uniform distribution of heat across the surface. A gas inlet for forming gas or formic acid was implemented which guarantees a homogenous and laminar gas flow over the solder pads without introducing any unwanted cooling effects on the sample. The PICs developed in PHASTFlex are large in area (5-10mm or more on a side) and flip chip bonded onto a large area carrier, hence a special oven/hot plate eutectic assembly heating process was developed to realize the flip chip hybrid assembly.

Chip Placement Accuracy:

The objective of the assembly process was to demonstrate that an InP and a TriPleX chip can be placed on the carrier with the suitable tolerances on all axes at the same time. In this short article we look at separation along the optical axis.

First the InP chip is mounted on the LTCC. In a second reflow cycle the TriPleX chip is placed in relation to the InP using the machine vision systems to locate the chips. Front to back registration using chip edges and corners is required to accurately align the waveguides on both chips to each other.

An intermediate step is to identify any fixed machine offsets required to compensate and achieve a final required placement position. Thermal mismatches between the chips and pick up tools (PUTs), carrier and oven need to be characterised but cannot be completely avoided. These parts are all in contact for part of the eutectic heating process so some movement of the piece parts during the heating cycle is to be expected, but as long as these effects are reproducible they can be calibrated out. A PUT based on ceramic "Macor" which is better matched thermally to the chips than standard polymer based tools, was designed for the second step TriPleX assembly.

Waveguide-axis chip to chip separation:
The passive alignment and assembly approach which is used for placing the InP and TriPleX chip onto the LTCC is based on the evaluation of camera images.
Placement accuracy is therefore largely dependent on the accuracy of image recognition in the machine. A calibration exercise was set up between partners in order to check the distance measurements recorded. Measurements from the machine cameras were compared with low voltage SEM measurements and external microscope images at TU Eindhoven and Aifotec.

The SEM measurement result of 1-1.6µm gives confidence that the targeted gap for these assemblies can be in the desired range, but the machine measurement of the same assembly was 2.5-3.0µm. More calibration work is needed to bring the machine based systems and SEM calibration into line.

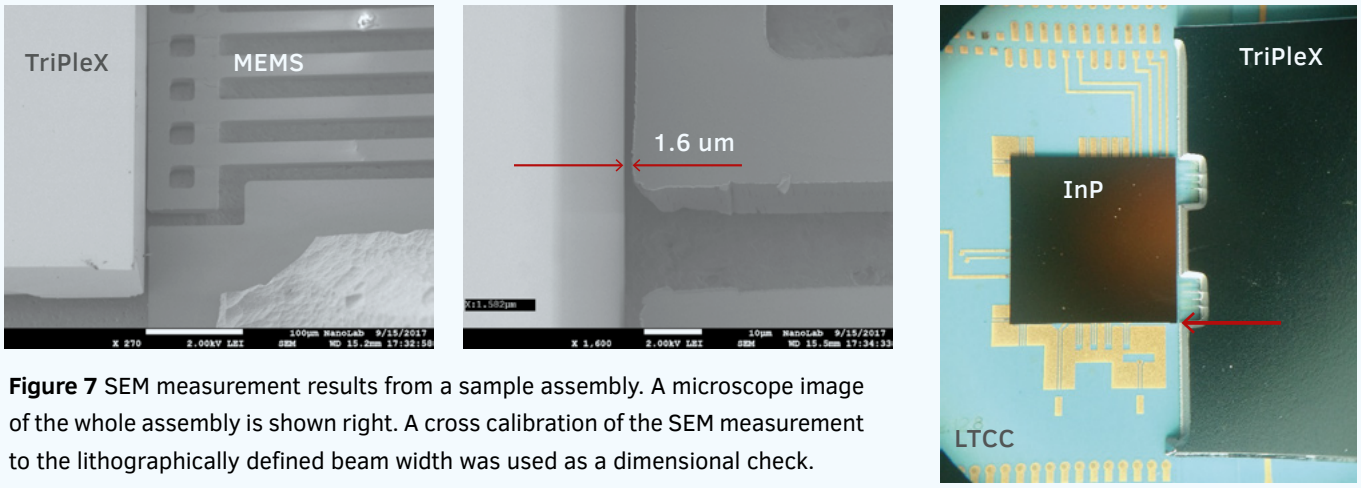

Figure 7 SEM measurement results from a sample assembly. A microscope image of the whole assembly is shown right. A cross calibration of the SEM measurement to the lithographically defined beam width was used as a dimensional check.

Finger movement trials using Lab Bench testing | TU Eindhoven, LioniX

The project has studied the optical coupling between the InP PICs fabricated by Oclaro and TriPleX MEMS fabricated by LioniX in a lab setup, in order to experimentally verify the coupling efficiency and the dependence on the electrically driven actuation of the MEMS.

To measure the displacement of the structure under electrical bias, the light of two adjacent waveguides was captured in an IR camera. The separation between these waveguides is very accurately known from the mask design of the MEMS chip and allows for absolute displacement calibration. By applying a bias voltage to the MEMS actuators, the near field image will move across the camera sensor and the movement is determined. The resolution of the system, in this configuration, was determined to be better than 200nm.

With this method we determined the out-of-plane displacement. Several chips have been tested from wafers with different poly-silicon actuator thickness. For the wafers with a poly-silicon thickness of 5µm the maximum power applied to each of the two actuators was 100mW. The waveguides show a movement range of ~8µm which is sufficient for proper compensation of the initial placement inaccuracy.

Position drift under actuation:

We observed that the waveguides first move to their expected position but then drift from that position. This effect is understood to be due to a thermal relaxation of the whole chip to an overall thermal equilibrium. The relaxation time is about 1500s for the long actuators and about 1000s for the short ones. From the figures we extract that, directly after positioning the MEMS, the drift is approximately 0.6nm/s. That means that for a maximum allowed drift of, say, 20nm, we would need to fix the structures within 30s. That is well within the expected time needed.

Coupling between actuated waveguides and InP:

Next step is to measure the actual optical coupling between the Oclaro test sample and the TriPleX MEMS waveguides, while operating the actuators. To this end, the Oclaro test sample was mounted in a dedicated sub-mount.

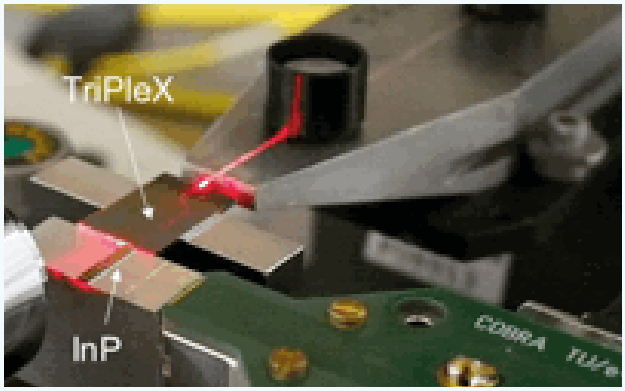

Figure 8 Photograph of the TriPleX with MEMS waveguides aligned to the Oclaro test chip.

Figure 8 shows the lab-bench setup with the TriPleX sample on a two axis stage, and light coupled into it from an optical fibre on a 3-axis stage. The Oclaro test chip is on a 6-axis stage aligned to the TriPleX waveguides. The MEMS waveguides are on a 50µm pitch. Using the data from the displacement mappings we can calculate the displacement of the beam versus MEMS actuation power. This has been used to calculate the modal overlap versus displacement, which is shown for the two outer waveguides (250µm apart) in Figure 9. The match between theory, for a Gaussian beam with 3µm beam diameter, and experiment, is seen to be very good.

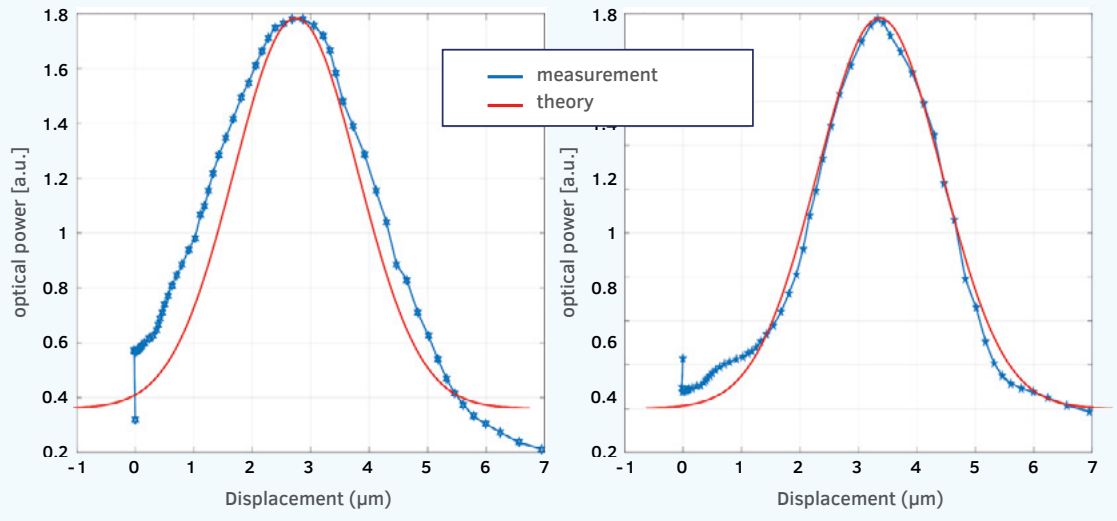

Figure 9 Optical power inferred from detected photocurrent in the Oclaro InP chip as a function of the MEMS displacement.

Co-design of applications chips for a common carrier | IMST, Oclaro, TELNET, LioniX

Applications

Two application specific PICs (ASPICs) have been designed and fabricated for demonstration in PHASTFlex, one an active applications chip designed by TELNET and fabricated by Oclaro using their generic platform. The second chip was a matching TriPleX PIC with MEMS functionality, which was fabricated by LioniX. TELNET targets the development of a multi-wavelength 40G WDM photonic transceiver for the next generation of Passive Optical Networks (PONs). The schematic of the transceiver design for PHASTFlex is shown in Figure 10.

TELNET ASPIC:

The InP TELNET ASPIC has been designed using Oclaro's MPW Process Design Kit (PDK) on their generic platform. A photograph of the fabricated chip is shown in Figure 11. The ASPIC consists of a 4-channel multi-wavelength transceiver. The transmitters are placed in the right side of the chip and consist of four DBR laser emitting at four different wavelengths and four Mach-Zehnder modulators for 10GHz modulation. The receivers consist of four pairs of amplifier and detector and are placed in the left side of the chip. The receiver will operate with a bandwidth of 10GHz. For the PHASTFlex hybrid integration approach, light sources and photodetectors were added for the alignment procedure. These were placed on the sides of the signal waveguides and allow the automatic alignment. Also, in-line optical power monitors, that tap only a small fraction of the incoming or outgoing optical power, were added in all optical I/Os for redundancy purposes. On-wafer test and chip testing were used to validate the process run.

The mux and demux passive components were designed in LioniX´s TriPleX technology; they are discussed in more detail in the next article.

LTCC carrier:

The LTCC carrier for the TELNET ASPIC consists of a seven layer stack-up of DuPont 951 with a final thickness of 980µm (140µm each layer). The final dimensions of this LTCC carrier are 18.5mm x 20.8mm. Figure 12 shows the top view of the carrier. It shows the InP chip (red) in front of the TriPleX chip (dark yellow). The carrier has two set of pads on the upper left side where the probe cards used during the alignment process may be contacted.

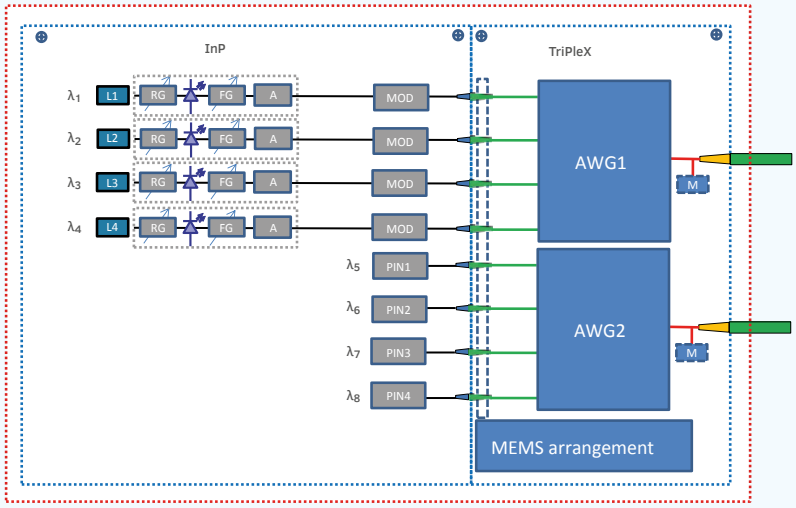

Figure 10 Schematic of the NG-PON ASPIC proposed by TELNET.

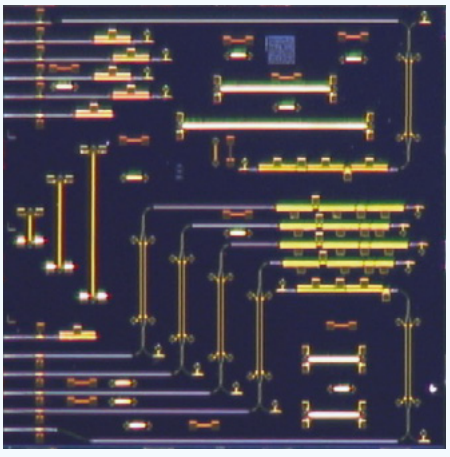

Figure 11 Photograph of the TELNET NG-PON fabricated by Oclaro. The total circuit size is 6x6mm^2

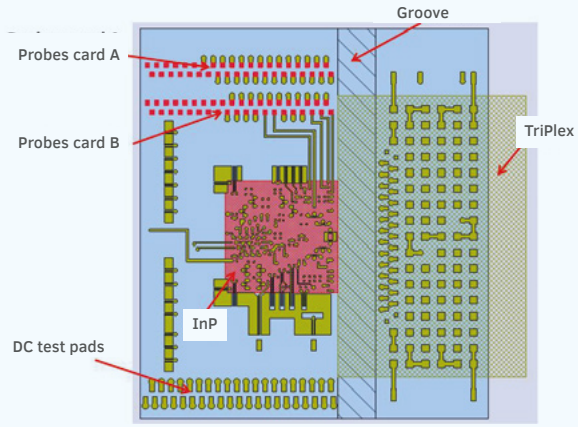

Figure 12 Top view of the LTCC carrier layout.

These two set of pads (A and B) are related to the two independent alignment mechanisms in the TriPleX chip. A third set of DC pads has been included on the lower side of the carrier. These pads connect to the different InP chip pads that need to be monitored during tests or used during the operative mode of the chip. Finally, a 60µm wide groove has been diced on the carrier, sited underneath the edge of the TriPleX chip. This groove provides the required free space for movement of the chip's mechanical structures.

Arrayed Waveguide Gratings in TriPleX | (TELNET, LioniX)

The TriPleX ASPIC that connects to the TELNET NG-PON application chip uses Arrayed Waveguide Grating (AWG) (de)multiplexers. It also provides passive waveguides and mode expansion from the coupling interface to the fibre array unit (FAU). For the AWG input and output channels are connected to TriPleX facets at the InP as well as the fibre interfaces. The optical layout of the TriPleX chip comprises two independent AWGs for implementing the mux and demux passive functionality of the transceiver. This 4-channel cyclic device has a channel spacing of 100GHz and a free spectral range (FSR) of four times the channel spacing, or 400GHz. The resulting AWG layout is shown in Figure 13.

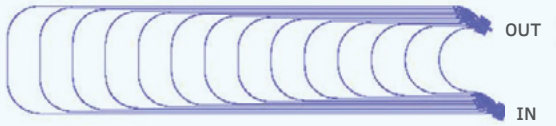

Figure 13 AWG mask layout. The AWG design has been carried out with the support of an external design service provider with access to device models calibrated on the TriPleX platform: brightphotonics.eu

The simulated and measured responses of the AWG are shown in Figure 14. Both the channel spacing and the FSR perfectly match the design values of 100GHz and 400GHz, respectively. The excess loss is around 4dB, which is a reasonable value, certainly when considering that these are among the first AWGs to be fabricated in this waveguide materials structure. The crosstalk levels are sufficient for this first demonstration, and can be improved in future design cycles.

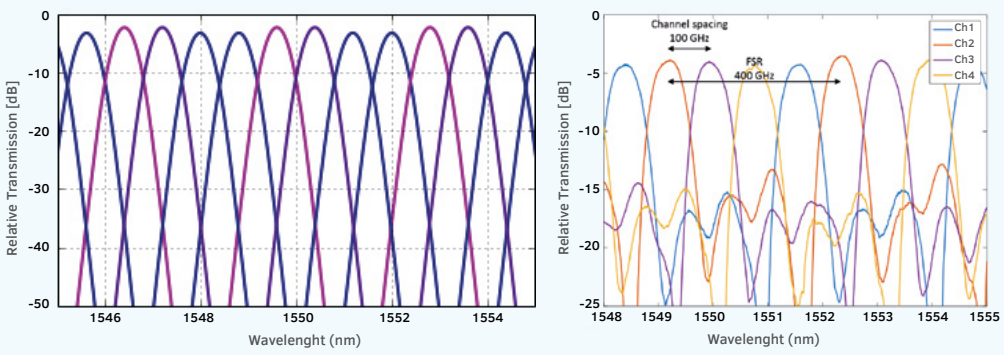

Figure 14 AWG response simulated (left) and measured (right).

Summary

The PHASTFlex project has made a lot of progress, and many aspects of the approach have been demonstrated successfully, as presented in this newsletter. Convincing demonstration of the full process flow; comprising accurate and reproducible passive placement of the TriPleX chip in relation to a pre-assembled InP chip, followed by electrically driven waveguide positioning and locking, will require further advancements in several areas; however. The co-design and fabrication of the matching piece parts using a foundry approach has been one of the successes of the project. Waveguide beam movement using on-chip actuators in three axes has been demonstrated, as well as electrically driven waveguide movement of MEMS chip integrated with an LTCC carrier. A preliminary demonstration of locking has also been achieved although not discussed here.

The design and fabrication of MEMS structures in the TriPleX photonic platform based on the SiO_2/Si_3N_4 material combination used for the interposer chip is quite novel, as most MEMS designs are realised in Si. Good progress has been made in design and realisation, and fabrication yield has significantly improved, though for industrialisation major steps have yet to be made. The limited yield level is largely a consequence of the rather large mechanical structures adopted for PHASTFlex, and future work will need to move to more compact designs.

Passive placement of the chips using a dedicated assembly machine has proved challenging. Careful optimisation of the two step reflow cycle is required to achieve sound uniform bonds. The InP chip in particular has a large number of electrical connections; there are different pad sizes; RF lines for driving the optical circuit and many DC connections. The chips are significantly larger than expected at the outset of the project, particularly the TriPleX chips which are ~10mmx15mm. Nonetheless, good bonds have been achieved with good electrical connectivity, shear forces can be high and preliminary environmental testing is encouraging, as are the results of RF testing. Chip separations along the optical axis in the range 1-5µms have been demonstrated using SEM to support microscope and machine based measurements. Lab bench trials have demonstrated the principle of electrically driven coupling optimisation.

Packaging challenges can only become more acute as PIC complexity increases, package footprints shrink and the number of channels grows; the consortium members retain their confidence that, in the longer term, an approach based around waveguide fingers to optimise waveguide coupling can be successful. Significant further investment will be required to bring PHASTFlex to full fruition, but the advantages to be gained are also significant.

MORE INFORMATION ABOUT THE PHASTFLEX PROJECT

PHASTFlex has sought to publicise is work through a variety of workshops, symposia and meetings, in Europe and in the US. Through our coordinator, Xaveer Leijtens of TUE, the PHASTFlex packaging concept was presented in a paper entitled *MEMS-assisted fiber-chip coupling*[1] in 2017.

[1] X.J.M. Leijtens, R. Santos, M. Tichem, K. Wörhoff and K.A. Williams
(Partners TU Eindhoven, Delft University of Technology, and LioniX BV) Proc ECIO 2017 Eindhoven

Further sources of information:

[2] *TriPleX: a versatile dielectric photonic platform Kerstin Wörhoff*, et al. (2015) Adv. Opt. Technol. 2015; 4(2): 189–207
[3] *Photonic Hybrid Assembly Through Flexible waveguides* (2016), K. Wörhoff et al. SPIE paper Vol 9891, doi: 10.1117/12.2227814

GENERAL PROJECT FACTS AND FIGURES

PHASTFlex: Photonic **H**ybrid **AS**sembly **T**hrough **Flex**ible Waveguides is funded through EU FP7 (Project Number: 619267)

The website address for the project is: **phastflex.eu**

Partners and their principal roles in the PHASTFlex consortium are:

TU Eindhoven, NL (Coordinator)	Project management; optical bench trials of MEMS functional chips, structural characterization of assemblies and carriers, dissemination.
TU Delft, NL:	MEMS design and MEMS processing, dissemination.
Oclaro Technology, Ltd., UK.	Applications, setting applications requirements, InP chip fabrication, environmental testing.
LioniX International BV, NL	TriPleX PIC design and fabrications. Implementation of MEMS designs in TriPleX, technical lead.
Willow Photonic Ltd, UK	Administration, technical management and dissemination
ficonTEC Service GmbH, DE	Design and build of the assembly machine, process development support.
IMST GmbH, DE	LTCC carrier design and fabrication, RF testing.
TELNET Redes Intelligentes SA., ES	Applications requirements, next generation PON design and development.
Aifotec AG, DE	Flip chip, thin film, assembly process development.

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