PHASTFlex

Photonic Hybrid Assembly Through Flexible Waveguides

Photonic Hybrid ASsembly Through FLEXible waveguides

PROJECT FINAL REPORT

Project acronym: PHASTFLEX

Project title: Photonic Hybrid ASsembly Through FLEXible waveguides

Funding Scheme: FP7

Period covered: from 1/7/15 to 31/8/2017

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Deliverable Report (WP5, D7.5)

Final Public Summary

Compiled by David Robbins

Submission Date: 22nd December 2017
Lead Partner: WIL
Other Contributing Partners: TUE, TUD, LX, Aifotec, Ficontec, TELNET, IMST and OCLR.

Acknowledgement: *The research leading to these results has received funding from the European Community's Seventh Framework Programme FP7/2007-2013 under grant agreement n°619267, PHASTFlex.*

European Commission

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Glossary of Terms	
ASPIC	Application Specific Photonic Integrated Circuit
AWG	Arrayed Waveguide Grating
CPW	Coplanar waveguide
DBR	Distributed Bragg Reflector
DP-QPSK	Dual–Polarization Quadrature Phase–Shift Keying
FAU	Fibre Array Unit
FSR	Free spectral range
InP	Indium Phosphide
I&Q	In-phase and quadrature
JePPIX	Joint European Platform for InP-based Photonic Integrated Components and Circuits
LTCC	Low Temperature Co-fired Ceramic
MEMS	MicroElectroMechanical System
MPW Run	Multi-Project Wafer Run
(NG-)PON	(Next generation) Passive optical network
PDKs	Photonic Design Kits
PIC	Photonic Integrated Circuit
PIN	P – I – N – junction photodiode
PUT	Pick Up Tool
PIC	Photonic Integrated Circuit
SOA	Semiconductor Optical Amplifier
WDM	Wavelength division multiplexing

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1. Executive Summary

PHASTFlex has been engaged in developments towards a fully automated, high precision, cost-effective assembly technology for next generation hybrid photonic packages. The most demanding assembly task for multi-port PICs today is the high-precision (±0.1µm) alignment and fixing required for the optical I/O. A two step approach is proposed in PHASTFlex in which a machine based passive assembly step makes initial placement of two chips, one containing the active functions, and a second interposer chip, on a common carrier. In a second step, PHASTFlex has explored a novel concept in which the waveguides in the interposer are part of a moveable MEMS structure, released during fabrication. The idea is that the integrated MEMS actuators and fixing functions place and fix the flexible waveguides in the optimal position (peak coupled power) in the transverse plane.

The co-design and fabrication of the matching piece parts using a foundry approach has been one of the successes of the project. Waveguide beam movement using on-chip actuators in three directions was demonstrated, as well as electrically driven waveguide movement of MEMS chip integrated with an LTCC carrier. A demonstration of locking has also been achieved.

The design and fabrication of MEMS structures in the TriPleX photonic platform based on the SiO_2/Si_3N_4 material combination used for the interposer chip is quite new and was from the outset viewed as one of the higher risk areas of the project. Despite good progress in design and realisation, yield of the MEMS structures remains low; however, for reasons of both process and design, it is largely a consequence of the rather large structures needed to support the required functionality.

Passive placement of the chips using a dedicated assembly machine has not turned out to be the lower risk activity it was believed to be. The chips are significantly larger than expected, particularly the TriPleX chip, have large numbers of electrical connections with different pad sizes, and so are more difficult to place accurately. Good bonds have been achieved for single chips with good electrical connectivity, shear forces can be high and environmental testing is very encouraging, as are the results of RF testing. Chip separations in the range 1-5µms have been demonstrated using SEM to support microscope measurements.

PHASTFlex project has made a lot of progress, and many aspects of the approach have been demonstrated in isolation, nonetheless convincing co-demonstrations of the two basic principles of accurate and reproducible passive placement of the TriPleX chip in relation to a pre-assembled InP chip, followed by electrically driven positioning and locking have eluded us. Against this backdrop progress with applications led work in the project has been curtailed. Lab bench trials have demonstrated the principle of electrically driven coupling optimisation, and TELNET has benefitted from the design and fabrication of integrated circuits for their applications, but the final stage of testing a subassembly in the dedicated test station at TELNET has not been possible due to a lack of suitable complete assemblies. Nonetheless, packaging challenges can only become more acute as PIC complexity increases, package footprints shrink and the number of channels grows; the consortium members retain their confidence that, in the longer term, an approach based around waveguide

fingers to optimise waveguide coupling can be successful. It is clear that further investment and innovation will be required to bring the PHASTFlex assembly concept to full fruition.

2. The PHASTFlex Assembly Concept

Photonic Integrated Circuit (PIC) fabrication can now be done using generic foundry based processes (*See for example the JePPIX website www.jeppix.eu)*, bringing the cost of an application specific PIC (ASPIC), into the range ~10-100€, greatly increasing technology access. However, packaging is an order of magnitude more expensive, and this is still a major bottleneck to further market penetration. A new approach is required.

PHASTFlex has been engaged in developments towards a fully automated, high precision, cost-effective assembly technology for next generation hybrid photonic packages. The most demanding assembly task for multi-port PICs is the high-precision (±0.1µm) alignment and fixing required for optical I/O in photonic chips, even with waveguide spot size conversion. A two step approach is proposed in which a machine based passive assembly stage makes initial placement of a chip containing the active functions, and an interposer chip on a common carrier. For PHASTFlex the chosen technologies are InP (active) and TriPleX (interposer) optical chips on a~~n~~ common LTCC carrier. Both chips support significant functionality and can be complex in design. In addition to simple mode matching the TriPleX chip is capable of adding functionality in a way which can be optimised between the chips for any given application. The chosen assembly process is a double reflow flip-chip assembly on a LTCC carrier. High end applications desirably require initial placement accuracies for the two PICs of 1.5 ± 0.5µm chip separation in the direction of the optical waveguides and required lateral alignment accuracy of +/-2-3µm. These are demanding specifications, at the limits of what can be achieved today, and a dedicated assembly machine has been designed and built for this purpose. In a second step, PHASTFlex has explored an innovative concept, in which the waveguides in the matching TriPleX™ [1] PIC are part of a moveable MEMS structure, released during fabrication. The idea is that actuators and fixing functions, integrated in the same PIC, as illustrated in Figure 1, place and fix the flexible waveguides in the optimal position (peak coupled power) in the transverse plane. Given the expected travel range of the MEMS structures, a few microns, thin film solder metallisation is chosen because of its good bond height control. Connection to the signal fibres is then relatively easily arranged through the attachment of a fibre array unit to the interposer chip.

This approach offers not only high alignment accuracy for the optical circuit but also some other possible advantages, for example local hermeticity (as opposed to expensive overall hermetic packaging), and the possibility of activating and locking the electrically driven MEMS fingers only after external packaging enclosures are in place.

[1] A proprietary silicon based waveguide technology of LioniX International. http://www.lionix-international.com/

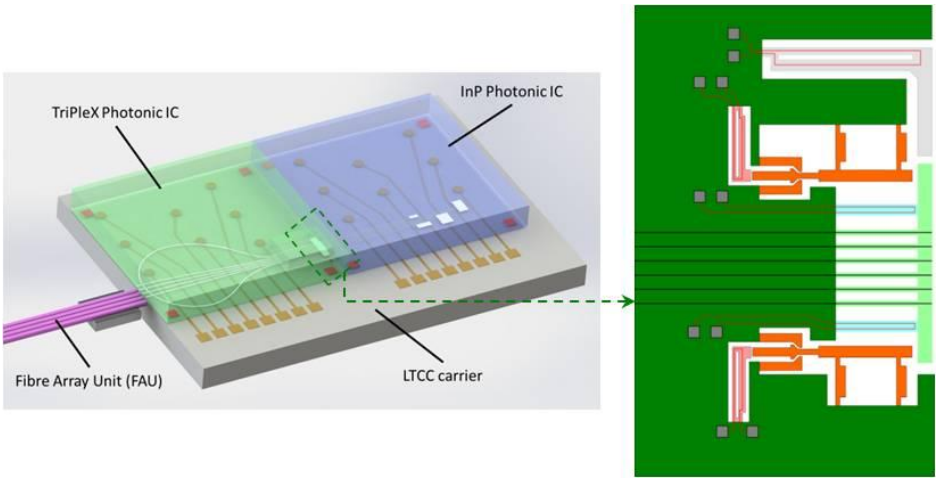

Figure 1: 3D view of the overall assembly concept proposal with the InP active chip and the TriPleX interposer chip flip-chip mounted on a carrier (left). To the right the fine detail of the proposed MEMS-based fine alignment functions on TriPleX PIC are illustrated in more detail (right).

The PHASTFlex project has aimed for proof of concept for a complete assembly process including the required tooling to implement this approach: assembly using two step eutectic solder reflow, automated chip handling, and on-chip micro-fabricated fine-alignment and fixing functions, all designed for real end user applications. This ambitious solution is made possible by recent advances in generic integration platforms and assembly technology, but requires nonetheless assembly process development and complex co-design and realisation to achieve.

3. PHASTFlex Objectives

The central PHASTFlex objective was to develop a complete process suitable for high volume PIC assembly: A two-phase process was proposed for assembling an InP PIC and TriPleX PIC on a common carrier. The first phase, the pre-alignment phase, is a passive alignment on the basis of industrial solutions for substrate and chip handling, including vision systems. The bonding and electrical interconnection of the chips was addresses using solder reflow. The second phase, fine alignment, will be done with the on-chip assembly functions provided by the MEMS structures. PHASTFlex has aimed:

1. **To develop on-chip MEMS-based fine alignment and fixing functionality** for TriPleX to support the fine-assembly. This includes flexible waveguides, actuators for moving the waveguides and structures for fixing the waveguides in the final position. These functions to be integrated with the TriPleX PIC in a post-processing step (MEMS). A variety of embodiments for each of the functions should be explored, and fabrication flows developed for realising these functions.

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Initial "straw man" specifications were: 4 waveguides, in-plane and out-of-plane motion range 10µm, precision ±0.1µm, post-fixing shift < 0.1µm.

2. **To build an industrial prototype of an assembly machine:** The machine consisting of a 4-axis manipulator, with nozzles for chip handling and sensor systems for process control and a vision system to support the alignment. The machine will be used for single package assembly and contain functions for solder reflow of the PICs; to target passive alignments to better than ±0.5µm will require state-of-the-art or better machine capability. This is a new technology target, it exceeds the initial specifications set in the DoW: *single PIC size 4x4 up to 6x6mm^2, pre-alignment (initial placement) precision ± 1-5µm*, and was motivated by modelling of specific applications chip carried out in WP1.

3. **To address a complete assembly process**: A two-step process based on flip chip assembly technology will be developed for assembling an InP PIC and TriPleX PIC on a common carrier. The first phase, the pre-alignment phase, will be a passive alignment on the basis of industrial solutions for substrate and chip handling, including vision systems. The bonding and electrical interconnection of the chips will be done using solder reflow. The second phase, fine alignment, will be done with the on-chip assembly functions. The two phases must be compatible. Initial specifications: single PIC size 4x4 up to 6x6mm^2, pre-alignment precision ±1-5µm.

4. **Volume and cost compatible assembly:** Typical production volumes for hybrid photonic packages are 50k-100k per year. Device cost targets demand that the cost of the optical assembly process is in the range of 10-20€ per package, i.e. < 4€ per port for a 4-port PIC. The consortium has developed cost models for the assembly suggesting that this is target remains achievable and that the PHASTFlex approach costs in for medium volume applications.

5. **To test out the PHASTFlex concept using** real applications and functional chip designs.

4. Overview of the project achievements

4.1. Introduction

PHASTFlex is a consortium with broad skills (some further consortium details are given in section 6 below). Figure 2 summarises the partner contributions. The PHASTFlex consortium has carried out many fabrication iterations in developing its ideas and expertise, but except where it is specific to the development of ideas there is not space in this overview report to cover everything in detail. Most relevant to the final concept are the second and final full series of assembly trials using custom designed chips fabricated on the Oclaro MPW platform with matching TriPleX fabricated on the LioniX

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platform. In the following sections trials with these piece parts are emphasised. In the remainder of section 4 we review the technical progress in the three main areas of assembly, MEMS development and applications work.

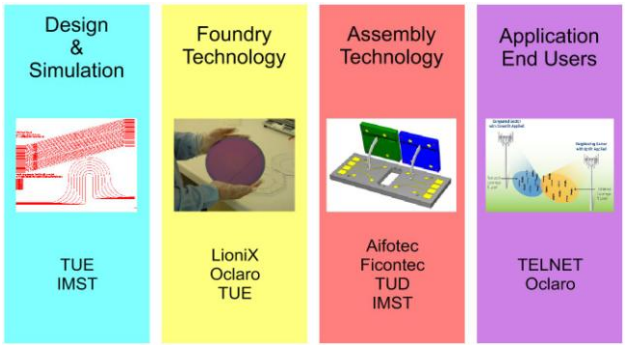

Figure 2: Schematic representation of the consortium partners and their technical roles

4.2. MEMS development

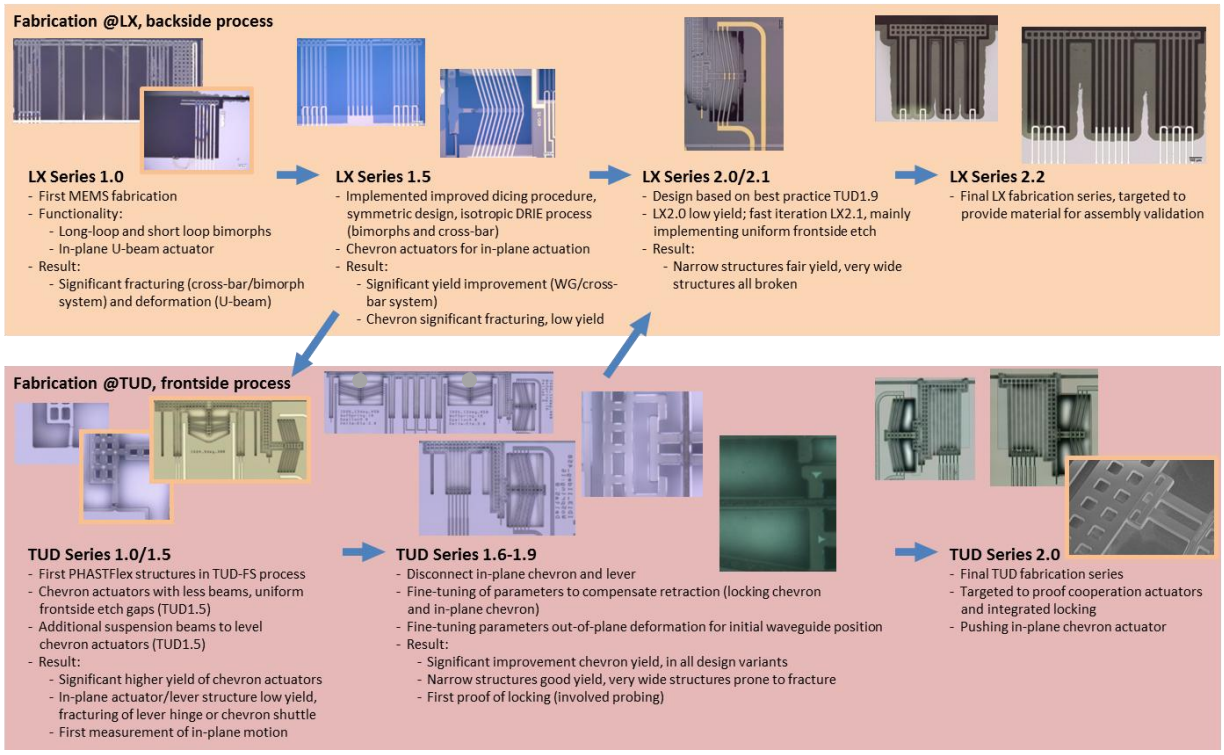

Figure 3: Overview of all design and fabrication series in PHASTFlex.

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Design and fabrication series summary

Figure 3 shows an overview of the many design and fabrication cycles realized in PHASTFlex. The LioniX Series were fabricated in their "back side" process, releasing the MEMS structures with waveguides embedded in SiO_2 by removal of the supporting Si from the back side of the wafer. At TU Delft, the~~ir~~ "front side" process was used, which removes the supporting Si through the openings in the SiO_2 layer. LioniX Series 1.0 and 1.5 (see labels defined in Figure 3) showed principle fabrication feasibility of the targeted structures. In the subsequent TU Delft Series TUD1.5-1.9 design adaptations were made and parameter value ranges were identified. This knowledge was used to design the demonstrator chip Series LX2.0-2.2. Also, a final TUD2.0 Series was fabricated, targeting to demonstrate integrated locking.

The overall design content is summarized here:

- A number of waveguide beams. (In this work typ. 4 plus 2 alignment waveguides, six in total)
- Two sets of short-loop bimorph actuators for out-of-plane translation and rotation around the propagation direction of the light. "Short-loop" refers to the fact that the actuator beams are provided with a short section of poly-Si; the length of this section allows tuning the initial out-of-plane deflection of the end-facets after fabrication.
- A chevron actuator in combination with a lever mechanism for in-plane motion.
- A cross-bar connecting the waveguide beams and actuator structures.
- A MEMS mechanism for locking purposes, adjacent to the waveguide beams.

The targeted waveguide beam pitch in this work is 250µm to be compatible with the Oclaro MPW process. It is now clear that this very wide pitch leads to large MEMS structures which proved hard to fabricate successfully, and it does not favour precise simultaneous alignment of all the end waveguide facets, so other structures on a pitch of 50µm were also fabricated for experimental purposes. Another important issue is the significant space consumption by the chevron actuators, particularly the ones for locking. They have a major contribution to the overall width of the MEMS structures as well.

Design innovation: decoupled chevron actuator

For in-plane actuation a lever mechanism is employed to amplify the short stroke available from the chevron actuators as illustrated in Figure 4. However, the significant post-release deformation of the chevron, in the order of several micrometers, in combination with its relatively high stiffness led to fracturing. Either the hinge of the lever or the chevron shuttle were typical positions where failure occurred. To overcome this issue, an innovative design of the interface between the in-plane actuator and the lever was introduced, see Figure 4 detail. The chevron shuttle and the lever were decoupled in the mask design. The post-release expansion of the chevron actuator is now purposefully used to close the gap during fabrication and make shuttle and lever engage.

In the designs up to TUD1.9 Series, the in-plane chevron actuator was designed *to pull* the cross-bar and waveguide structure. One problem that was identified with this design was an asymmetry at the

locking interface. The chevron actuator is not able to pull the cross-bar sufficiently, and the cross-bar expands in the opposite direction. This leads to a too wide gap at the locking interface, which cannot be closed by the chevron actuator. A solution for this issue was found in reversing the motion direction of the chevron actuator, *i.e.* the chevron is now *pushing* the cross-bar and waveguide system. This was implemented in TUD Series2.0. Figure 5 shows microscopy pictures of TUD2.0 chips with both pulling and pushing in-plane chevron actuators, as well as detailed views of the engaged actuator-lever interface.

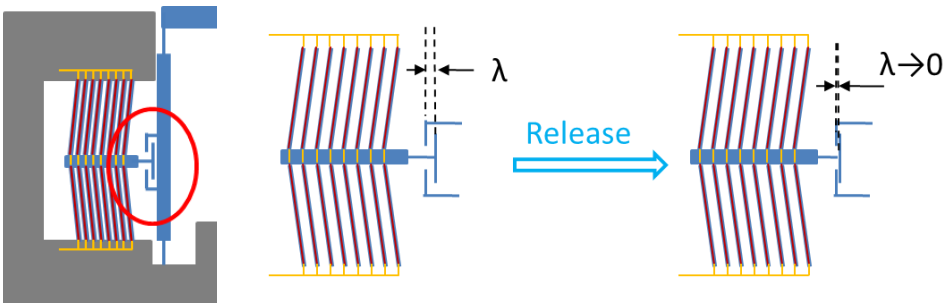

Figure 4: Design innovation: decoupled in-plane chevron actuator decoupled from lever mechanism in the mask design, gap λ closes due to post-release deformation of the chevron actuator.

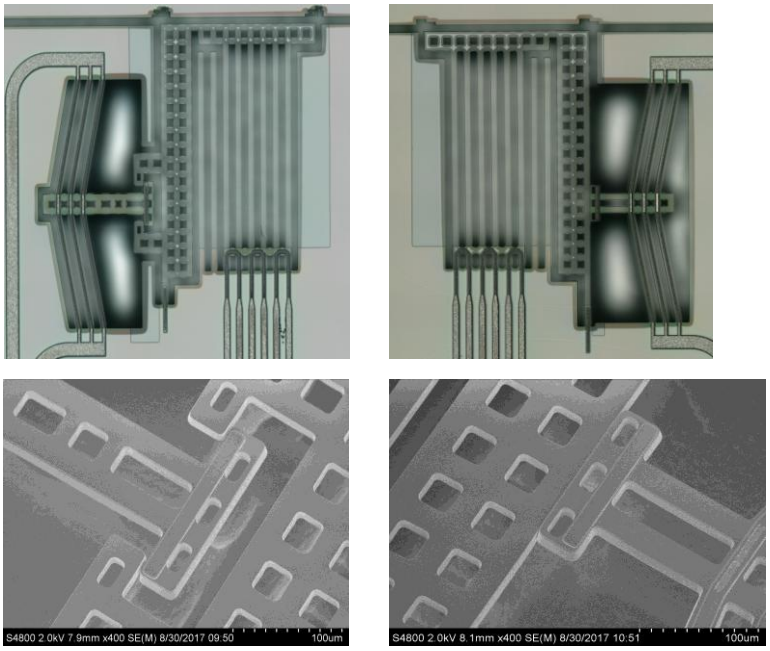

Figure 5: Fabrication results of TUD2.0 Series. Left: design with pulling in-plane chevron. Right: design with pushing in-plane chevron.

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Design improvements and design parameters

A critical step in the fabrication is the release of the structures. The optical TriPleX stack shows significant expansion, and that non-uniformity in release leads to stress situations which cause fracturing. Hence, controlled release is essential. In the designs this is implemented by making all openings in the SiO_2 mask as uniform as possible. After the SiO_2 patterning, trenches are etched in the underlying Si, and if the SiO_2 openings are not uniform, the trench-depth will vary, leading to uncontrolled release in the final step. Wide structures are for that reason provided with regular patterns of etch holes (visible in Figure 5), particularly in the cross-bar and lever.

Simple chevrons show significant out-of-plane distortion. To solve this issue, we have introduced suspension beams, in various layouts, to hold the chevron actuator level (visible in Figure 8). This has shown to be effective, although it obviously comes with some reduction in effective motion.

Finally, to achieve a performing design, several parameters are critical, and through design and fabrication iterations, suitable values and value ranges were identified, as summarized in the table below.

Design target	**Design parameters and values**
~7-9µm post-release out-of-plane deflection of end-facets	Beam length: 900µm Poly-Si length: range 40-80µm
Engaging of in-plane actuator	Gap chevron shuttle-hook in mask design: 7-9µm Chevron actuator dimensions: - Beam length: 400-450µm - Beam angle: 7-13^o - Nr. of beam pairs: 3-4
Chevron Actuators	- Beam length: 400-450µm - Beam angle: 7-13^o - Nr. of beam pairs: 3-4

Actuator performance

Figure 6 summarizes the result of an in-plane motion measurement. The graph shows that with 130mW power, about 1.8µm of cross bar motion is generated. The measured motion amplification the lever offered is ~3.3, which corresponds well with the designed lever ratio of 3.4.

It is understandable that the structures show cross-coupling, since all actuators are mechanically coupled in the design. Figure 7 shows measurement results; the figure to the left shows operation of the left-side bimorph actuator the figure to the right the operation of the right-side actuator. In the graphs two situations are captured: one where the chevron actuator is off and one where the chevron actuator is at a certain power level. As can be expected, at the same power level, the left side actuator

leads to more deformation of the corresponding beams than the right-side actuator; the latter one is closely placed to the lever and chevron actuator, which adds to the out-of-plane stiffness. When the chevron actuator is switched on it exhibits and expected bimorph effect as well, and it lifts the entire structure up. Subsequent operation of the bimorph actuators shows that the motion range that can be obtained is still available. It is clear, however, that the parasitic motion of the chevron actuator reduces the available space in which end-facets can be positioned.

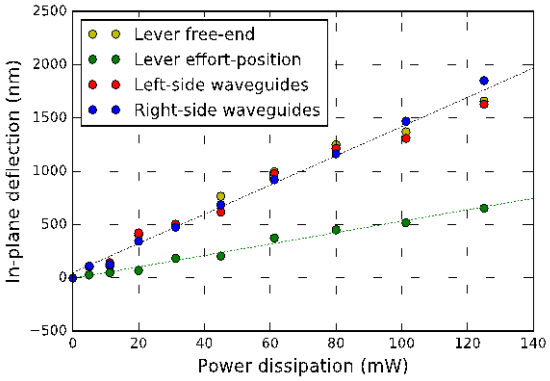


Figure 6: In-plane motion measurement: graph showing motion of chevron shuttle and cross-bar

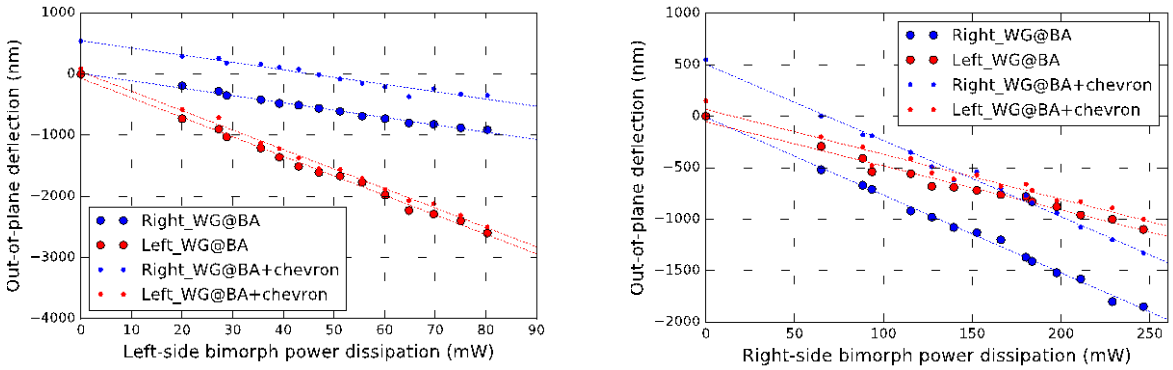


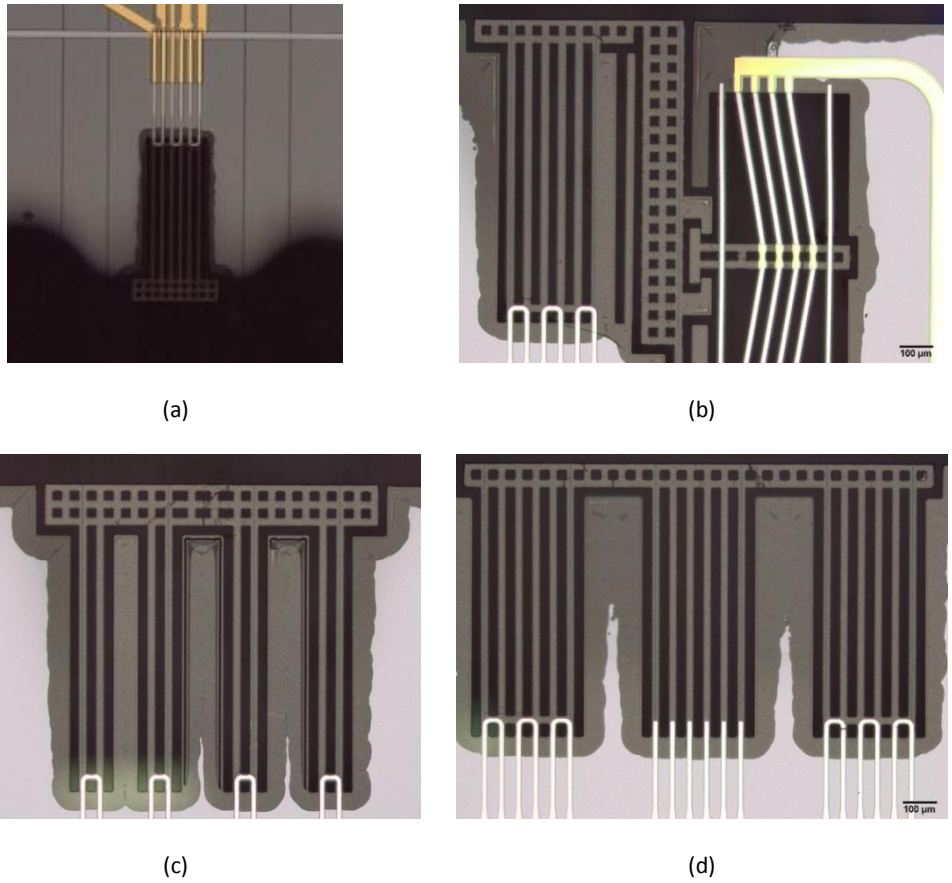
Figure 7:3D motion measurement and Illustration of cross-sensitivities.

First clamping demonstration

Fabrication issues meant that we were not able to test the cooperation of integrated actuators and locking functions together using the electrical drive. To test the potential to lock the structures using friction, we diverted to another approach, using mechanical probing to move the cross-bar to bring it in suitable position. This is a very delicate operation, but proof of principle was obtained and we managed to position the cross-bar such that cooperation with the locking mechanism was possible. The lock was engaged, and stayed in place for about 15 minutes after which it spontaneously disengaged.

Demonstrator chips

Using the LioniX back side process, full demonstrator chips were fabricated. The optical design complied with the demonstrator TELNET InP PIC. The MEMS design was based on best practices learned at TU Delft, summarized above.



(a) (b)

(c) (d)

Figure 8: Series 2.2 MEMS examples of processing (a), chevron detail (b), actuator detail (c) and (d).

Figure 8 shows fabrication results of the final LioniX fabrication run. As the pictures indicate, different waveguide and actuator beam layouts were implemented to explore the design space. White light interferometry imaging was used to characterise these chips. Motion measurements were performed using a laser vibrometer, and confirmed the expected initial out-of-plane position of the waveguide end-facets and movement ranges of the new structures. These measurements indicate that indeed MEMS actuators can be designed and fabricated, and have the potential to perform according to the specifications.

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4.3. Flip chip Assembly

4.3.1. Introduction

In this section the development of the chip assembly process is described. A two step approach is proposed in PHASTFlex. First, a machine based passive assembly stage makes the initial placements of a chip containing the active functions, and an interposer chip on a common carrier. For PHASTFlex the chosen technologies are InP (active) and TriPleX (interposer) optical chips on a LTCC carrier. High end applications desirably require placement accuracies for the two PICs of 1.5 $\pm$ 0.5µm chip separation in the direction of the optical waveguides and required lateral alignment accuracy of +/-2-3µm. These are demanding specifications, at the limits of what can be achieved today, and a dedicated assembly machine has been designed and built for this purpose. Secondly, PHASTFlex has explored an innovative concept in which the waveguides in the matching TriPleX PIC are part of a moveable MEMS structure, released during fabrication. The idea is that actuators and fixing functions, integrated in the same PIC, place and fix the flexible waveguides in the optimal position in the transverse plane (see section 2, and Figure 1). The proposed die attach is via a double reflow flip-chip assembly. Given the expected travel range of the MEMS structures, a few microns, a thin film metallisation has been chosen because of its good bond height control.

4.3.2. Assembly Process Development

In summary, the passive placement of single chips, InP and TriPleX, on diced LTCC by the dedicated assembly machine has turned out to be quite successful, and reproducible, although different reflow cycles and offsets were needed in the second reflow for the placement of the TriPleX. Extension of the process into co-assembly of the InP and the TriPleX onto a common LTCC substrate introduced some further challenges, particularly the characterisation of the thermal expansion and contraction during the TriPleX placement, making the placement accuracy of 1.5±0.5µm gap between the two chips very difficult.

Chip separations in the range 1-5µms have been demonstrated using SEM to support microscope measurements. Good bonds have been achieved for single chips with good electrical connectivity, shear forces can be high and environmental testing is very encouraging, also the results of RF testing. In spite of these isolated successes, there is a lack of reproducibility from assembly batch to batch that remains to be explained.

An example of two chips passively aligned on the carrier in a real assembly is shown in Figure 9 (left). The image in Figure 9 (right) was obtained via mechanical polishing of an assembly embedded in polymer. It shows a rather visually striking image of the MEMS waveguide finger approaching the upside down InP chip on the left, and gives some idea of the scales on which PHASTFlex works. The gold vias and tracks in the multi-layer LTCC carrier are also clearly visible underneath the InP chip. The natural curvature of the waveguide fingers is used to partially accommodate for the difference in chip

heights. It has been confirmed to be ~8µm in realised assemblies and the vertical position is adjustable via the MEMS over a few microns.

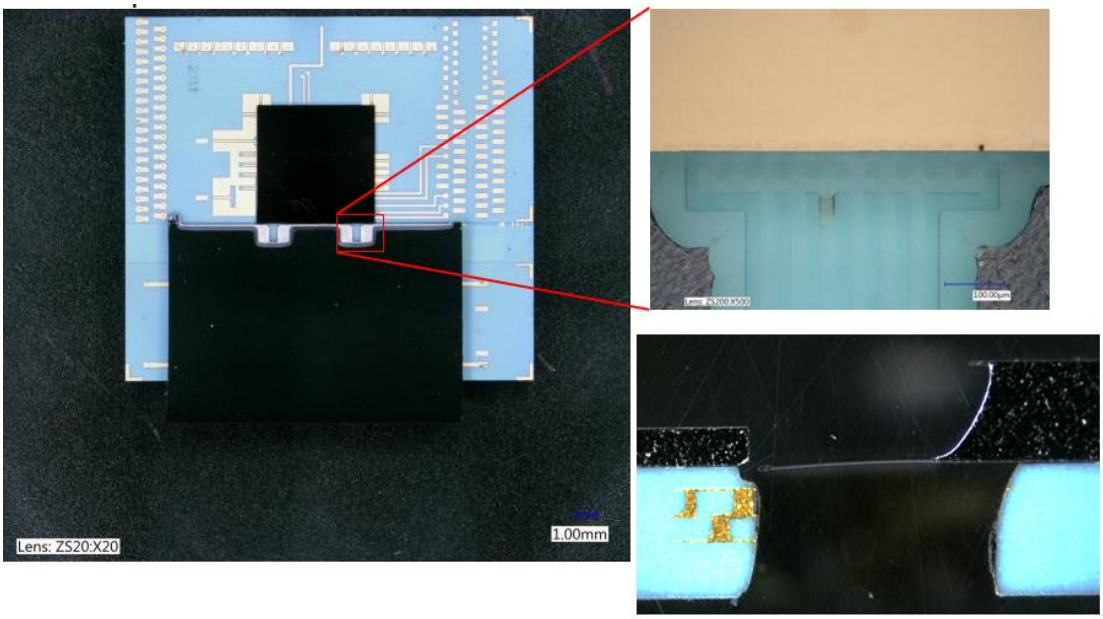

Figure 9: Photograph of a fully assembled InP and TriPleX chips on a carrier (left). Note the overhang at the left of the TriPleX chip which is needed for fibre array unit attach. Cross-section through an assembly showing a waveguide finger and T-bar in front of the InP chip waveguide bottom right.

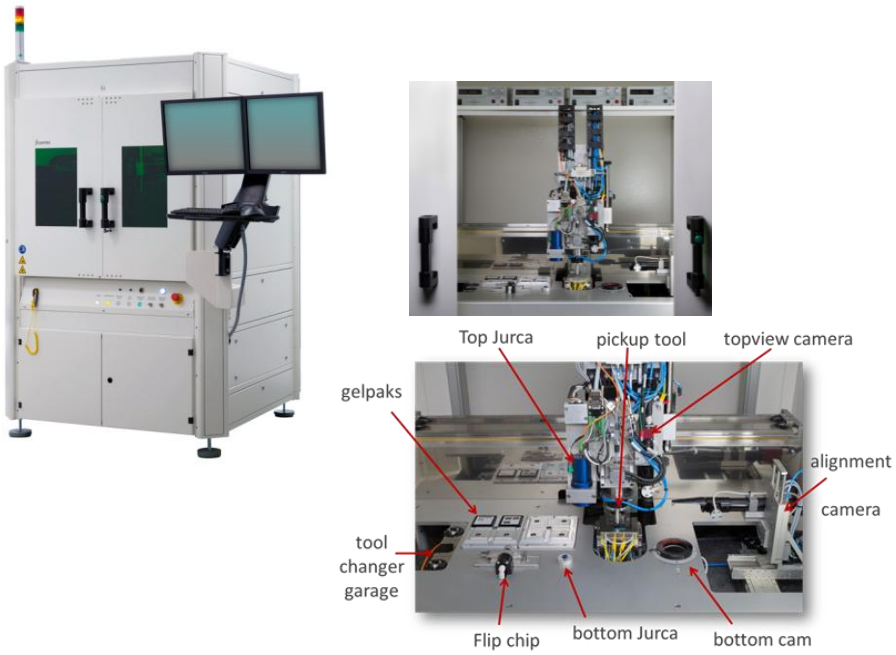

Figure 10 Photographs of the assembly machine: the outer enclosure (left) and internal detail (right)

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Machine development

An automated assembly machine was designed capable of oven bonding of the InP and the TriPleX chips as well as to allow active alignment of the MEMS structures of the TriPleX chip through probe cards and contact pads designed into the LTCC carrier. It was designed and assembled at ficonTEC, and shipped and set up at Aifotec.

Soldering two chips on one common substrate

For PHASTFlex it was decided to use a two step solder reflow. The alternative, to bond both chips in a single reflow, introduces great complexity into the multi-axis alignment of the two chips at the same time. It is necessary, however, in a two step solder reflow to protect the solder pads used in the second reflow from oxidation while soldering the InP chip and also ensuring a uniform distribution of heat across the surface to ensure simultaneous reflow of all solder bond pads. A gas inlet for forming gas or formic acid needed to be implemented which guarantees a homogenous and laminar gas flow over the solder pads without introducing any unwanted cooling effects on the sample. The PICs being developed in PHASTFlex are large in area (5-10mm or more on a side) and flip chip bonded onto a large area carrier, hence a special oven/hot plate eutectic assembly heating process was developed to realize the flip chip hybrid assembly.

Chip Placement Accuracy

The objective of the assembly process was to demonstrate that an InP and a TriPleX chip can be placed on the carrier with the required tolerances on all axis at the same time. To set a good baseline, an accuracy of 2.5 ± 1.0µm is considered a worthwhile short term goal. In the vertical and lateral directions (x- and y- respectively) alignment +/-2-3µm is targeted, values within the movement range of the MEMS, but longer term, target placement accuracies of 1.5 ± 0.5µm (along the optical z-axis) are desirable.

First the InP chip is mounted with the chip facet slightly overlapping the edge of the MEMS access groove in the LTCC. In a second reflow cycle the TriPleX chip is placed in relation to the InP using the machine vision systems to locate the chips. Front to back registration using edges and corners is required to accurately align the waveguides on both chips to each other to enable light coupling since the top surface fiducials are no longer visible in the flipped configuration.

An intermediate step is to identify any fixed machine offsets required to compensate and achieve a final required placement position. Thermal mismatches between the chips and pick up tools (PUTs), carrier and oven need to be characterised but cannot be completely avoided. These parts are all in contact for part of the eutectic heating process so some movement of the piece parts during the heating cycle is to be expected, but so long as these effects are reproducible they can be calibrated out. A PUT based on ceramic “Macor” which is better matched thermally to the chips, was designed for the second step TriPleX assembly. It performed well in operation and the two chip placement trials.

Y-axis alignment: To obtain a calibration of the lateral chip positioning some of the carriers were windowed in the region of the MEMS access groove in the LTCC. The two chip assembly process proceeds in the normal way: the InP chip is mounted overhanging the groove by a small amount. In the second reflow cycle the TriPleX chip is placed in relation to the InP using the machine vision systems to locate the chips. With a windowed carrier the waveguides in the InP chip can be seen after assembly, so it is possible to view the waveguide alignment directly from the back side by viewing through the window. Windowing removes many of the electrical connections buried in the LTCC however, and it is only used in process development to obtain a calibration of the viewing system

Results - Waveguide-axis chip to chip separation: The passive alignment and assembly approach which is used for placing the InP and TriPleX chip onto the LTCC is based on the evaluation of camera images. Placement accuracy is therefore largely dependent on the accuracy of image recognition by the cameras mounted in the machine. A calibration exercise was set up between partners in order to check the distance measurements recorded by the machine. Measurements from the machine cameras were compared with low voltage SEM measurements and external microscope images at Aifotec and TU Eindhoven.

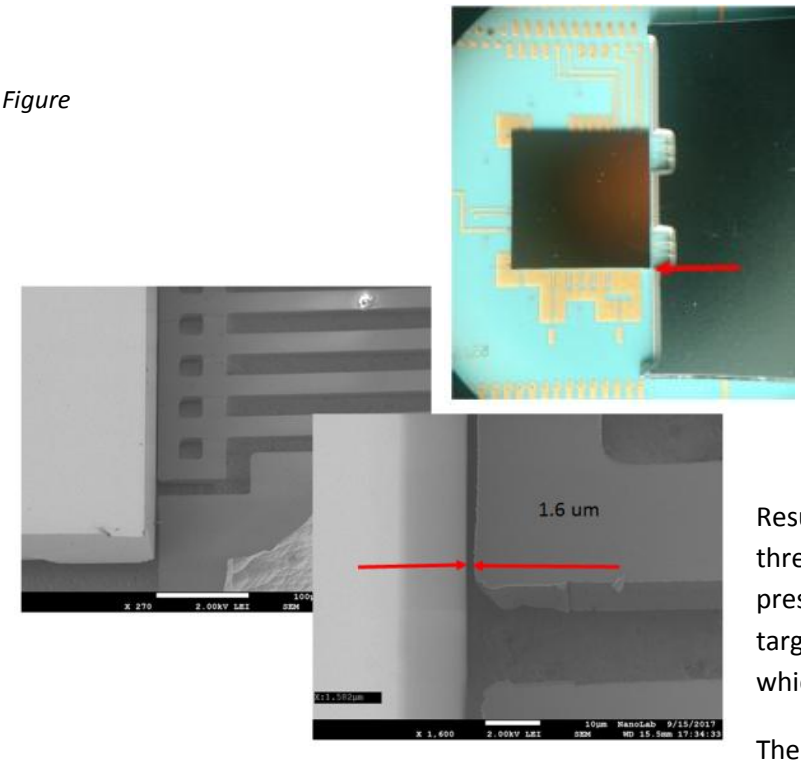


Figure 11 SEM measurement results of the sample assembly on carrier 2.12.8. A cross calibration of the SEM measurement to the lithographically defined beam width was used as a dimensional check.

Results of the gap measurements for three of these assemblies are presented below in Table 1. A nominal target gap is set for the each assembly which contains a calibration offset.

The SEM measurement results give confidence that the targeted gap set for these assemblies could yield results in the desired range, but the machine measurements do have differences and aren't the same as the SEM measurement. This is due to the fact that gap measurement in the machine is done by image processing and is highly dependent on gray scale imaging and hence the appearance of each MEMS set.

Dissemination level		
PU	Public	

Carrier ID	Nominal Gap as Targeted in the process (µm)	Gap the machine measures (µm)	Gap as measured by the SEM (µm).
2.12.7	10	2.5 – 3.0 µm	1 - 1.6µm
2.12.8	10	4.5µm	1 – 1.6µm
2.10.3	10	3.0 – 3.6µm	Sample broken in transportation

Table 1: Tabulated results of the chip separation measurements from the ficonTEC machine and by SEM. Photographs of one of the samples, sample 2.12.8, are shown in Figure 11.

4.4. Test and Applications

Introduction

In this section the design and function of the chips and carriers used in the series 2 work are described, but first lab bench level trials of the MEMS operation under electrical drive are reported. Characterisation work on RF performance of the assemblies, and environmental testing is also described.

Lab bench tests MEMS actuation of flexible waveguides

The coupling between the Oclaro InP samples and TriPleX MEMS with matching mode size has been analysed in a lab setup in order to experimentally verify the coupling efficiency and the dependence on the electrically driven actuation of the MEMS. To perform the tests with a dedicated Oclaro test chip, a TriPleX MEMS counterpart was used, with matched waveguides, which was first characterised by measuring the mode field and by mapping the movement range. Before characterizing this chip, a fibre array unit was connected to the TriPleX chip to give a stable input of the optical signal. As expected the $1/e^2$ beam diameter was determined to be approximately 3 µm in both the lateral x-direction the transverse y-direction.

The next step was to map the displacement obtained when different electrical power was applied to each actuator individually. To measure the displacement of the structure, the light of two adjacent waveguides was captured in an IR camera. The separation between these waveguides is very accurately known from the mask design of the MEMS chip and allows for absolute displacement calibration. By applying a bias voltage to the MEMS actuators, the near field image will move across the camera sensor and the movement is determined. The resolution of the system, for this configuration, was determined to be better than 200nm. With this method we determined the out-of-plane displacement. Several chips have been tested from wafers with different poly-silicon actuator thickness. For the wafers with a poly-silicon thickness of 5µm the maximum power applied to each of

the two actuators was 100mW. The waveguides show a movement range of 8µm. The measured movement range is sufficient for proper compensation of the initial placement inaccuracy.

Position drift under actuation

In order to arrive at a good alignment and fixing procedure, it is important to understand the time stability of the MEMS waveguide structure when activated. To characterize this, a voltage step was applied to the actuators and the time dependence of the displacement was recorded in the IR camera. We observe that the waveguides first move to their expected position but then drift from that position. This effect is understood to be due to a thermal relaxation of the whole chip to an overall thermal equilibrium. The relaxation time is about 1500s for the long actuators and about 1000s for the short ones. From the figures we extract that, directly after positioning the MEMS, the drift is approximately 0.6nm/s. That means that for a maximum allowed drift of, say, 20nm, we would need to fix the structures within 30s. That is well within the expected time needed.

Coupling between actuated waveguides and InP

Next step is to measure the actual optical coupling between the Oclaro test sample and the TriPleX MEMS waveguides, while operating the actuators. To this end, the Oclaro test sample was mounted in a dedicated sub-mount, Figure 12. The contact pads from the InP PIC were wire bonded to a signal distribution PCB.

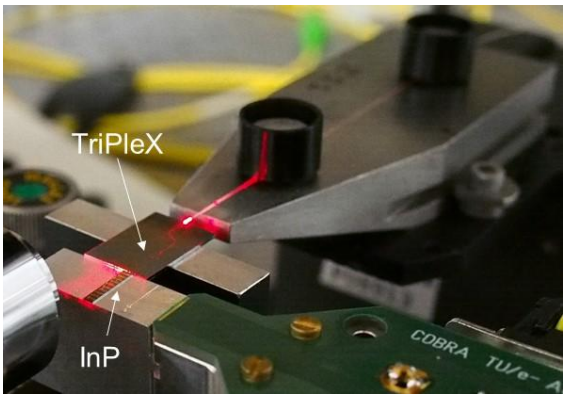
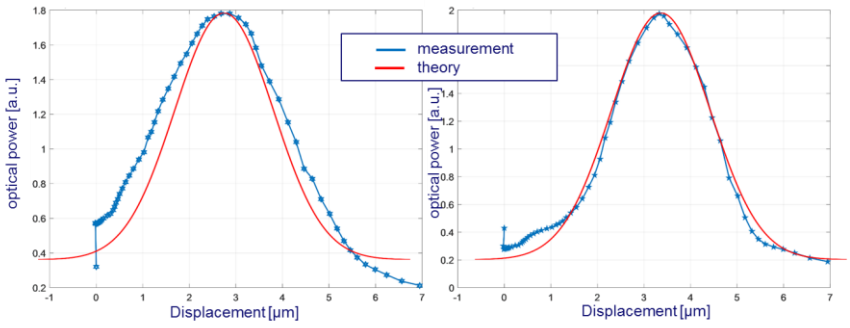


Figure 12: Photograph of the TriPleX with MEMS waveguides aligned to the Oclaro test chip.

Figure 12 shows the lab-bench setup with the TriPleX sample on a two axis stage, and light coupled into it from an optical fibre on a 3-axis stage. The Oclaro test chip is on a 6-axis stage aligned to the TriPleX waveguides. Using the data from the displacement mappings we can calculate the displacement of the beam versus MEMS actuation power. This has been used to calculate the modal overlap versus displacement, which is shown in Figure 13. The match between theory and experiment is very good.



Dissemination level		
PU	Public	

Figure 13: Optical power from detected photocurrent in the Oclaro InP chip as a function of the MEMS displacement showing good match with a Gaussian curve with 3µm beam diameter.

Applications

Two application ASPICs have been made for demonstrating the PHASTFlex concept: one application by TELNET and one by Oclaro. TELNET targets the development of a multi-wavelength 40G WDM photonic transceiver for the next generation of Passive Optical Networks (PONs). The schematic of the proposed transceiver for PHASTFlex is shown in Figure 14.

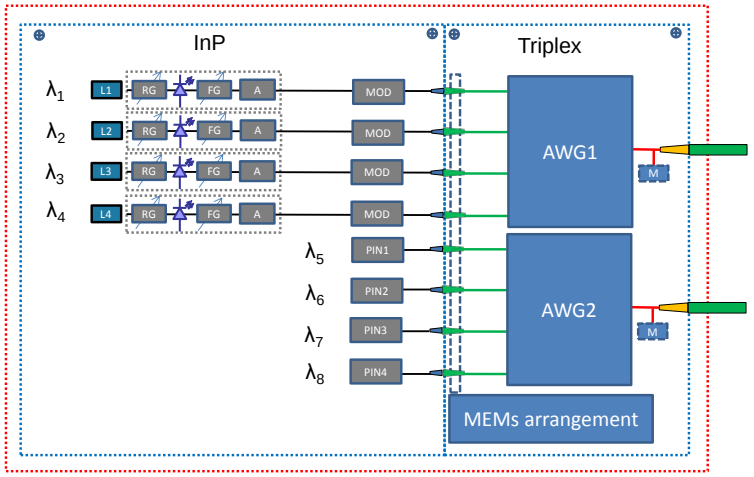


Figure 14: Schematic of the NG-PON ASPIC proposed by TELNET.

The transmitter and receiver active functionalities of the transceiver were designed using the Oclaro InP-based MPW platform, while the mux and demux passive components were designed in LioniX´s TriPleX technology. MEMS arrangement will be integrated in the TriPleX chip in order to be able to flexibly aligning and fixing both chips in order to be able to assemble them in a LTCC carrier using flexible waveguide packaging technology developed in the PHASTFlex project.

Oclaro's MPW platform supported a full range of transmitter and receiver functions; lasers, phase modulators, photodiodes, Bragg gratings and composite passive waveguide structures such as Multimode Interference devices (MMIs) and Arrayed Waveguide Devices (AWGs). The TELNET ASPIC has made good use of the overall MPW capability.

TELNET ASPIC

The InP TELNET ASPIC has been designed with Oclaro's MPW Process Design Kit (PDK). A photograph of the fabricated chip is shown in Figure 15. The total circuit size is 6x6 mm.

The ASPIC consists of a 4-channel multi-wavelength transceiver. The transmitters are placed in the right side of the chip and consist of four DBR laser emitting at four different wavelengths and four Mach-Zehnder modulators for 10 GHz modulation. The receivers consist of four pairs of SOA + PIN

detectors and are placed in the left side of the chip. The receiver will operate with a bandwidth of 10 GHz. For the PHASTFlex hybrid integration approach, light sources and photodetectors were added for the alignment procedure. These were placed on the sides of the signal waveguides and allow the automatic alignment. Also, in-line optical power monitors, that tap only a small fraction of the incoming or outgoing optical power, were added in all optical I/Os for redundancy purposes.

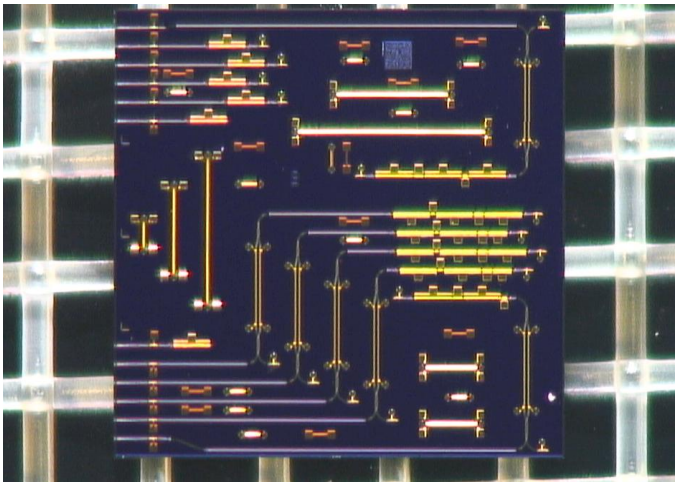


Figure 15: Photograph of the TELNET NG-PON fabricated by Oclaro.

For better understanding and characterization of the final assembly, several test structures were also included. These structures will allow the characterization of each individual element of the ASPIC, daisy chain test of the bonding, and improve the mechanical stability of the assembly. These include DBR lasers, PIN detectors, MZM modulators and GSG RF lines. On wafer test and chip testing were used to validate the process run, but there is not space in this report to go into detail.

LTCC carrier

The LTCC carrier for the TELNET ASPIC consists of a 7 layers stack-up of DuPont 951 with a final thickness of 980µm (140µm each layer). The final dimensions of this LTCC carrier are 18.5mm x 20.8mm.

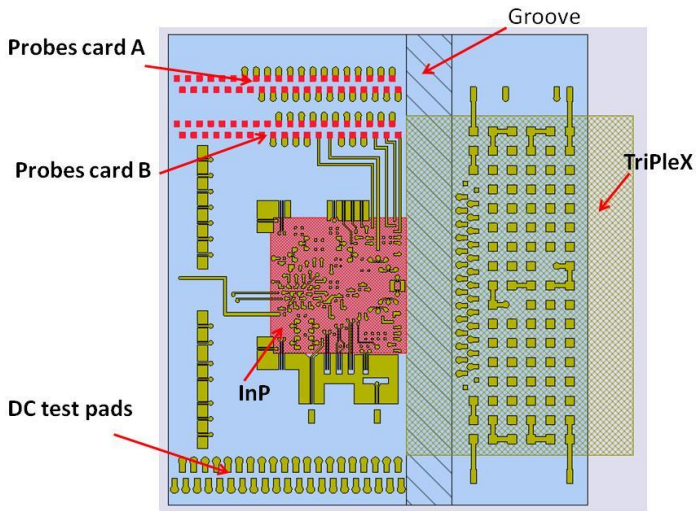


Figure 16: Top view of the LTCC carrier

Figure 16 shows the top view of the carrier. It shows the InP chip (red) in front of the TriPleX chip (dark yellow). The carrier has two set of pads on the upper left side where the probe cards used during the alignment process may be contacted. These two set of pads (A and B) are related to the two independent alignment mechanisms in

the TriPleX chip. A third set of DC pads has been included on the lower side of the carrier. These pads connect to the different InP chip pads that need to be monitored during tests or used during the operative mode of the chip. Finally, a 60 µm groove has been diced on the carrier underneath the TriPleX chip. This groove provides the required free space for the chip's mechanical structures.

To test the various RF lines on the InP chip, the carrier includes different RF connections. A row of GSG (Ground Signal Ground) pads is used to measure the CPW (Co-Planar Waveguides). The MZ RF lines are connected by GSSG (Ground Signal Signal Ground) pads and the RF pins are connected by GSG pads.

TriPleX ASPIC

The TriPleX ASPIC that connects to the TELNET NG-PON application chip uses AWG (de)multiplexers. It also provides passive waveguides and mode expansion from the coupling interface to the FAU. For the AWG input and output channels are connected to TriPleX facets at the InP as well as the fibre interfaces. The optical layout of the TriPleX chip comprises two independent AWGs for implementing the mux and demux passive functionality of the transceiver. This 4-channel cyclic device has a channel spacing of 100GHz and an FSR of four times the channel spacing, or 400GHz. The resulting AWG layout is shown in Figure 17[2].

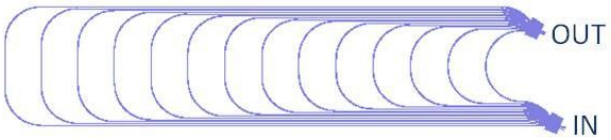


Figure 17: AWG mask layout.

The simulated and measured responses of the AWG are shown in Figure 18. Both the channel spacing and the free spectral range (FSR) perfectly match the design values of 100 GHz and 400 GHz, respectively. The excess loss is around 4 dB, which is a reasonable value, certainly when considering that these are among the first AWGs to be fabricated in this waveguide materials structure. Although the crosstalk level can be improved, the overall performance is adequate for demonstration of the system concept.

[2] *The AWG design has been carried out with the support of an external design service provider with access to device models calibrated on the TriPleX platform: http://brightphotonics.eu/*

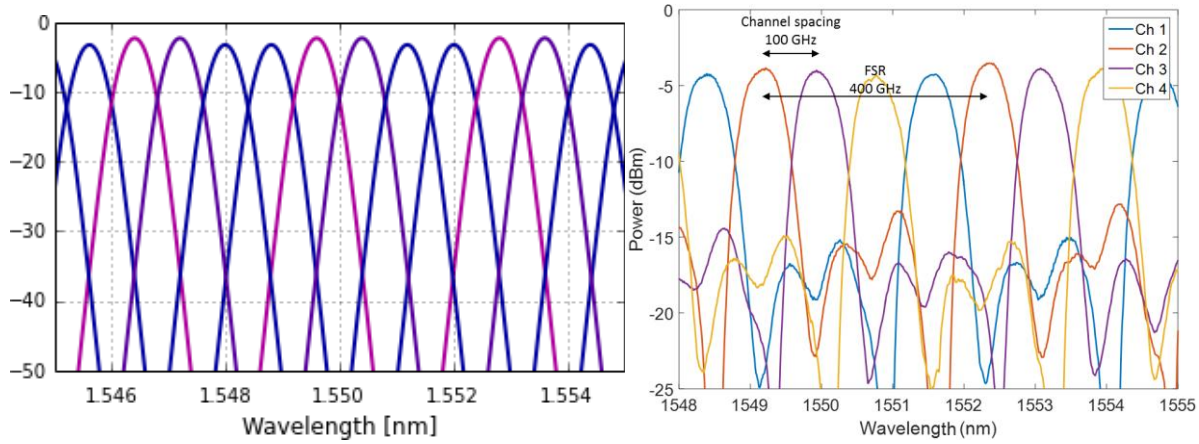


Figure 18: AWG response simulated (left) and measured (right).

RF performance

The RF performance has been evaluated on two types of assembly. In addition to the TELNET chip assemblies, a 100G amplified modulator chip supplied by Oclaro and assembled on the co-designed LTCC substrate with matching TriPleX have been assessed. The Oclaro 100Gbps DP-QPSK ASPIC provides high performance coherent optical transmitter functionality in a miniaturized footprint and is well suited to the application of high-density pluggable modules. In an in-house development project Oclaro has realised an enhanced dual-polarization (DP) in-phase and quadrature (I&Q) optical PIC which integrates semiconductor optical amplifiers (SOAs) together with modulators with a single sided optical interface. Oclaro has made these devices available to PHASTFlex in order to elucidate the specific challenges and opportunities of the flip-chip bonded approach and the use of MEMS-enabled optical coupling.

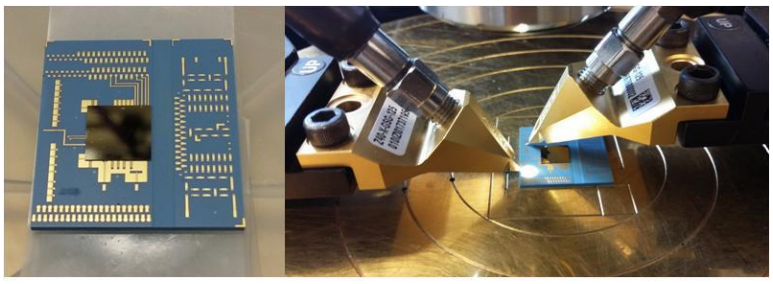


Figure 19: a) assembled TELNET InP chip on LTCC carrier b) RF measurement set-up

The RF performance of the 100G chip from Oclaro when assembled on an LTCC substrate has shown good agreement with respect to the RF performance expected from the chip specifications. The use of CPW lines on the LTCC has shown repeatability on the measurements. Measurements were carried out up to 30GHz and the frequency bandwidth has been proven to fulfil the chip specifications in

terms of reflection coefficient and transmission coefficient up to ~20GHz. The use of CPW lines on the substrate is limited to the access and position of the bond pads. In the 100G chip case, the pads are on the perimeter of the chip and the access seemed to be feasible with CPW lines. The use of striplines to feed the RF signal to the 100G chip has also been proven. Furthermore, striplines allow flexible routing of shielded RF-lines in inner layers of the LTCC carrier. In the PHASTFlex series 2.0, the assembly has shown lower repeatability in terms of electrical connectivity and also in RF performance with bandwidth ~15GHz. Measured lines have shown that transitions between stripline and CPW have resulted in a frequency bandwidth reduction but the overall performance can still be considered acceptable.

Concerning the RF measurements of the TELNET application chip, a disagreement between simulations and measurements has been observed. The measured frequency bandwidth resulted to be narrower than expected. The chip and the carrier alone have been independently measured and the results agreed with the expected RF performances with reflection coefficients <-10dB up to 12GHz. On the other hand, the effect of flip-chip assembly of PIC on LTCC in terms of RF-performance can be predicted by FDTD-Electro-magnetic simulation. In the case under study where CPW lines are utilized on the PIC, the fields of the waveguide are so concentrated in the vicinity of the surface that there is no significant influence from the LTCC surface. In that case, an unexpected effect of the bond pads may be considered as the reason of such bandwidth reduction, but no conclusions can be taken at this stage and more assembled devices should be needed.

Environmental Testing

Thermal Cycling at Aifotec and LioniX: As a demonstration of the mechanical strength and stability of the assemblies the samples were taken through thermal cycling at Aifotec, LioniX and thermal cycling and shock and vibration testing Oclaro. An initial baseline in temperature cycling was first demonstrated at Aifotec where the assembled parts were tested for mechanical strength and electrical continuity by measuring resistance across the bond pads. The samples were then subjected to thermal cycling by running them in an environmental chamber from 0°C to 70°C at 0% relative humidity for 10 cycles. No changes over cycling were observed.

The TriPleX assembly used an electrical test chip (no optical part) with the CrPtAu metallization specified for series 2.0. These samples had already seen 20 cycles over 0-70^{o}C at Aifotec. Three daisy chains (which are electrical test structures widely over the chip) were tested after shipment and found to be fully functional electrically. The main aim was to test the response of the assembly to temperature cycling down to -40^{o}C. In order to control condensation, (this assembly was not packaged in its own separate outer enclosure), the chamber was heated to 100^{o}C for 30m to remove moisture before cycling. Over eight temperature cycles the minimum temperature was decreased in steps to -40^{o}C followed by two further cycles with increasing hold times at -40^{o}C. At each stage the daisy chains were tested; only small resistance changes were observed.

Thermal Cycling, and Shock and Vibration testing at Oclaro: Six samples were wire bonded in generic packages at Oclaro and lidded for the climate chamber. These were temperature cycled. The temperature range used was -40C to 85C with a ramp of 10C/min. Dwell time was 15 minutes with a total of 100 cycles. Comparing the pre and post thermal cycling results show only a few changes in resistance on the interconnects on the first four units tested but everything else was good as expected, with no failure of chip to substrate bond. The assemblies were then subjected to shock and vibration testing. Specifically: Vibration 22G , 20Hz->2000Hz->20Hz , 4mins/cycle (from low to high and return to low), 4 cycles per axis. (Schedule based on MIL-STD-883F); shock 500G, 1msec pulse, 5x/axis, 6 directions. Again, no failures of chip to substrate bond were recorded, but changes in the electrical characteristics were observed which will need further investigation.

5. Prospects for PHASTFlex

Significant further investment will be required to bring PHASTFlex to full fruition, but the advantages to be gained are also significant. The platform based co-design and fabrication of the matching piece parts has been one of the successes of the project, and initial problems encountered in the thin film solder deposition on polished LTCC have been overcome. Flexible waveguide beam systems have been fabricated, together with integrated actuators for motion in three directions, alongside a partial demonstration of an integrated locking mechanism. Finally, demonstrations have been made of electrically driven finger movement of MEMS chips on carrier. Significant challenges remain for yield of the MEMS structures and in reproducibility of the two chip assemblies; however, good reproducible bonds have been achieved for single chips with good electrical connectivity, shear forces can be high and environmental testing is encouraging, also the results of RF testing. Chip separations in the target range 1 to 5µms along the optical axis have also been demonstrated using SEM to support microscope and machine based measurements.

A major opportunity exists in the optimization of the MEMS functionality. The current design concept uses bulky actuators for in-plane positioning (thermal chevron actuators). It is believed that these can be replaced with in-plane bimorph actuators. This reduces significantly the size of the MEMS section, thereby improves the fabrication yield relaxes the demands on the precision in chip assembly because of the larger motion range that can be expected, and reduces the MEMS component cost (smaller chip real estate). Modelling confirms the expectation of in-plane bimorph actuators, and as part of the PHASTFlex project the feasibility of fabricating in-plane bimorph actuators was verified.

Next to the chip prices the main contributor of the module price in volume production will be the cost of the assembly (and packaging). In current low volume assemblies, where assembly steps involve significant manual labour, the chip price may be about 10-20 % of the cost price of the module. The PHASTFlex concept aims (as do all assembly processes) at significant assembly cost reduction resulting in component (chips and carrier) fabrication cost becoming the dominant factor. Based on our continuing analysis we can conclude that not only does the PHASTFlex assembly concept still look promising compared to where packaging technology is today, and we believe costs in for medium to

high volume applications where multiple channel operation is required, but also offers a potential way around some assembly issues in current module builds based on micro-optics.

6. General project facts and figures

The website address for the project is http://phastflex.eu

Partners and roles in the PHASTFlex consortium are:

TU Eindhoven (Coordinator): Project administration. Lab bench trials of MEMS chips, structural characterization of carriers and assemblies. Dissemination.

TU Delft, Netherlands: MEMS design and MEMS processing, dissemination.

Oclaro Technology, Ltd., UK. Applications and applications requirements. Environmental testing.

LioniX International BV, Netherlands: TriPleX design and fabrications. Implementation of MEMS designs in TriPleX. Technical lead.

Willowphotonic Ltd, UK: Administration, technical management and dissemination

ficonTEC Service GmbH, Germany: Development of the assembly machine.

IMST GmbH, Germany: LTCC carrier design and fabrication. RF testing.

TELNET Redes Intelligentes SA. Applications, GPON.

Aifotec AG, Germany: Flip chip assembly process development.

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7. Further reading

[1] TriPleX: a versatile dielectric photonic platform Kerstin Wörhoff, René G. Heideman, Arne Leinse and Marcel Hoekman. (2015) Adv. Opt. Techn. 2015; 4(2): 189–207

[2] Photonic Hybrid Assembly Through Flexible waveguides (2016), K. Wörhoff; A. Prak; F. Postma; A. Leinse; K. Wu; T. J. Peters; M. Tichem; B. Amaning-Appiah; V. Renukappa; G. Vollrath; J. Balcells-Ventura; P. Uhlig; M. Seyfried; D. Rose; R. Santos; X. J. M. Leijtens; B. Flintham; M. Wale; D. Robbins; SPIE paper Vol 9891, doi: 10.1117/12.2227814

[3] MEMS-assisted fiber-chip coupling X.J.M. Leijtens, R. Santos, M. Tichem, K. Wörhoff and K.A. Williams. Proc ECIO 2017 Eindhoven.

Dissemination level		
PU	Public	