SEVENTH FRAMEWORK PROGRAMME THEME 3
Information and Communication Technologies (ICT)
ICT-2009.3.3 – Flexible, organic and large area electronics

POLARIC

Printable, organic and large-area realisation of integrated circuits

Deliverable D3.1

Design of universal OTFT fabrication platform

PUBLIC PART

Responsible beneficiary: **Imperial College London**
Nature of deliverable[1]: R
Dissemination level[2]: PU
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Date: 2012/04/18
Version: 0.8
Status: Final version approved by the Steering Group

[1] R = Report P = Prototype D = Demonstrator O = Other

[2] PU = Public, PP = Restricted to other programme participants (including the Commission Services), RE = Restricted to a group specified by the consortium (including the Commission Services), CO = Confidential, only for members of the consortium (including the Commission Services

Draft revision history (to be sent to the Coordinator)

Version	Date	Author	Summary of main changes and/or status of the version
0.1	16th April 2012	Beinn Muir	1st draft, sent to WP3 leader
0.5	16th April 2012	Alasdair Campbell	Accept 1st draft, sent to the consortium
0.8	18th April 2012	Beinn Muir	2nd draft incorporating consortium corrections
0.8	18th April 2012	Alasdair Campbell	2nd draft agreed by WP3 leader

Approval for final version (to be submitted to the Commission)

Contributor	Meeting date	Meeting place	Remarks
Steering Group	18.4.2012	E-mail decision	Approved and marked as version 1.0

Public description of the deliverable

A universal organic thin film transistor (OTFT) fabrication platform has been successfully designed. This is as a test-bed for large-area printing of OTFTs on flexible substrates, and for the rapid feedback of information and process development within the POLARIC project. The design consists of an array of 30 TFTs, 10 capacitors, a range of different resolution test areas, and different alignment and positioning features. Transistor channel lengths and widths were designed to correlate with POLARIC project workpackage 4 to maintain a common framework for comparison within the consortium. The mask set allows the fabrication of all four active transistor layers (semiconductor, insulator, gate, source and drain). It is compatible with the registration, alignment and substrate dimensions of all POLARIC relevant fabrication techniques and equipment, including gravure printing and photolithography. This mask set design has been made available to all POLARIC partners within the Consortium.