1. Publishable summary

1.1 Introduction

Printed electronics uses printing and other roll-to-roll-processing (R2R) based methods to fabricate electronics. This brings important advantages such as flexibility in changing the production flow, flexible or bendable products, and possibility to process large-area at once. The most commonly known functional components or devices of the printed electronics are organic light emitting diodes (OLEDs), organic photovoltaics (OPV), sensors and electronic circuits.

To date the use of organic thin film transistors (OTFTs) and electronic circuits based on these in industrial products has been limited. The main obstacle for substantial market penetration of such organic electronic components has been the inability to achieve sufficient device performance using large-area and high-volume production methods such as printing. This has been mainly caused by the limited ability to achieve sufficiently small patterns in the OTFTs when using standard printing techniques. This has delayed the commercially viable implementation of organic transistors in complex electronic circuits and the system development.

In response to this, the POLARIC project aims to revolutionise the way printed electronic circuits are made and simultaneously, take a major step forward in the device performance. The project partners are 3D-Micromac AG (Germany), AMO GmbH (Germany), Asulab Division of The Swatch Group R&D Ltd (Switzerland), BASF Schweiz AG (Switzerland), Cardiff University (UK), CSEM (Switzerland), Fraunhofer EMFT (Germany), IMEC (Belgium), Imperial College (UK), Joanneum Research (Austria), micro resist technology GmbH (Germany), Obducat Technologies AB (Sweden), and VTT (Finland) as the coordinator. The project is spread over the years 2010 – 2013. This document describes the project objectives, work progress, and achievement for the second project period (year 2011).

1.2 Objectives

The objective of the project is to realise high-performance organic electronic circuits using large-area processing compatible fabrication methods. The high performance of the organic circuits referred to here means high speed (kHz-MHz range), low operating voltage (below 5 V), low power consumption, and low parasitic capacitance. The OTFT fabrication development will be focused to enable a high resolution nanoimprinting lithography (NIL) step, which is compatible with R2R processing environment. Applying NIL will enable smaller transistor channel lengths (below 1 μm) and thereby an increase in the performance of the device. Another important concept to improve the performance is the self-aligned fabrication principle, in which the critical patterns of the different layers are automatically aligned in respect to each other during the transistor fabrication. This decreases the parasitic capacitances and thereby increases the operating frequency, decreases the gate leakage currents, and is one of the key elements to enable the use of large-area fabrication techniques such as printing.

Also complementary transistor technology will be developed, enabled by availability of both n- and p-type organic semiconducting materials. The high performance organic transistors will be tested in basic electronic building blocks such as inverters and ring oscillators. The technology development will be exploited in the active matrix liquid crystal display (AMLCD) and radio-frequency identification (RFID) demonstrators. In addition to showing that sufficient performance can be reached without sacrificing the mass fabrication approach, solutions for the fabrication of roll-to-

roll tools in order to make serial replication viable will be provided. Finally, the circuit design, modelling, and characterisation of organic electronics will be developed to support the fabrication technology development in the project.

1.3 Work progress and achievement during the second reporting period

1.3.1 Thin dielectrics for short channel OTFTs

The dielectric layer to which is referred here is the insulating layer between source–drain contacts and gate contact in OTFT. Thin dielectric layer is a necessity for a short-channel transistors. The manufacturing of highly stable OTFTs for the project demonstrators requires a wet coating process for reliable and homogenous dielectric layers with a dry thickness down to 100 nm. To reach highly reliable dielectric films, photo crosslinkable poly(methyl methacrylate) (x-PMMA) has been selected as the dielectric material to be used with demonstrators. During the reporting period, further tests of process parameters were first done on Si wafers. The dielectric process was then transferred from rigid samples to 4" flexible foils in order to support the fabrication development towards the first demonstrator (transistor matrix for the AMLCD). The handling was adjusted in such a way that no permanent fixing to any rigid carrier was necessary. In addition, web coating (R2R processing) was started with promising results and R2R processed dielectrics have been demonstrated. However, the process parameter needs to be adjusted in order to enhance the electrical performance of dielectrics.

1.3.2 OTFT channel miniaturisation

In a field-effect transistor, which is the type of the transistors studied in this project, the channel length is defined by the distance between the source and drain electrodes. In order to maximise the operation frequency of the device, the transistor channel length should be minimised. The project addresses this challenge by applying nanoimprinting lithography in fabrication of OTFTs, which allows reaching very small patterns with dimensions below 1 μm. Several devices with such short channel lengths were manufactured and electrically tested. In addition to introducing the NIL fabrication step, upscaling the process area towards large-area fabrication is another challenge of the project. During the reporting period, a significant part of the work done in the OTFT channel miniaturisation was devoted to scaling up the imprint process from small area batch process (millimeter scale) to 4" x 4" process. This is considered as an in-between step in upscaling the OTFT fabrication processes towards R2R.

1.3.3 Complementary OTFT technology

In order to decrease operating voltage and power consumption, and increase noice margins, n- and p-type OTFTs and organic complementary circuits are developed in the POLARIC project. Here, the R2R compatible gravure contact printing fabrication method combined with other techniques is used. During 2011, the activities focused on developing a full and versatile multi-step process flow and related designs, which are necessary to fabricate transistors compatible with the demonstrators. In addition, different process steps, especially printing the dielectric and semiconductor layers of the OTFT, were developed further.

1.3.4 Circuit development for organic integrated circuits

In the circuit development, technical boundary conditions are collected from the fabrication tools to be used, and from them, the design rules respecting the specifications required for the demonstrators are deduced. During the reporting period, several design iterations were done to support the fabrication technology and demonstrator development. One of these was an updated design for the AMLCD transistor matrix (Demonstrator 1). In addition to these activities, a new approach for the

parameter extraction has been studied, which is a step towards a design methodology called g_m/I_d. It is used in the silicon industry to design analogue circuits regardless of the process parameter variations. An Outstanding Paper Award was awarded to the published paper[1].

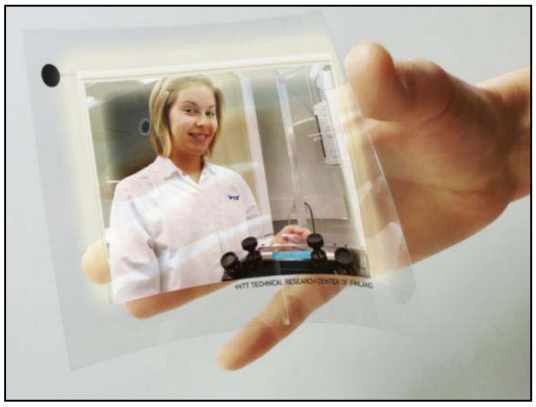
1.3.5 Manufacturing platform development

In the project work plan, there is a dedicated work package for the development of the tooling, especially shim fabrication for the NIL, and overall manufacturing platform development of NIL based OTFTs. One of the targets is to establish a manufacturing platform for the NIL based and R2R fabricated OTFTs. In the second period of the project, the activities here continued on the progress that was made in the first period with regards of the validation of the technologies and processes. On the tooling side, more Ni shims have been produced. The master making process chains have been modified to implement the self-align concept that has been agreed as the basis of the demonstrator OTFT fabrication.

1.3.6 Demonstrators

In the project plan, the following demonstrators are specified:

- Demonstrator 1: OTFTs with micron spaced electrodes for AMLCD fabricated in a large-area nanoimprinting batch (6") process
- Demonstrator 2: Active matrix LCD
- Demonstrator 3: Roll-to-roll processed load modulator for RFID tag
- Demonstrator 4: Roll-to-roll processed antenna capacitor and rectifier for RFID tag



An artistic rendering of the vision of a flexible display

The details for these demonstrators were specified during the preparation of the project. However, matching these specifications with the process flow development proved to be more challenging than expected. To compensate the delays originated from this, a redefinition of the project plan was done. In the new work plan, the Demonstrators 3 and 4 (RFID) will be realized completely with roll-to-roll (R2R) processes. The new scheme puts emphasis on the printing part as mentioned in the project title. On the other hand, the processing of Demonstrators 1 & 2 can run in parallel to Demonstrators 3 & 4 due to different process chains and partners involved.

1.3.7 Dissemination and exploitation

During the second year of the project, the POLARIC members have organised two training events: a summer school and a workshop. In addition, the project has been presented actively in 9 scientific conferences. During 2011, one reviewed conference and one journal paper were published[1, 2]. The prolonged publishing processes and patenting related issues have slowed down the publishing of more journal papers, but many more publications are under preparation. Co-operation between other

[1] F. Zanella et al. "Towards a gm/Id design methodology for polymer-based organic thin-film transistors", Mixed Design of Integrated Circuits and Systems (MIXDES), 2011 Proceedings of the 18th International Conference, pp. 379-383, 16-18 June 2011.

[2] R. Müller et al. "High mobility short-channel p-type organic transistors with reduced gold content and completely gold-free source/drain bottom contacts", Organic Electronics, Vol. 12, Issue 7, July 2011, pp. 1227-1235.

EU projects within the field of flexible, organic and large-area electronics has been active through joint training events and a concertation meeting.

1.3.8 Management

The Steering Group is the highest decision-making body of the Consortium. It takes decisions concerning e.g. the agreements, finances, intellectual property rights, contributions, deliverables, default, and evolution of the Consortium. It is free to act on its own initiative or on Coordinator's proposal to formulate proposals and take decisions in accordance with the procedures set out in the Consortium Agreement. The Steering Group consists of one representative of each beneficiary and it meets every six months. During 2011, two steering groups meetings were kept, one in Frankfurt, Germany, and the second one in Muttenz, Switzerland.

The Technical Management Team (TMT) is the project management body responsible for the decision making regarding technical aspects within the limits set by the Description of Work (Annex I or the Grant Agreement). Thus, it is the main forum for the steering of the scientific work in the project. TMT consist of the Technical Manager (appointed by the coordinator) and the Work Package Leaders of the technical work packages. During 2010, the TMT had 14 meetings, of which 6 were teleconferences.

1.4 Summary

Regarding the main activities in 2011, following general remarks can be made:

- Dielectric material (specific formulation of x-PMMA) was selected and tested for the short channel OTFTs.
- The tool fabrication and NIL processing were developed further to introduce a NIL process step, which will pattern the full 4" area of the flexible substrate at once in a batch (or sheet) OTFT processing. Similar process development is under construction with roll-to-roll facilities in parallel with the batch process.
- Gravure printing of n- and p-type OTFTs is developed to establish large-area processing concepts for complementary organic electronic circuits.
- A complete process flow for short-channel OTFTs, incorporating the NIL step and self-align concept, has been tested. Devices have been fabricated and characterised.
- The designs of Demonstrator 1 and Test Structure 2 were updated, released and the corresponding process flow started.
- Demonstrator 1 production was started.

The deliverables are distinct and specified outcomes of the project, usually put in the form of a report. The work plan had total of 24 deliverables due in 2011. Of these, 19 deliverables were related to technical work, 3 were related to dissemination, and 2 were management deliverables. Of the total 24 deliverables due during the reporting period, 9 deliverables were submitted during 2011. The remaining deliverables are related to the delays in the fabrication process development. Despite the delays, the general target of the project to decrease the channel length of OTFTs while maintaining the compatibility with high-volume and large-area processing methods is still valid and achievable.

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