PROJECT PERIODIC REPORT

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1. Publishable summary

1.1 Introduction

To date the use of organic thin film transistors and circuits in industrial products has been limited. The main obstacle for substantial market penetration of such organic electronic components has been the inability to achieve sufficient device performance using high-volume production methods such as printing. This has delayed the commercially viable implementation of organic transistors in complex electronic circuits and system development. In response to this, the POLARIC project aims to revolutionise the way printed electronic circuits are made and simultaneously, take a major step forward in the device performance. The project partners are 3D-Micromac AG (Germany), AMO GmbH (Germany), Asulab Division of The Swatch Group R&D Ltd (Switzerland), BASF Schweiz AG (Switzerland), Cardiff University (UK), CSEM (Switzerland), Fraunhofer EMFT (Germany), IMEC (Belgium), Imperial College (UK), Joanneum Research (Austria), micro resist technology GmbH (Germany), Obducat Technologies AB (Sweden), and VTT (Finland) as the coordinator. The project is spread over the years 2010 – 2013. This document describes the project objectives, work progress, and achievement for the first project period (year 2010).

1.2 Objectives

The objective of the project is to realise high-performance organic electronic circuits using large-area processing compatible fabrication methods. The high performance of the organic circuits referred to here means high speed (kHz-MHz range), low operating voltage (below 5 V), low power consumption, and low parasitic capacitance. The organic thin film transistor (OTFT) fabrication development will be focused to enable a high resolution nanoimprinting lithography (NIL) step, which will be compatible to roll-to-roll processing environment. Applying NIL will enable smaller transistor channel lengths (below 1 μm) and thereby an increase in the performance of the device. Also complementary transistor technology will be developed, enabled by availability of both n- and p-type organic semiconducting materials. The high performance organic transistors will be tested in basic electronic building blocks such as inverters and ring oscillators. After this, more complex circuits will be used in the technology demonstrators. The main demonstrators will be active matrix liquid crystal display (AMLCD) and radio-frequency identification (RFID) tag (see Subsection 1.3.6). In addition to showing that sufficient performance can be reached without sacrificing the mass fabrication approach, solutions for the fabrication of roll-to-roll tools in order to make serial replication viable will be provided. Finally, the circuit design, modelling, and characterisation of organic electronics will be developed to offer a toolbox similar to that of silicon-based microelectronics. The presentation covers the overview of activities and latest research results in the way towards printable, organic and large-area realisation of integrated circuits.

1.3 Work progress and achievement during the first reporting period

1.3.1 Thin dielectrics for short channel OTFTs

The manufacturing of highly stable OTFTs for the project demonstrators requires a wet coating process for reliable and homogenous dielectric layers with a dry thickness down to 100 nm. During the first project year, the work started with finding initial specifications for the material selection and characterisation protocols. This was followed by initial material selection for the active matrix LCD demonstrator and their property comparison and testing. Development of process and material formulation for thin gate dielectric in a web coating process was started.

To reach highly reliable dielectric films, photo crosslinkable poly(methyl methacrylate) (x-PMMA) has been used. It is formulated by BASF and it is well known for its good film building properties. For the PMMA coating a spin cast process on 6 inch rigid substrates was developed, showing remaining thicknesses of 190 nm with high reproducibility and high homogeneity. Because of the strong interdependencies to the work package channel miniaturisation, it is essential to reach the planned film thickness of 100 nm. This should be achievable by variation of the solids content in x-PMMA formulation.

1.3.2 OTFT channel miniaturisation

Micron sized OTFTs fabricated in a large-area-compatible batch process has been achieved. Pentacene OTFTs with channel length of 2 and 5µm were fabricated with a yield higher than 90% and channel lengths down to 600 nm were demonstrated. The performance of the OTFTs were characterised by output currents of several 100 nA, reasonable saturation, mobilities of up to $1x10^{-2}$ cm^2/Vs, and good saturation. Gate leakage ($\geq$ 2nA) in conjunction with the on-off ratio ($\approx$100), subthreshold swing (some 3 V/dec), and contact resistance need to be improved.

1.3.3 Complementary OTFT technology

A set of device structures which are compatible with gravure printing and conventional processing was successfully designed for the development of laboratory scale processing towards reel-to-reel fabrication. A related device fabrication process flow compatible with fabricating all the different device layers by either gravure printing, conventional processing or combination of both techniques has been achieved. In terms of materials, high performance p-type and n-type organic semiconductors (OSCs), metal inks and dielectrics have been purchased or synthesized. Using these device structures, process flow and materials, an initial set of conventionally processed OTFTs have been successfully fabricated and tested.

1.3.4 Circuit development for organic integrated circuits

During 2010, the activities in this work package started with providing the project with a standard measurement protocol that aims to ensure reproducible measurement procedures for OTFTs. Standard protocols such as IEEE-1620™-2004 Standard Test Methods are available, but the project needed further precisions to ensure that the measurement throughout the project are done in reproducible way. The standard measurement protocol will further evolve during the project with the technical development, e.g. the voltage range will reduce with smaller channel lengths and thinner gate dielectrics layer. Parallel to this, a standard test circuit with various test structures for characterisation purposes was designed.

After several design iteration, the design for the first demonstrator, a transistor matrix comprising a 16 x 16 active matrix for LCD, was released. The design comprised of 6 different sets of chromium masks, 2 shadow masks and 1 shim. The matrix consisted of 16 different transistor channel width/length pairs varying in the range from 400 to 8400. They were organized in rows such that one row of the matrix met the expected drain current given by the specifications set to the demonstrator.

1.3.5 Manufacturing platform development

A cost-effective process chain for fabrication of up to 5”x5” Ni shims incorporating different length scale features for high throughput manufacturing was developed. These Ni shims are required in the NIL step when fabricating the short-channel OTFTs. Furthermore, a complete OTFT fabrication process flow was designed, enabling the realisation of the active matrix backplane for flexible liquid crystal displays. The transistor fabrication process comprises the self-alignment of the

transistor source-drain electrodes in respect to the gate electrode. This has important consequences in enabling large-area fabrication of patterns with small dimensions. Corresponding self-alignment processing concept has made the silicon based microelectronics fabrication as reliable and scalable as it is today.

1.3.6 Demonstrators

The project has the following demonstrators:

Demonstrator 1: OTFTs with micron spaced electrodes for AMLCD fabricated in a large-area nanoimprinting batch (6") process

- intermediate demonstrator, consists of a transistor matrix backplane (electronic part of AMLCD)
- the fabrication process for the AMLCD is demonstrated
- due in M18 (June 2011)

Demonstrator 2: Active matrix LCD

- 32 x 35 mm display
- 64 x 192 pixels, pixel size 380 µm x 140 µm
- due in M26 (February 2012)

Demonstrator 3: Large-area processed shift register

- parallel in / serial out (8 bit)
- transistor channel length below 5 µm
- due in M36 (December 2012)

Demonstrator 4: RFID tag

- 50 x 50 mm max. footprint
- 13.56 MHz, touch and pass configuration
- due in M42 (June 2013)

An artistic rendering of the vision of a flexible display.

During the first reporting period, the specifications for the active matrix display to be used in Demonstrators 1-2 were defined. To achieve this work, the constraints and the expected performances for these demonstrators were defined. These included process and material restrictions as well as dimensional, optical, and electrical specifications. Also, details for qualification tests were given. These details defined the specific targets for all the activities in the project.

1.3.7 Dissemination and exploitation

The first project year started with setting up the necessary tools for dissemination. After this, active dissemination through numerous dissemination channels was started. As a result, the POLARIC project was visible in numerous industrial and scientific magazines. The Consortium also informed the scientific community of the newly started project by active participation in scientific conferences within the field of Flexible, Organic and Large Area Electronics (FOLAE). Regarding standardisation activities, a specific standard preparation, managed in the ISO (International Organisation for Standardisation) by the Technical Committee for Ergonomics (TC 159) and Subcommittee for Ergonomics of human-system interaction, was seen as potentially relevant for the exploitation of the project foreground.

Since the first significant results were created in the laboratories during the latter half of the year 2010, detailed research results where not published in scientific journals during 2010. The next step

is to ensure that the most important research results, possessing potentiality for industrial exploitation, are patented and subsequently published.

1.3.8 Management

The Steering Group is the highest decision-making body of the Consortium. It takes decisions concerning e.g. the agreements, finances, intellectual property rights, contributions, deliverables, default, and evolution of the Consortium. It is free to act on its own initiative or on Coordinator's proposal to formulate proposals and take decisions in accordance with the procedures set out in the Consortium Agreement. The Steering Group consists of one representative of each beneficiary and it meets every six months. During 2010, two steering groups meetings were kept, one in Oulu, Finland, and the second one in London, UK.

The Technical Management Team (TMT) is the project management body responsible for the decision making regarding technical aspects within the limits set by the Description of Work (Annex I or the Grant Agreement). Thus, it is the main forum for the steering of the scientific work in the project. TMT consist of the Technical Manager (appointed by the coordinator) and the Work Package Leaders of the technical work packages. During 2010, the TMT had 9 meetings, of which 6 were teleconferences.

1.4 Summary

The work plan had total of 19 deliverables due in 2010. Of these, 12 deliverables were related to technical work, 4 were related to dissemination, and 3 were management deliverables. Regarding the main objectives for 2010, following general remarks can be made:

- specification of the AMLCD demonstrators (Demonstrators 1-2) and alignment of the individual work package targets with these specifications
- design of standard test circuits for OTFT development
- based on the AMCLD specifications protocols for dielectric material selections, testing, properties and targets, as well as web-coating process development
- design of the overall process flow for the OTFTs matrix of the Demonstrators 1-2, including the process flow for the Ni shim fabrication to be used in the NIL process
- fabrication of the first test transistors with materials and processes which are based on the Demonstrator 1-2 process flow
- finding a step-wise approach and process flow for the development of gravure printing based OTFT fabrication, in the aim of scale up towards reel-to-reel fabrication
- design of the process flow for the Demonstrators 1-2

Of the total 19 deliverables due during the reporting period, completion of 5 deliverables was delayed by more than 1 month. Despite these delayed deliverables, the project has achieved most of its objectives and technical goals set to the period, and the deviations can be considered as minor. This is because achieving the general objectives and the main demonstrators (Demonstrators 2 & 4) as planned is not endangered.

More information:

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