Community Research

PROJECT FINAL REPORT

Grant Agreement number: 247978

Project acronym: POLARIC

Project title: Printable, organic and large-area realisation of integrated circuits

Funding Scheme: CP

Period covered: from 01/01/2010 to 30/06/2014

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Executive summary

Organic electronics offer a thin, light-weight, and flexible/bendy alternative to the silicon based microchips existing nowadays all around us. One of the main benefits of using organic materials in the production of electronic devices is the possibility to use large-area fabrication technologies such as printing. Despite the promising market forecasts, the use of organic electronic circuits in today's industrial products is limited. The main obstacle for substantial market penetration of the technology has been the inability to achieve sufficient device performance using high-volume production methods. The POLARIC project, funded by the European Commission through the Framework Programme FP7, has tackled this challenge by developing the fabrication methods for the organic thin film transistors (oTFTs), which are basic building blocks of the electronic circuits. The technical approaches towards improved performance and yield included 1) high resolution nanoimprinting lithography (NIL) to downscale the critical dimensions in the transistor, 2) metal lift-off technique to realise metal electrodes with high conductivity, and 3) self-alignment principle for accurate alignment of the transistor electrode patterns in the different thin film layers to decrease the parasitic capacitances.

Extensive efforts were put in designing and developing the fabrication processes utilising the above mentioned fabrication concepts to the demonstrators. The fabrication development and eventually the realisation of the AMLCD demonstrator were carried by 8 POLARIC project partners from 6 different countries. Thus, the establishment of working fabrication platform required a significant joint effort and solving a set of practical and technical challenges. As a result of this collaboration, 22 fully processed AMLCD backplane substrates giving 88 individual flexible display backplanes with different transistor channel geometries were produced. Of these, 10 backplanes were further processed into displays, contacted, and tested. Although the developed transistor technology is still in rather immature level, the results indicated that the technology generally is capable of fulfilling the specifications demanded by the AMLCD application.

The aim for the second demonstrator in the project was to utilise TFTs with very short (below 1 μm) transistor channel lengths in the RFID front end circuitry. The front end of an RFID tag means here the load modulator, antenna capacitor, and rectifying unit. The target in this demonstrator was to use continuous roll-to-roll (R2R) fabrication techniques, enabling high throughput large-area manufacturing. Along the R2R process development it was observed that the used hot-embossing based NIL process was inapplicable for producing sub-micrometer scale TFT channels in large areas. In order to avoid a deadlock situation in the process development, and to simplify the fabrication process, NIL was replaced with flexographic printing. This enabled the R2R fabrication of working TFTs, however, with channel lengths beyond the target.

In the R2R demonstration run, a web (or roll) approximately 80 meters in length, containing more than thousand devices was produced. A TFT footprint was about 15 mm x 15 mm, and one RFID front end circuitry took an area of approximately 50 mm x 50 mm. The design margins were very conservatively selected, and the footprints can be decreased substantially. The minimum transistor channel length for the R2R fabricated TFTs in this work was tens of micorometers. Although being relatively short for a thin film transistor fabricated completely with continuous type roll-to-roll techniques, this transistor channel length is not in itself beyond the state-of-the-art. The on-currents in the TFTs remained relatively low, well below 1 μA. Also the on/off current ratios were measured to be modest, being in most cases below 10^3. However, the main success is in implementing the self-aligned fabrication concept to such TFT fabrication process on a R2R platform. This eliminates the problem of limited registration accuracy of the R2R equipment, and decreases the overlap capacitances. The achieved yield in this first demonstration was roughly 40% in average. With further fabrication development and process iterations, the yield can be improved, while the parameter spread can be decreased.

1. Project context and objectives

1.1 Introduction

Organic electronics offer a thin, light-weight, and flexible/bendy alternative to the silicon based microchips existing nowadays all around us. One of the main benefits for using organic materials in the production of electronic devices is the possibility to use large-area fabrication technologies such as printing. A transistor is a fundamental component of any electrical circuit. It is an electronic switch, which can be turned on or off by modulating the potential applied to the gate electrode, in presence of a supply voltage between the source and drain electrodes. When on, the current flows in the semiconductor material between the source and drain in an electrically conductive channel created by the gate voltage. The distance between the source and drain is defined as the transistor channel length, which determines amongst others the speed of the device. In organic electronics, a special type of transistor, a thin film transistor is used. A schematic illustration of a thin film transistor (TFT) with all of the functional layers is shown in Figure 1.

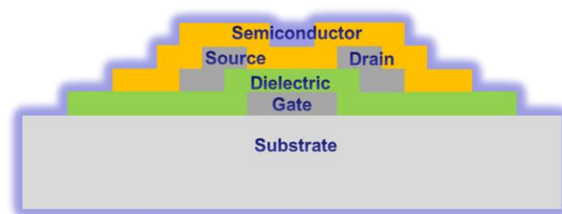

Figure 1. A schematic figure of a thin-film transistor.

Despite the promising market forecasts, the use of organic thin film transistors and circuits in today's industrial products has been limited. The main obstacle for substantial market penetration of such organic electronic components has been the inability to achieve sufficient device performance using high-volume production methods. This has delayed the commercially viable implementation of organic transistors in complex electronic circuits and system development.

To tackle the above challenge, the European Community granted funding for the POLARIC (Printable, organic and large-area realisation of integrated circuits) project consortium through the 7th Framework Programme (FP7/2007-2013), under the area of Information and Communication Technologies (ICT). The 13 organisations involved in the consortium are listed in Table 1. The project duration was from January 2010 until June 2014.

Table 1. The organisations involved in the POLARIC project.

Partner	Country	Partner	Country
3D-Micromac AG	Germany	IMEC	Belgium
AMO GmbH	Germany	Imperial College	UK
Asulab	Switzerland	Joanneum Research	Austria
BASF Schweiz AG	Switzerland	micro resist technology GmbH	Germany
Cardiff University	UK	Obducat Technologies AB	Sweden
CSEM SA	Switzerland	VTT Technical Research Centre of Finland	Finland
Fraunhofer EMFT	Germany		

The general aim for the project was to improve the performance of the organic electronics by improving the fabrication methods of the TFTs. The added goal was to further develop the fabrication towards large-area production processes, as far as possible in a R2R configuration or on large area flexible substrates in a batch process. The main numerical targets for the TFT performance indicators are listed in Table 2. The technology development was to be exploited in the flexible active matrix liquid crystal display (AMLCD) and radio-frequency identification (RFID) demonstrators, as listed in Table 3.

Table 2. The main performance targets for the TFTs on flexible substrate.

Target	Value	Target	Value
Dielectric layer thickness	< 100 nm	Charge carrier mobility	> 0.1 cm^2/Vs
Dielectric layer defect density	< 1/cm^2	Subthreshold slope	$\|S\| < 1V/dec$
Dielectric layer uniformity	> 95%	On/off current ratio	$\geq 10^4$
Dielectric layer breakdown voltage	>100 V/µm	Yield	95%* or 50%**
Transistor channel length	≤ 1 µm	Operation voltage for an organic IC	≤ 5 V
Cut-off frequency	500 kHz - 1 MHz		

* For the *AMLCD* demonstrators (Demonstrator 1 & 2, see Table 3)
** For the *RFID* demonstrators (Demonstrator 3 & 4, see Table 3)

Table 3. Demonstrators in the POLARIC project.

Demonstrators	Name	Description
Demonstrator 1	OTFTs with micron spaced electrodes for AMLCD fabricated in a large-area nanoimprinting batch (4” square) process	Flexible display backplane fabricated with the developed TFT fabrication concepts (NIL, lift-off, self-alignment)
Demonstrator 2	Active matrix LCD	A flexible display with 64 x 64 pixels, each with area of 380 µm x 380 µm (32 mm x 35 mm display) on 10 cm by 10 cm flexible substrate,
Demonstrator 3	R2R processed load modulator for RFID tag	Load modulator TFTs realised completely on R2R fabrication platform
Demonstrator 4	R2R processed antenna capacitor and rectifier for RFID tag	The load modulator, capacitors for the antenna, and rectifying unit together constitute the front end of an RFID tag. The antenna and the logic circuitry omitted.

Due to the challenging targets, it was seen necessary to develop the fabrication methods in parallel using three main *fabrication platforms*. Towards the *AMLCD* demonstrators, the *batch processing platform* was used. Here, a 10 cm by 10 cm flexible substrate was the starting point for the TFT fabrication. The *batch processing platform* utilised sheet-to-sheet type processing techniques such as photolithography in the patterning, in addition to the NIL based patterning. For the *RFID front end demonstrators* a *R2R processing platform* with web coating techniques was used. In the *R2R processing platform*, the focus was on the manufacturing techniques that offer the highest expectation for the throughput, the continuous-type roll-to-roll processing. Thus, it is not a stop-

and-go type process, which would enable the use of lithography to define small features. The batch processing enables smaller footprint of the devices, whereas R2R processing opens up the possibilities for true large-area processing. In spite of this main division, the platforms had strong interlinks and it was often necessary to mix the batch processing and printing type processing. This is especially the case with the complementary OTFT technology development in the project, in which R2R compatible *gravure printing* was used as widely as possible to produce the device layers, but with a sheet-to-sheet batch process with table-top type printing equipment. The main fabrication concepts, common to all of the fabrication platforms throughout the project, are described next.

1.2 Downscaling transistor dimensions with nanoimprint lithography

The transistor fabrication development was focused to enable a high resolution nanoimprinting lithography (NIL) step to decrease the critical dimensions of the TFT down below 1 μm. A schematic illustration of the NIL process is shown in Figure 2.

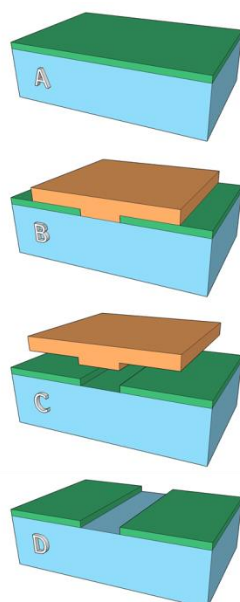

Figure 2. Nanoimprinting lithography NIL process consisting of A) resist deposition, B) imprinting step, C) release of the stamp (or shim), and D) removal of the residual resist (if necessary). Image copyright owned by VTT.

In the NIL process, very small features, with the resolution down to tens of nanometers[1], can be patterned to a thin resist film. The resist, typically monomer or polymer material designed for NIL processing, is deposited on the substrate. The substrate can be either rigid or flexible material. There are many techniques for the resist deposition, the most common being spin coating. However, in the case of roll-to-roll technology on a web substrate, spin coating is not possible, and the resist must be deposited using printing techniques. In the imprinting step, a polymer stamp or nickel shim with predefined fine features is pressed against the resist. The pattern transfer takes place after curing the resist, which is done by using either UV light or thermal process. The former is called UV-NIL, and latter thermal NIL or hot-embossing (HE). After releasing the stamp, the pattern is left in the resist.

[1]Stephen Y. Chou, Peter R. Krauss, and Preston J. Renstrom, "Imprint Lithography with 25-Nanometer Resolution", Science 5 April 1996: 85-87.

It is important to note that depending on the materials and process used, there might be a thin residual resist layer left in the imprinted area, in which case the substrate is not exposed. The residual resist can be removed with an anisotropic etching process, or avoided by modifying the materials and processes. After the proper patterns are achieved in the resist layer, it can be used as an etch or lift-off mask in the subsequent process steps.

1.3 Lift-off process to pattern high-resolution metal electrodes for TFTs

In POLARIC, the target was to use high-resolution NIL in the TFT fabrication to pattern metal gate electrodes with very small dimensions. There were two main benefits to use this approach. First, the technique allowed the gates to be made of pure metal with significantly lower resistance compared to conductive polymers or metal nanoparticles, which are commonly used alternatives for electrode materials in organic electronics. Second, the small width of the gate enables high switching speeds of the devices, particularly when parasitic capacitances are minimised by the self-alignment, as described in the next subsection.

A combination of NIL and metal lift-off can be used to pattern the gate electrodes, as shown in Figure 3. After the NIL resist deposition and imprinting step, a metal layer is evaporated all over the surface. In the lift-off step, the resist is removed and the metal is left only at the imprinted areas.

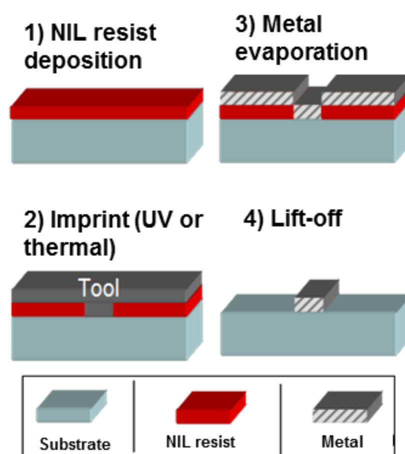

Figure 3. Combining NIL and metal lift-off in realising metal gate electrodes for TFTs with high resolution. Image copyright owned by Joanneum Research.

1.4 Self-alignment of the source/drain and gate electrodes in a TFT

The remaining TFT process can be designed in such a way that the small width achieved in the gate electrode will define also the channel length. The basic concept is shown in Figure 4. After using NIL and metal lift-off as described above, a very narrow gate with width down below 1 μm is achieved on a flexible substrate, as shown in step A in Figure 4. Next, a dielectric layer is deposited on top of the gate (Figure 4 – B). After the dielectric deposition, a positive type photoresist is deposited on top of the dielectric layer (Figure 4 – C). The resist is then exposed from the backside of the substrate using the gate in the channel area as an ideal contact-photomask (Figure 4 – D). After development of the resist, openings for the source and drain electrodes are created in an ideal alignment with the gate electrode. To realise source/drain electrodes from bulk metal, another lift-off process consisting of metal evaporation and resist removal steps is carried out (Figure 4 – F&G). The final step in this TFT fabrication approach is deposition of the semiconductor material (Figure 4 – H).

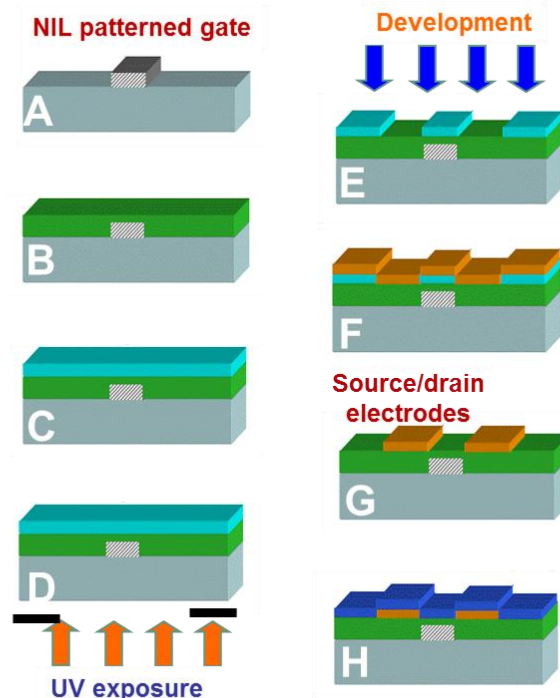

Figure 4. Self-align concept for accurate aligning of the source/drain electrodes with the gate electrodes in the TFT fabrication. Image copyright owned by Joanneum Research.

It must be noted, however, that when realising a fabrication process for an integrated circuit, where the devices are connected, further process steps must be included to the basic TFT fabrication flow shown in Figure 4. Furthermore, the selection of the processing platform to be used, as well as the targeted application have additional requirements to the final process flow. This will be seen later in the report, when the different process flows for *AMLCD* and *RFID front end* demonstrators will be described.

2. Scientific and technical results

2.1 TFT development on the batch processing platform towards AMLCD

2.1.1 Introduction

The main challenge in NIL based TFT fabrication development was that the process needed to be designed in the project without any prior preparation other than the basic concepts shown in Section 1. Thus, at the beginning of the project a considerable effort was put into designing the complete process flow, selecting the most promising technology, and identifying suitable partners for every step of the process.

In addition to the use of NIL to decrease the TFT dimensions, upscaling the process area towards large-area fabrication concepts has been one of main aspects of the project. It is essential to understand that typical area sizes in a NIL fabrication thus far had been in a millimeter scale. Thus, upscaling the processing area in NIL while reducing the feature size of the TFTs has been a remarkable challenge. First, achieving sufficiently large and high quality shims (sometimes also called stamps) to be used in the NIL process required large efforts and solving many difficult technical issues. After this, developing a wafer-scale or web-scale NIL process is another challenging step.

Therefore, although the substrate size of 4” (in a batch process) or web width of 20 cm (in a roll-to-roll process) might at a first glance not seem as a large area, for NIL processed OTFTs they certainly are. The development of the shim manufacturing process towards larger shims and the development of the NIL processing itself proved to be more challenging than the consortium anticipated during the project preparation.

As a results of the initial planning, 8 project partners from 6 different countries joined forces to establish a TFT development platform towards the AMLCD demonstrators. This Europe wide TFT fabrication platform, the project partners involved, and their respective roles are shown in Figure 5.

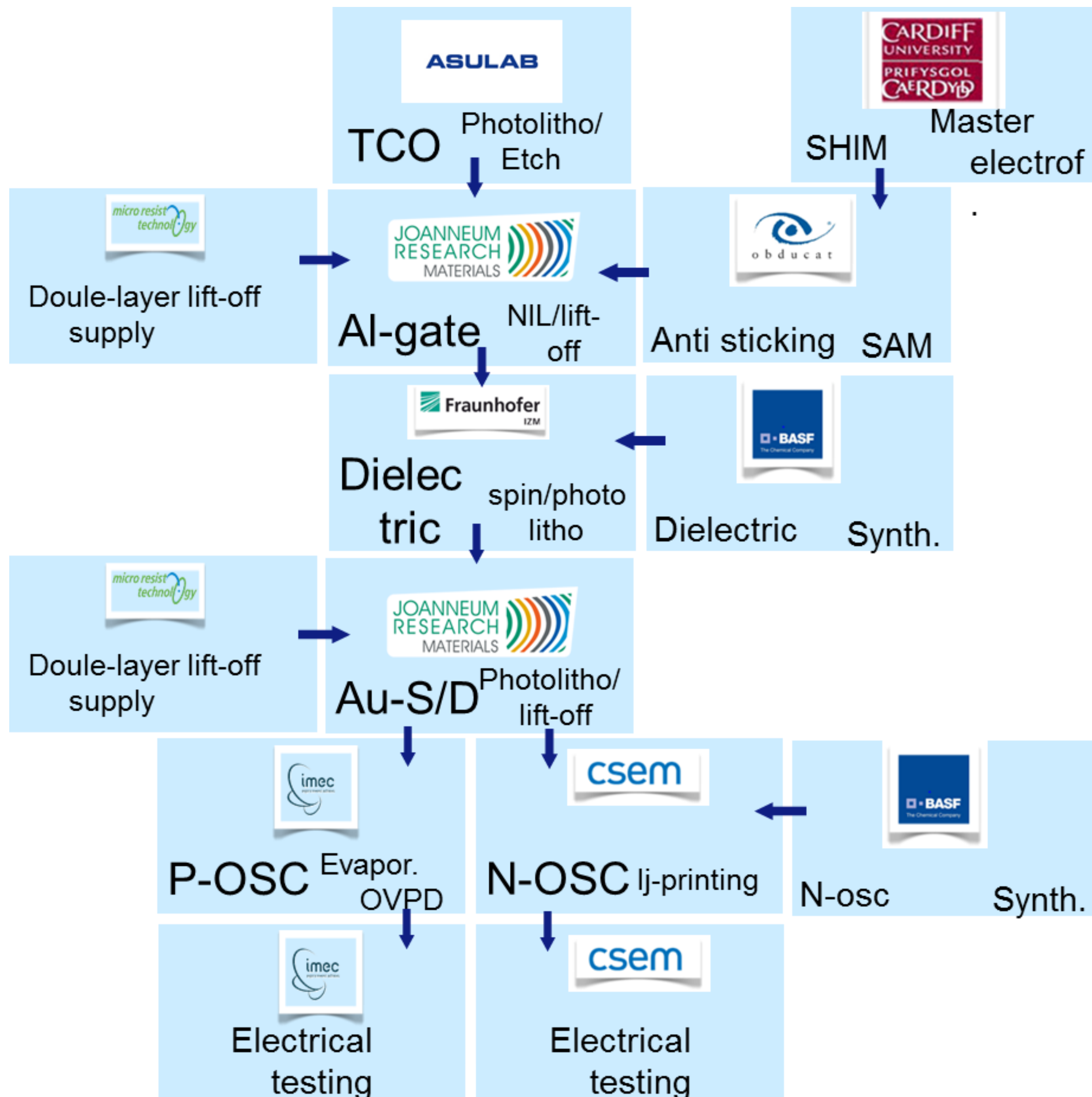

Figure 5. POLARIC project partners involved in the TFT development towards the AMLCD demonstrators. Image copyright owned by the POLARIC project consortium.

Although ensuring very active and fruitful collaboration between the partners, the collaborative approach caused also difficulties, challenges in coordination and scheduling (long total shipping time), and practical problems such as damages caused by shipping and handling in different labs. Although this did not in itself endanger meeting the targets, the implementation of the work plan was delayed significantly from the original schedule.

An overview of the developed work flow for AMLCD production and the individual process blocks are shown in Figure 6. Next, the individual process steps are described in more detail.

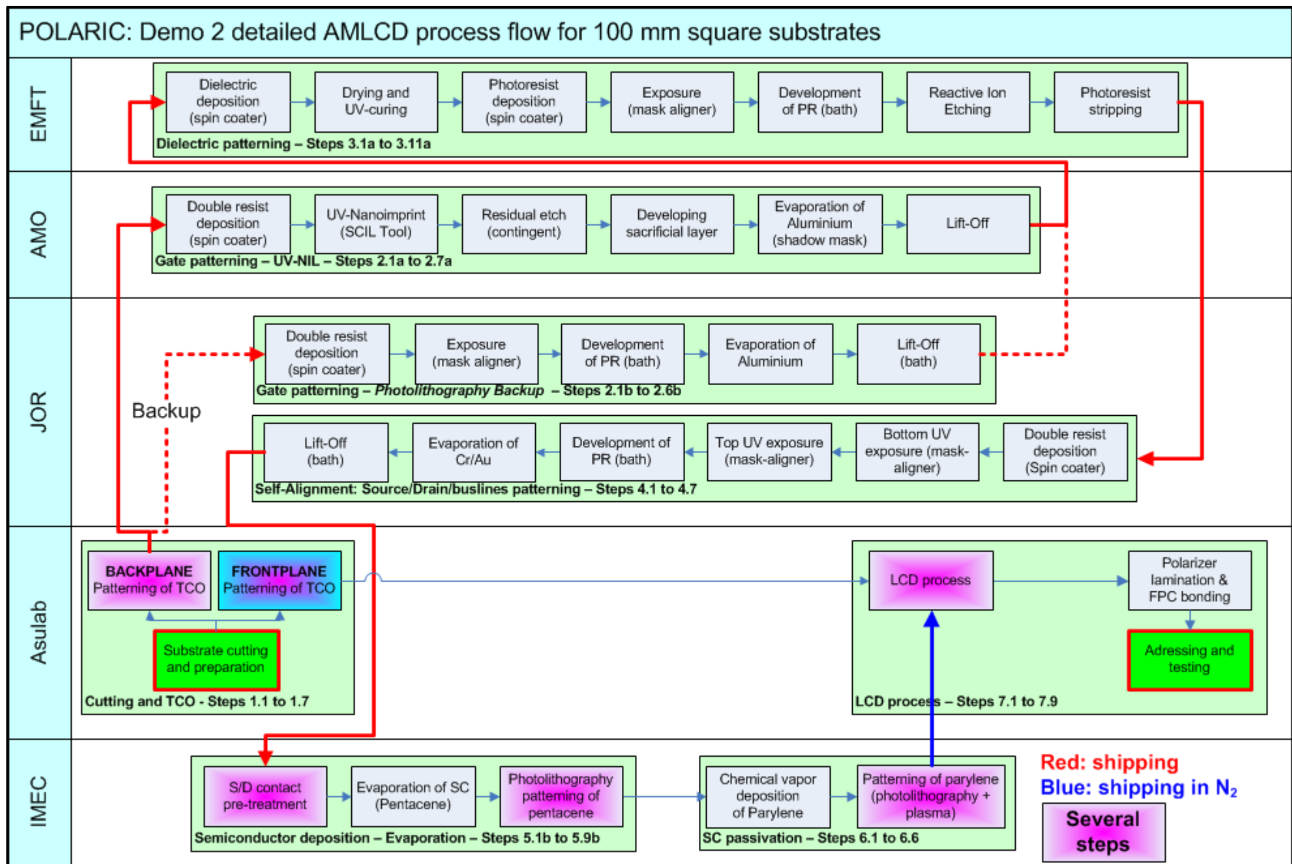

Figure 6. AMLCD demonstrator process flow. Image copyright owned by the POLARIC project consortium.

2.1.2 Substrate preparation and transparent conductive oxide (TCO) patterning

The process starts at Asulab with substrate preparation and patterning of the transparent pixel electrode. The 100 mm x 100 mm substrates are cut to size. The base is formed by a core of polycarbonate (PC) that fulfils the criteria for AMLCD application. The PC core is further enhanced by gas barriers and anti-scratch coatings. The patterning of the transparent conductive oxide (TCO) is done by a standard lithography and etching process.

2.1.3 Gate metallisation

The method of choice in the AMLCD platform for realizing very fine features in the gate metallization was UV-NIL followed by the metal lift-off, as shown in Figure 3. Aluminum was used as the gate material. During the early attempts in the lift-off step, a severe technical challenge was met when trying to disrupt the continuous metal film on top of the NIL resist. The film needed to be very thin in order to make the lift-off step possible at all, and the torn-off edges of the film formed bowed structures commonly referred to as "batman ears" (see Figure 7).

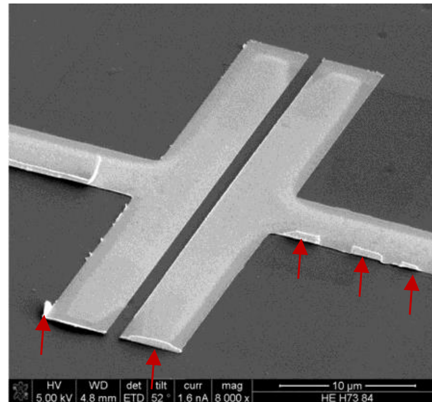

Figure 7. Bowed edges of metal layer, typically called "batman-ears", indicated by red arrows. Image copyright owned by Joanneum Research.

For having well defined metal edges without the "batman ears", several different approaches were tested in the project for the gate metallisation. Generally, these concepts can be categorized as follows:

- Special NIL stamps providing inclined side-wall for the imprinted NIL resist
- Bilayer-resist schemes while over-developing the lower resist and creating an undercut
- Avoiding the lift-off step by depositing the metal layer before the NIL step

During the implementation of the project, none of the tested NIL concepts gave convincing results with the tools and machinery available to the consortium, due to stamp related challenges, low yield, inhomogeneous pressure application, insufficient upscale to large NIL area, or alignment issues. Most of these problems were due to the somewhat outdated equipment used in the early phases of the project. For individual defect issues technical or material-related solutions have been found, but have been introduced during the very final phases of the project or are based on nanoimprint approaches outside the consortium. Thus, this project could not capitalise all of the rapid development in the NIL technology taking place in the industry.

Nevertheless, the problems with NIL based fabrication gave reason to realize some process runs using also contact photolithography in the gate patterning. The photolithography is a well-established and reliable process. The drawback is that contact photolithography cannot compete with NIL in the resolution, being limited to around 2 µm dimension. However, in this case this was not critical, since from a performance point of view sub-micron devices are not of utmost importance for the AMLCD application.

2.1.4 Dielectric deposition

A special formulation of crosslinkable polymethyl methacrylate (x-PMMA) was applied by spin-coating to be used as a dielectric gate insulator layer of the TFT. The main challenge was the demand to pattern the dielectric layer with high resolution, a requirement arising from the AMLCD application. Because of this, the material was developed to be photopatternable, to transfer the x-PMMA dielectric from liquid state into a rigid material by UV exposure. This gave a possibility to a subtractive patterning process with a relatively low number of steps as can be seen in Figure 8. A final flood exposure with higher intensity is used for optimized cross-linking of the x-PMMA.

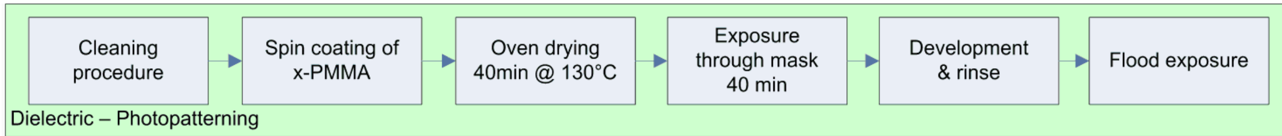

Figure 8: Process steps of dielectric formation by photopatterning. Image copyright owned by the POLARIC project consortium.

While giving sufficient pattern resolution on silicon wafers, the photopatterning appeared to be difficult on the transparent PC foils. The features were relatively well reproduced but the edges are widely broadened (width up to 20 µm), probably caused by light scattering effects. To achieve a higher resolution while keeping the optimized PMMA material, a standard photolithography step in combination with plasma etching was used for the AMLCD demonstrator production. The x-PMMA was processed in the same manner as before but cured by flood exposure instead of using a mask. Also the developing step was still used to remove the very thin not cross linked layer from the top of the x-PMMA which is due to oxygen inhibition.

This combination of UV x-linking and plasma etching gave very good pattern resolution below 5 µm (see Figure 9) but resulted in more process steps, as shown in Figure 10.

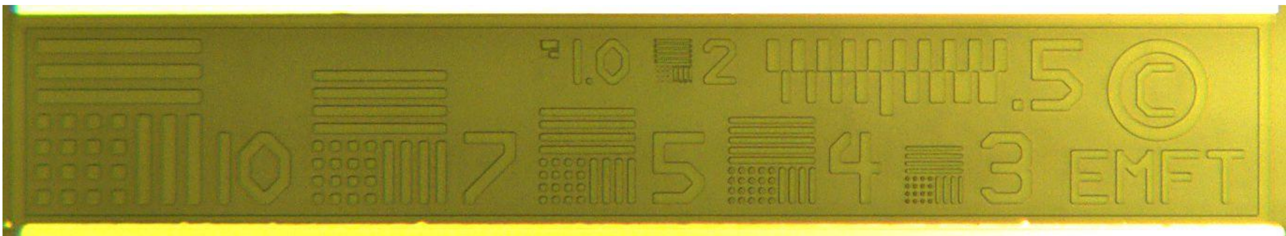

Figure 9: Dielectric resolution feature realized by photolithography and plasma etching. Numbers correspond to line and gap widths. Image copyright owned by the POLARIC project consortium.

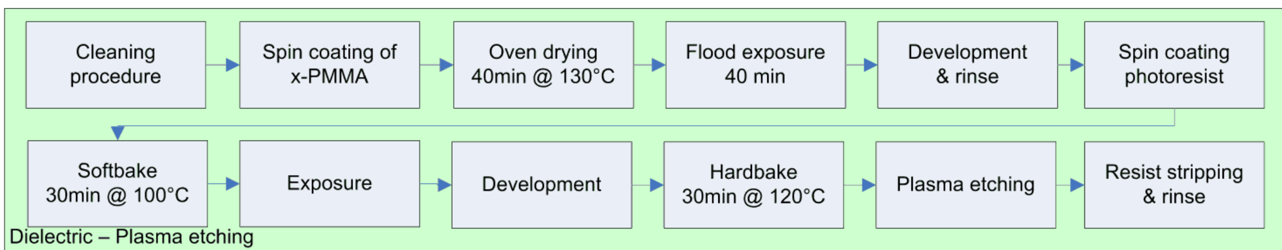

Figure 10: Process steps of dielectric formation by plasma etching. Image copyright owned by the POLARIC project consortium.

The electrical measurements for the x-PMMA formulation were done on capacitors with varying dielectric thicknesses and electrode sizes. The leakage current and capacity measurements scaled with electrode size and varied with dielectric thickness in good agreement to the theoretical calculations. Based on the experiments the relative dielectric permittivity for the material (ε_r) was 3.8, the dielectric field strength was estimated to be well above 1 MV/cm, and the layer uniformity was better than 95%.

2.1.5 Source, drain, and busline formation

In the second metallization layer Au was used to form the source and drain electrodes as well as the buslines. As aluminum, gold has high conductivity and ductility. Furthermore, it does not oxidize and gives typically a good contact to the semiconductor material. The adhesion is however insufficient on most surfaces and demands an additional adhesion promoter, a very thin layer of chrome in this process.

As described earlier, the self-aligned process was used in the formation of the source/drain metallisation. The beauty of this process is that it enables the realization of very fine and well aligned features in combination with a very small overlap of the gate and source/drain layer. This is a significant improvement compared to standard lithography approaches where an overlap in the region of 3-5 µm needs to be kept even on rigid glass substrates. Especially in the AMLCD this is a big advantage since the parasitic gate-drain capacitance leads to voltage shifts during the active-matrix addressing. These level shifts which can in state-of-the-art technologies easily be in the range of 10-20% of the applied data voltage need to be compensated by other means (additional storage capacitor, more sophisticated addressing signals) in order not to deteriorate the displayed image. Additionally, the temperature and moisture related dimensional changes of the plastic substrate can be compensated much better with the self-alignment concept.

The main challenges of the process were the poor quality of the edges of the metal patterns ("batman ears") and the particles originating from the lift-off step. However, the self-alignment itself worked very well. The overlap between source/drain and gate electrodes determining the parasitic capacitance was measured to be less than 200 nm.

2.1.6 Semiconductor deposition

Two types of semiconductor processes were tested in parallel on the TFT development platform towards the AMLCD demonstrator. The more forward-looking approach was the ink-jet printing of an n-type polymer semiconductor developed within the consortium. The more state-of-the-art process was p-type pentacene evaporated in a R2R compatible OVPD process.

Inkjet printed n-type semiconductor

Inkjet printing is seldom promoted for mass production due to its limited throughput. For the semiconductor deposition in the active matrix it is however a viable route since only the TFT channels need to be coated. Also for the process development it is more cost-saving than other printing techniques like gravure or flexography where much larger quantities of the costly semiconductor material are needed.

The additive nature of the pattern generation leads to a lean process (see Figure 11). Besides cleaning and pre-conditioning steps that are very important for a good metal-semiconductor and dielectric-semiconductor interface, there is only the printing and an additional drying step.

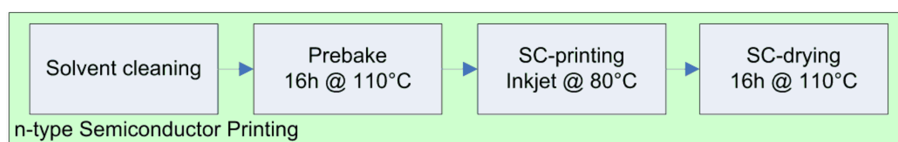

Figure 11: Process steps of n-type semiconductor inkjet printing. Image copyright owned by the POLARIC consortium.

After problems with exact ink placements in the first runs, the wetting behavior of the ink was improved and additional heating of the substrate table during printing led to visually stable printing

results (see Figure 12). For the Demonstrator 1 the semiconductor droplets were well placed. They covered the channel region while not covering buslines or pixel electrodes. However, for the Demonstrator 2 with more demanding dimensional requirements, the placement accuracy of the inkjet system was not sufficient anymore. For the final design of Demonstrator 2 the pixel size was reduced by a factor of 4 and the semiconductor island needed to be deposited in a thin line along the busline while not contacting neighbouring pixel electrodes or buslines. Because of this, the final AMLCD demonstrator was realized using pentacene as the semiconductor material.

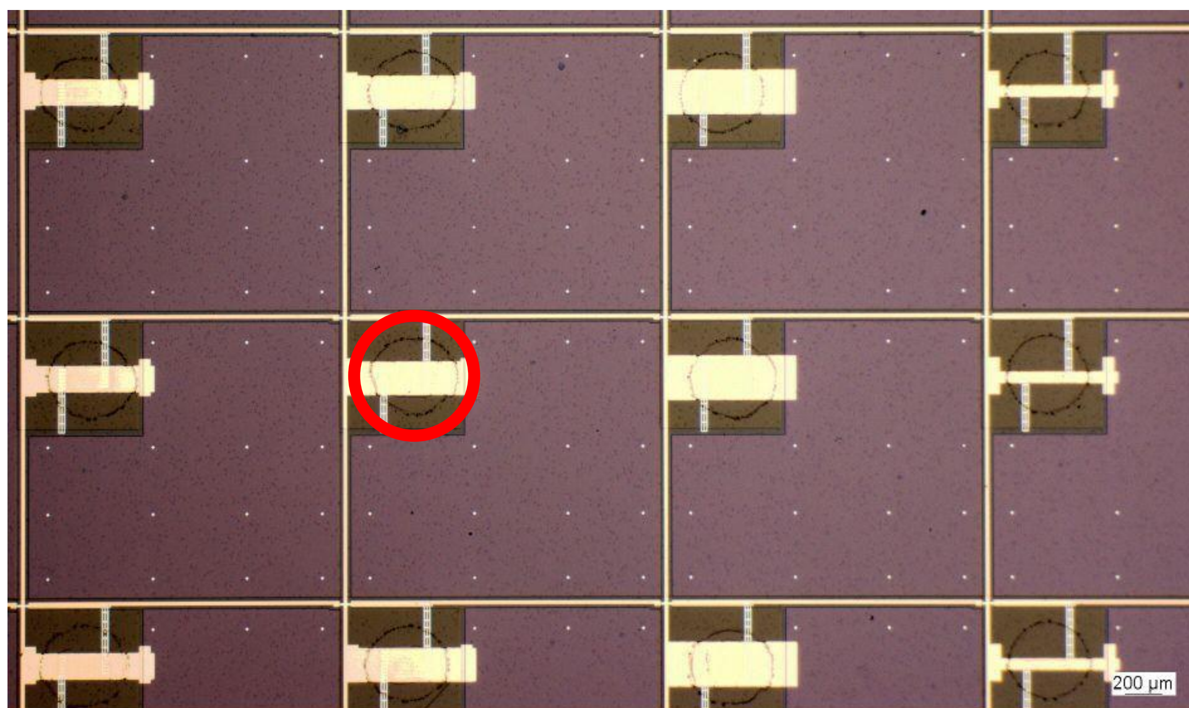

Figure 12: Inkjet printed semiconductor droplets in active-matrix. One of them is indicated a by red circle. Scale bar corresponds to 200 µm. Image copyright owned by Asulab.

Evaporated p-type semiconductor

The evaporation of the small molecule p-type semiconductor is a well-established process. Usually, the contacts are cleaned in isopropanol (IPA) with some sonication. The cleaning by UV-ozone treatment was also tested as possible alternative. This was done since organic contaminations were presumed to be on the Au source/drain contacts.

After a surface pre-treatment by dipping into a thiol solution a poly(alpha-methylstyrene) (PaMS) layer was applied by spin-coating. Both materials should give self-assembled monolayers selectively formed on the Au contacts due to their surface chemistry. Their purpose was to improve the charge carrier injection into the semiconductor.

The semiconductor can be evaporated through a shadow mask or it can be patterned afterwards with a photolithographic process. The shadow mask process was strongly limited in pattern resolution (above 50 µm) and alignment accuracy (above 500 µm). Photolithography allows alignment accuracies in the range of 5 µm and pattern resolutions down to some 10 µm. It increases however drastically the complexity and costs as becomes obvious from Figure 13. Also the additionally involved chemicals and etching steps might deteriorate other layers.

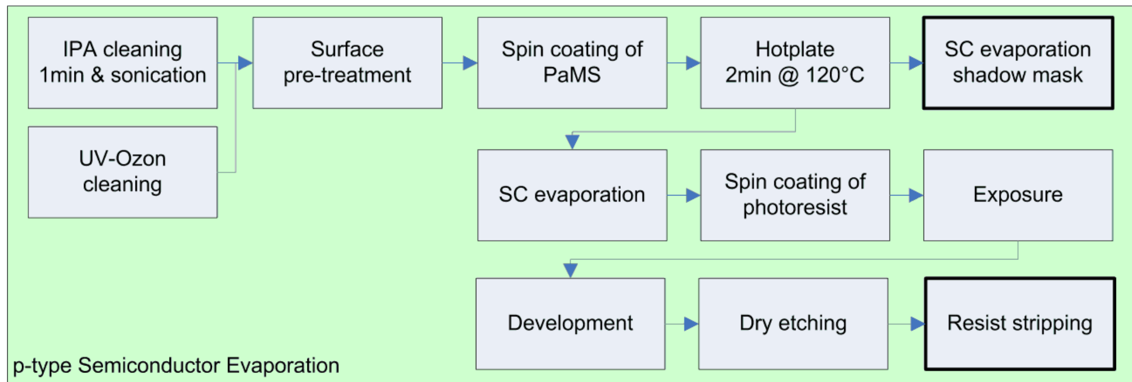

Figure 13: Process steps of p-type semiconductor evaporation and patterning. Image copyright owned by the POLARIC consortium.

2.1.7 Passivation of the semiconductor layer

The passivation acts as a protective layer for the organic semiconductor. It also serves as stable interface for the later LCD formation. A dimer of di-para-xylylene was vaporized at low pressure and the corresponding *p*-xylylene intermediate polymerizes when physisorbed on the substrate's surface. This method is scalable to large areas at least in the sheet-to-sheet type batch processing.

Trials of using a shadow mask did not work sufficiently since the vapor goes under the mask. The patterning was eventually done by photolithography and plasma etching which increases the efforts drastically and involves additional plasma etching and resist stripping (see Figure 14).

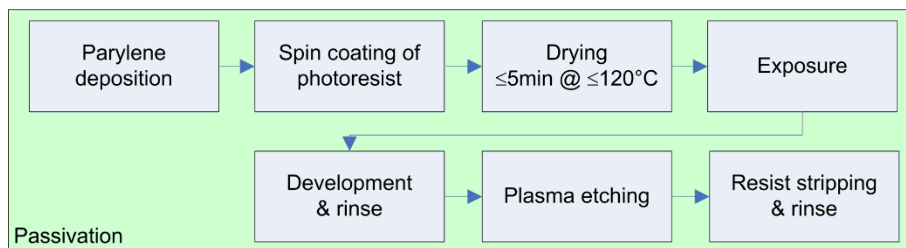

Figure 14: Process steps of parylene passivation layer deposition and patterning. Image copyright owned by the POLARIC consortium.

2.1.8 Liquid crystal display fabrication

All the process blocks presented so far only concern the control electronics backplane to direct addressing of the individual pixels of one gate line while not influencing the content of the other pixels of the AMLCD. The complete display consists however of the backplane and a frontplane with a liquid crystal layer. The frontplane has an additional TCO layer serving as counter electrode for the electrical driving of the liquid crystal molecules. For achieving the desired electro-optical effect, an orientation layer is needed both on front and backplane. The processing of front- and backplanes can be done in parallel and does not increase the complexity of the production.

The LC cells were realized by applying spacers in the micrometer range between the front- and backplane for a well-defined LC cell thickness and assembling both substrates with the help of a printed cell frame. The cell gap was filled with a suitable liquid crystal mixture. The realized displays use the so called twisted nematic (TN) mode.

The displays were finalized by cutting the individual displays from the batch and laminating polarizing films to both sides of the display. After bonding of flexible printed circuit boards to the external contacts the AMLCDs were tested. Figure 15 shows a complete display module with bonded FPCs and polarizing filters.

Figure 15: Display module with bonded FPCs and crossed polarizing filters. Image copyright owned by Asulab.

2.1.9 Summary of the main results related to the AMLCD demonstration

The first complete TFT process runs with above described fabrication steps showed very weak yield. The approach taken was to carry out as many complete process runs as possible and improve with every run. During the TFT process development towards the AMLCD, more than 10 process runs were initiated. During these runs, weak points were identified and improvements were done to the following runs. Due to the need for constant development, none of the process runs were identical. This allowed improving the technology, but made it difficult to compare the achieved results.

Table 4 lists the key specifications and parameters, achievements, and deviations in respect to the expected results for the AMLCD demonstrator. The results are derived from the large data set of over 800 TFTs measured during the project. To highlight the focus of the project – the downscaling of the TFT channel length – the short channel TFTs ($L \leq 1$ µm) are compared with conventional TFTs ($L > 1$ µm), all sharing the same processing platform as far as possible. This allows a direct comparison of the studied high resolution NIL patterning concept with more robust photolithography patterning in the TFT fabrication. To compare the studied technology with the targets set to the work, it was analysed which portion of the TFTs exceeded a given target specification.

Table 4. Comparison of the targets set for the AMLCD TFTs and the achieved results.

Specification	Target	Result
Transistor channel length (L)	≤ 1 µm	≤ 1 µm at minimum
Cut-off frequency	500 kHz - 1 MHz	Stage delay of 4 µs for a ring-oscillator Maximum cut-off for an inverter 115 kHz TFT transit frequency > 10 MHz*

Charge carrier mobility (in saturation)	$> 0.1\ cm^2/Vs$	Achieved with 30 % of the TFTs, when $L \leq 1\ \mu m$ Achieved with 3 % of the TFTs, when $L > 1\ \mu m$
Subthreshold slope	$\|S\| < 1V/dec$	Achieved with 32 % of the TFTs, when $L \leq 1\ \mu m$ Achieved with 64 % of the TFTs, when $L > 1\ \mu m$
On/off current ratio	$\geq 10^4$	Achieved with 33 % of the TFTs, when $L \leq 1\ \mu m$ Achieved with 64 % of the TFTs, when $L > 1\ \mu m$
Yield in AMLCD operation (based on the target levels of the on and off currents)	95%	Achieved with 10 % of the TFTs, when $L \leq 1\ \mu m$ Achieved with 25 % of the TFTs, when $L > 1\ \mu m$

[*]Estimation given in F. Zanella, “Organic Thin-Film Transistors: from Technologies to Circuits”, PhD, Ecole Polytechnique Fédérale de Lausanne (EPFL), 2014.

Concluding the results it can readily be seen that the targets were not well met. Furthermore, none of the measured TFTs fulfilled all the specifications set to the charge-carrier mobility, subthreshold slope, on/current ratio, and the targeted AMLCD current levels. This is mainly related to the low maturity level of the process. Also the collaborative approach involving several laboratories with long distances separating them might have had an effect to the results. However, the best samples indicated that the developed technology generally is capable of fulfilling the specifications demanded by the AMLCD application. Especially the realization on freestanding flexible plastic substrate with self-aligned source/drain TFT electrodes allows a unique display technology.

From the best samples it can be concluded that TFT channels with lengths down to the sub-micrometre regime were patterned with UV-NIL in the batch processing platform on 10 cm by 10 cm flexible substrates. Thin polymer dielectrics with thickness down below 100 nm were employed in order to maintain low operation voltages of 10 V. The overlap lengths between source-drain and gate electrodes as low as 0.2 µm were achieved by self-aligned electrode definition using back-substrate exposure. Pentacene based organic thin film transistors with a low line edge roughness of channels, mobilities of the order of 0.1 cm^2/Vs, low contact resistance, and an on-off ratio of 10^4 were fabricated . To demonstrate the speed of the TFTs, a ring-oscillator with an average stage delay below 4 µs at an operation voltage of 7.5 V was also demonstrated.

2.2 TFT processing on the roll-to-roll processing platform towards RFID

2.2.1 Introduction

The basic target for the RFID demonstrator was to utilise thin film transistors with very short (below 1 µm) channel lengths in the *front end circuitry* of an RFID tag. The expression *front end* of and RFID tag means here the load modulator TFTs, antenna capacitors, and the rectifying circuit. Thus, the antenna itself, and the logic circuitry have been omitted. The aim was to realise the fabrication process completely by using only roll-to-roll (R2R) fabrication techniques. To achieve the short transistor channel lengths on R2R fabrication platform, hot-embossing based nanoimprint lithography (HE-NIL) was to be used in the process to pattern the critical features. The final important concept to be exploited was the self-aligned fabrication principle in the similar way as in the TFTs towards the AMLCD application.

During the implementation of the NIL process in the patterning of the TFT gate electrodes on the R2R processing platform, difficult technical challenges were met. The main reasons for the NIL based gate defects on R2R which eventually could not be overcome were particle contamination, low substrate quality (scratches), uneven NIL resist layer, inadequate resist flow during the R2R hot-embossing, and inability to come up with a sufficient process window in the residual resist plasma etching, all leading to inadequate transistor channel formation. These problems reflect to the fact that R2R-NIL is quite a new technology for the fabrication of metal structures with submicron dimensions on large area flexible substrates. An example of this is that the commercialisation of the roller tools – required by the R2R-NIL process – started during the run of the project and there are still only very few roller tools available on the market. Thus, all roller tools which were available for the consortium were specially customized for the needs of the project.

As a response to the deadlock situation in the process development, it was eventually decided to replace the NIL processing by flexography printing and lift-off in the gate electrode structuring. After this decision, the overall process flow for the R2R demonstrators was redesigned. The main parts of the process flow can be seen in Figure 16. As seen in the figure, there are 11 main fabrication steps in the process, ignoring some minor steps such as drying and reeling for the sake of clarity. Including also the minor process steps, the process flow included 22 steps. This meant that the number of process steps was reduced from the unsuccessful NIL based process flow, which had 28 fabrication steps in total. The changes influenced the reliability of the process favourably. The drawback was that the minimum resolution, determined by the flexography printing, was now tens of micrometers, in comparison to the theoretical submicrometer resolution of NIL.

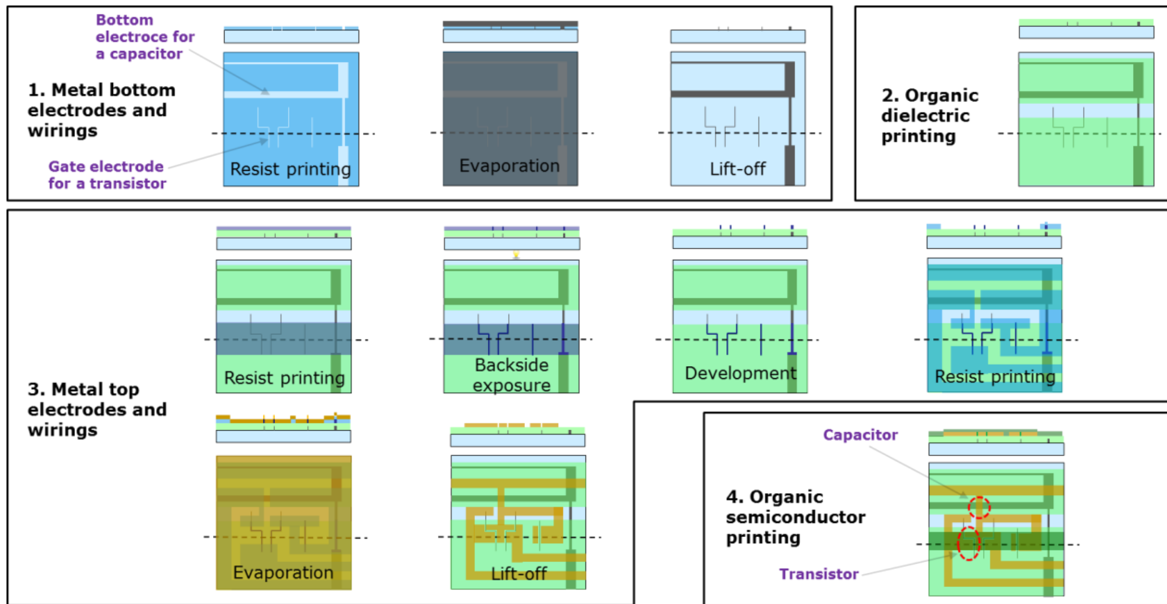

Figure 16. Redesigned roll-to-roll process flow for the RFID front end demonstrators. Image copyright owned by VTT.

2.2.2 Bottom level metallisation

Gate electrodes were fabricated using flexography printing, metal evaporation, and lift-off. In the transistor gate design, the centre parts of the gate electrodes were aligned to the direction of printing (machine direction or MD) and end areas leading to contact points were aligned perpendicularly to direction of printing (cross machine direction or X-MD). This had an important implication since in flexography printing, on contrary to the previously tested HE-NIL patterning, resulting features are affected by their geometrical orientation in printing cylinder.

Due to the unsummetrical behavior of the flexography printing, the minimum achievable dimensions are different for machine direction and cross machine direction. Since the transistor gate structure, defining the channel area, had sections to both orientations, the transistors in the final R2R demonstrator did not have a single uniform channel length. To clarify this, the channel geometry of the transistor diodes is presented in Figure 17 and channel dimensions in Table 5. From the table it can be seen, that the minimum channel length was 25 µm, but these transistors had also two channel sections of 73 µm in length.

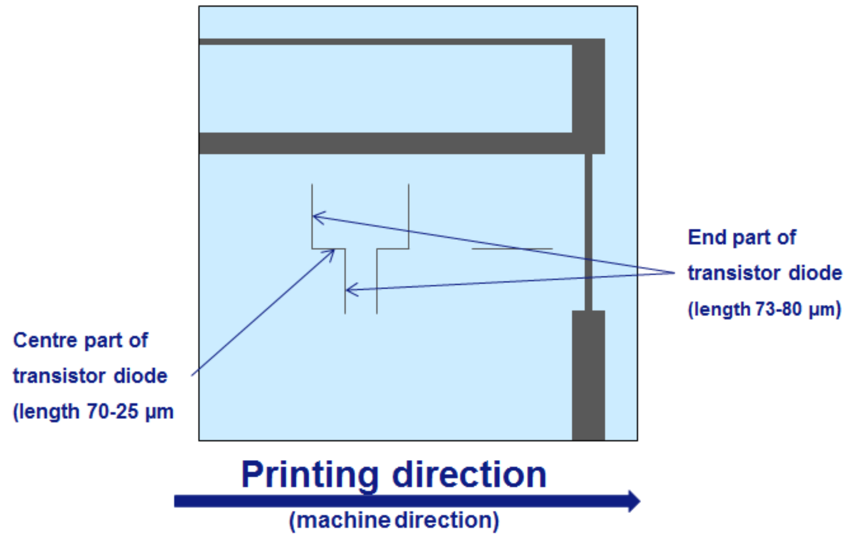

Figure 17. Channel geometry in Demonstrator 4. Image copyright owned by VTT.

Table 5. Channel dimension of the transistor diodes. MD refers to machine (printing) direction and X-MD refers to cross machine (printing) direction.

Area	Device	Channel lenght (MD)(µm)	Channel width (MD)(µm)	Channel lenght (X-MD)(µm)	Channel width (X-MD)(µm)	Channel lenght avg.(µm)	Channel width total	W/L ratio
Quarter 1	TFT diode 1	80	9910	70	3970	77	13880	180
Quarter 1	TFT diode 2	80	9906	70	3960	77	13866	180
Quarter 2	TFT diode 1	75	9940	50	4000	68	13940	206
Quarter 2	TFT diode 2	80	9910	45	3990	70	13900	199
Quarter 3	TFT diode 1	80	9900	35	3990	67	13890	207
Quarter 3	TFT diode 2	80	10070	35	4000	67	14070	209
Quarter 4	TFT diode 1	73	9921	25	3990	59	13911	235
Quarter 4	TFT diode 2	73	9990	25	4000	59	13990	236

Also the electrodes for the capacitors were made with flexography printing and Ag metal evaporation in the same process step as the electrodes of the TFTs. Capacitor areas and dimensions are presented in Figure 18 and in Table 6.

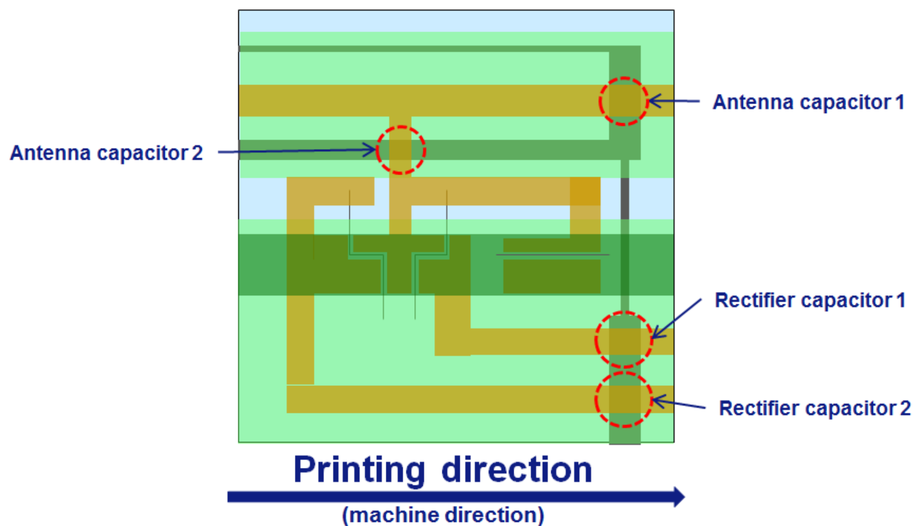

Figure 18. Capacitors used in the RFID front end circuitry. Image copyright owned by VTT.

Table 6. Dimensions of the capacitors.

Area	Device	lenght (µm)	width (µm)	Area (mm2)
Quarter 1	Antenna capasitor 1	4954	62	0,31
Quarter 1	Antenna capasitor 2	1020	899	0,92
Quarter 1	Rectifier capasitor 1	2007	4879	9,79
Quarter 1	Rectifier capasitor 2	2017	4864	9,81
Quarter 2	Antenna capasitor 1	4990	79	0,39
Quarter 2	Antenna capasitor 2	1030	926	0,95
Quarter 2	Rectifier capasitor 1	1966	4917	9,67
Quarter 2	Rectifier capasitor 2	1961	4888	9,59
Quarter 3	Antenna capasitor 1	4949	65	0,32
Quarter 3	Antenna capasitor 2	1029	904	0,93
Quarter 3	Rectifier capasitor 1	2002	4882	9,77
Quarter 3	Rectifier capasitor 2	2007	4857	9,75
Quarter 4	Antenna capasitor 1	4959	85	0,42
Quarter 4	Antenna capasitor 2	1019	917	0,93
Quarter 4	Rectifier capasitor 1	1961	4904	9,62
Quarter 4	Rectifier capasitor 2	1962	4885	9,58

2.2.3 Printing of the dielectric layer

The dielectric was printed with reverse gravure using PMMA insulator tailored in the project. The thickness of the dried printed layer varied between 800 nm and 1200 nm. Printed dielectric is shown in Figure 19.

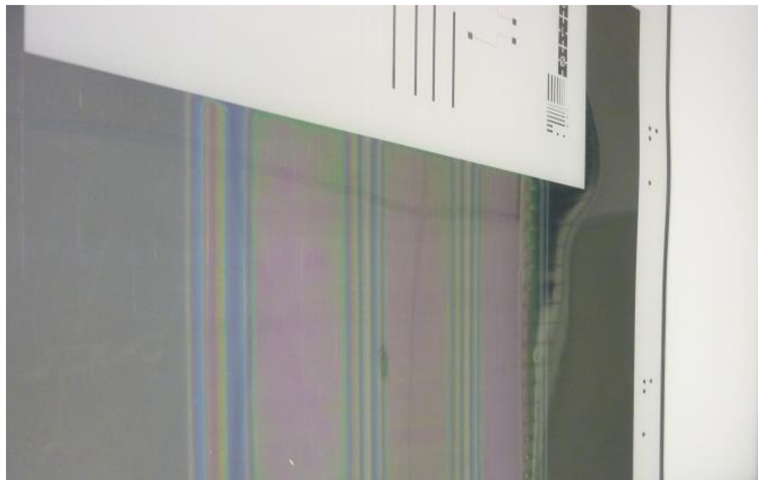

Figure 19. Dielectric on top of bottom electrodes printed with reverse gravure. Image copyright owned by VTT.

2.2.4 Fabrication of the top electrodes

The top electrodes including wiring, source/drain electrodes, and top electrodes of the capacitors where made at the same time including:

- Photoresist printing with flexography for defining the channel area (self-alignment concept)
- Exposure from the back side of the substrate with UV and development in potassium hydroxide for defining the self-aligned channels
- Black ink flexography printing for defining the wirings, top electrodes of the capacitors, and TFT source/drain electrodes
- Ag evaporation
- Lift-off to remove the unwanted metal areas, completing wiring, top electrodes of the capacitors, and source/drain electrodes

Process steps are presented below in Figure 20.

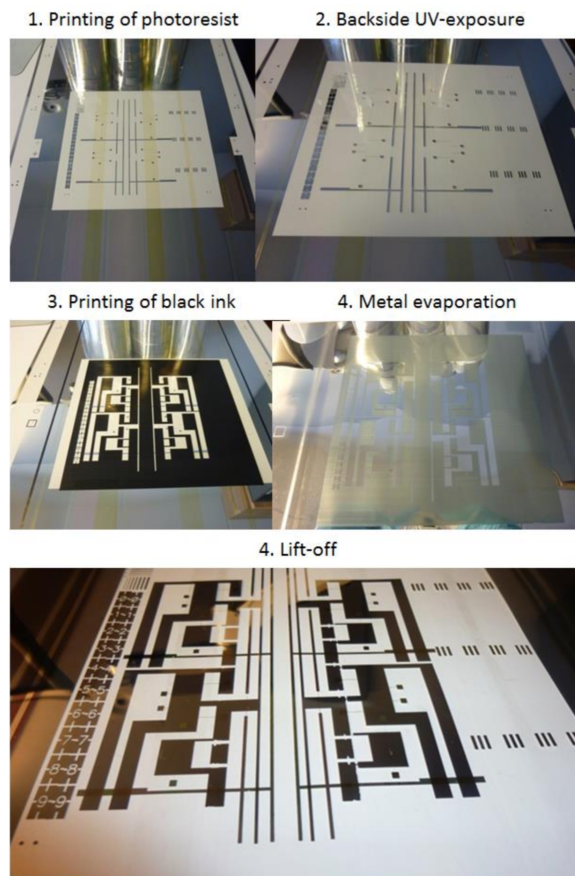

Figure 20. Process steps involved in formation of wiring, source/drain electrodes, and top electrodes of the capacitors. Image copyright owned by VTT.

2.2.5 Printing of the semiconductor layer

Deposition of the semiconductor done with reverse gravure printing was the final step of the roll-to-roll process. An image from the completed devices is shown below in Figure 21.

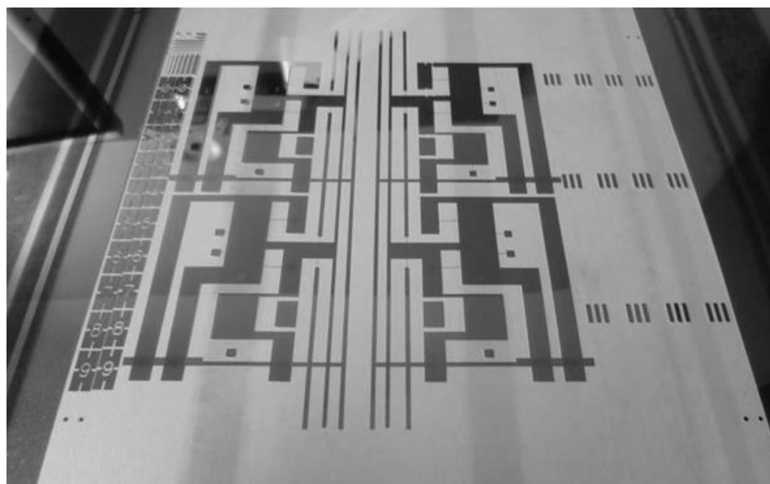

Figure 21. Final R2R fabricated TFT circuits for the RFID demonstration. Image copyright owned by VTT.

2.2.6 Summary of the main results related to the RFID demonstration

Table 7 lists the key specifications and parameters, achievements, and deviations in respect to the expected results for the roll-to-roll fabricated RFID front end demonstrator. The results are derived from the R2R demonstration run, in which a web (or roll) being approximately 80 meters in length, and containing more that thousand devices was produced.

Table 7. Comparison of the specifications given in DoW for the Demonstrator 3 and the achieved results.

Specification	DoW	Result
Transistor channel length:	1 µm	25 µm at minimum*
W/L ratio	12,500	~ 200
Ion (transistor on-current)	10 µA	< 1 µA
Ion/Ioff (current on/off ratio)	>1,000	Achieved with less than 50% of the TFTs
Operation frequency	13.56 MHz	Not achieved
Substrate roll width	200 mm	300 mm
Max footprint	70 mm x 70 mm	TFT footprint ca. 15 mm x 15 mm Circuit footprint ca. 50 mm x 50 mm
Yield (share of devices showing transistor operation)	50 %	~ 40 %

* The channel length was not uniform along the width of the TFT channel due to different orientations effecting the resolution in the flexography printing.

Consolidating these results it can readily be concluded that the targets set in the work plan were not met. This was mainly due to the unsuccessful implementation of the NIL processing steps in the TFT fabrication, which caused the unsuccessful realisation of the short-channel transistors on R2R platform. Decreasing the TFT dimensions, especially the channel length, was one of the most important general objectives, also on the roll-to-roll fabrication platform. The minimum transistor channel length for the R2R fabricated TFTs in this work was 25 µm. However, it must be noted that this channel length was not constant due to the different orientations having an effect on the printing resolution. Although being relatively short for a thin film transistor fabricated completely with continuous type roll-to-roll techniques, this transistor channel length is not in itself beyond the state-of-the-art.

The main success in the RFID front end demonstration was in implementing the self-aligned fabrication concept to such TFT fabrication process on a R2R platform. This eliminates the problem of limited registration accuracy of the R2R equipment, and decreases the overlap capacitances. The achieved yield, based on the share of the devices showing transistor operation, was roughly 40 %. This is relatively close to the target of 50 % set to the first process run. With further fabrication development and process iterations, the yield can be improved, while the parameter spread can be decreased.

2.3 Other main results

2.3.1 Modelling of the self-aligned NIL based sub-micrometer pentacene-based organic thin-film transistors

The devices developed and characterised were used to select a model based on the "TFT Generic Charge Drift model" which works well for a broad range of channel lengths including the submicron TFTs. It was shown that these TFTs can be accurately modelled, thus giving access to complex circuit simulations and design. The results were published in *Organic Electronics* journal[2].

This dedicated static model was then updated to account for the subthreshold regime and was used to simulate a zero-V_{GS} inverter (one of the most basic unipolar logic gate). Based on the extracted noise margins, two methodologies were studied to assess the potential of the studied TFT technology in terms of p-logic digital circuits. The different analysis showed that these TFTs, in the current state of the technology, are still not ready for complex digital circuits as the throughput is expected to be quite low. The proposed methodology and related interpretation are technology-independent. Therefore, this analysis may serve as a basis to characterize unipolar-logic printed electronics and can be further extended to complementary-logic circuits. These results were published in *IEEE Transactions on Electron Devices* journal[3].

2.3.2 Complementary OTFT technology

In order to decrease operating voltage and power consumption, and increase noise margins, n- and p-type OTFTs and organic complementary circuits were developed in the project. The n- and p-type OTFT components consisted of short-channel UV-NIL or conventionally photolithography patterned gates, thin organic photo-patterned or printed dielectric, self-aligned source and drain, and gravure printed semiconductors. Circuits were developed on plastic substrates using materials available within the POLARIC consortium. Complementary inverters and NAND gates were successfully fabricated and their DC and AC response were tested.

For complementary inverters based on short-channel UV-NIL gates, printed dielectric, self-aligned source and drain, and gravure printed semiconductors, optimal device behaviour at low operational biases of V_{dd} = +9 V, giving a high inverter gain of G = 28, was achieved. The more robust process flow of short-channel conventionally patterned gates (L = 3 μm), photo-patterned dielectric, self-aligned source and drain, and gravure printed semiconductors was found to achieve the necessary yield and highly uniform behaviour for multiple working circuit elements. Inverter (NOT gates) had a 40 μs stage delay, and NAND logic gates could be operated at frequencies > 5 kHz at an operating bias of V_{dd} = +20V.

[2] F. Zanella et al., "Design and modeling of self-aligned nano-imprinted sub-micrometer pentacene-based organic thin-film transistors", Organic Electronics 14 (2013) 2756–2761.

[3] F. Zanella et al. "Submicrometer Organic Thin-Film Transistors: Technology Assessment Through Noise Margin Analysis of Inverters", IEEE Transactions on Electron Devices, 61 (2014) 1508-1514.

2.3.3 Nanogravure as a method to pattern submicron scale gates for TFTs

Using special printing clichés developed in the project, doctorblade-less discontinuous dewetting as a method to fill ink cells was demonstrated for the nanogravure printing. Using this method, a range of liquid polymers and high boiling point solvents were printed onto the surface of a flexible substrate. This included micron and sub-micron lines, circles, dots, arrays of dots, and numbers. Finally, the nanogravure printed PMF etch resist process was used to pattern a sub-micron wide Au wire on the flexible PC substrates. This enables the use of the method e.g. in patterning of the gates for short channel transistors, when combined with the other process steps used in the project for TFT fabrication.

3. Impacts, dissemination, and exploitation

3.1 Impacts

The European Commission set general expectations for the impacts of the projects to be funded in the original FP7 call (Objective ICT-2009.3.3: Flexible, Organic and Large Area Electronics). In the POLARIC project proposal, the expected impacts from the project were reflected to these EC expectations as given in Table 8. In the table, the expected impacts are updated to reflect the view at the end of the project.

Table 8. Comparison of the expected impacts of the project .

Expected impact listed in the call	Expected impacts listed in the project proposal	Expected impacts at the project end
Reinforced leadership position of Europe in the creation of flexible or large area electronics tailored to meet key societal and economic needs.	POLARIC will strengthen the European leadership in the basic building blocks and large-area processing technology for organic and flexible electronics, which will enable growth of economics and have an impact on areas such as mobility, environment, food, health, and energy by offering thin, light-weight, flexible and environmentally friendly applications.	During the project, an extensive amount of expertise and new knowledge was created on materials, processes, devices, and modelling for the flexible and large-area electronics. The experiences gained from the project will reinforce the European capabilities in this technology.
Sustainable electronic device performance and manufacturing costs matching low capital investment requirements and new market opportunities.	Addressing device and circuit performance of organic and flexible electronics and combining this with parallel development of low-cost fabrication techniques, POLARIC will enable a broad range of new low-cost applications. The strongest impact will be in packaging and display sectors. However, offering essential electronic building blocks and platforms, the impact is expected to cover areas such as sensors, solar cells, batteries, lighting and especially combination of these.	The targeted device and circuit performance was not demonstrated during the project, but the activity was an important step for further development. By improving the maturity of the technology and applying it to further application demonstrators will guarantee new market opportunities.
Contribution to the evolution of traditional industries in the EU, such as printing and clothing industries, towards the e-media revolution.	POLARIC will fill the gap between traditional paper and printing industry products and ICT/electronics industry products and aim to applications like disposable sensors, simple ”electronic" components and circuits on large areas, large area functional paper-like products, smart packages, tag and code technologies for ICT and hybrid media applications.	The experiences gained from the limitations and opportunities of the organic electronics technology forms a good basis for planning the next steps with the traditional industries in the EU, for which the consortium members have wide networks.

3.2 Dissemination activities

3.2.1 Publications

Dissemination of the project results has been active, and the whole consortium has taken part in it. Table 9 summarises the number of expected publications in the project for the whole duration of the project.

Table 9. Journal and conference publications in the POLARIC project.

Type of dissemination	Number of publications
Journal papers	16 + 3 (submitted) + 12 (to be submitted)
Conference papers	10
Talks at conferences	40
Posters at conferences	19
Demos at conferences	1
Press releases	2
News articles	18
Book chapters	1

The scientific journal papers and conference proceedings describe the key scientific findings and new knowledge created in the project. These publications and presentations, covering 14 scientific journals and 47 different industrial, scientific, or training events, dealt with practically all aspects studied in the project. However, the following main topics can be identified from the titles of the publications:

- Fabrication of self-aligned, sub-micron thin film transistors (TFT) on flexible substrate with nanoimprint lithography (NIL)
- Materials for NIL processes to be used for short-channel TFTs on flexible substrate
- Material and tooling aspects for upscaling the processing area in the NIL based production
- Modeling of sub-micron thin film transistors on flexible substrate
- Pentacene transistors on flexible substrate
- Roll-to-roll fabrication of thin film transistors

3.2.2 Workshops and summer schools

POLARIC / COSMIC Workshop 2010: Organic Complementary Devices and Circuits

This workshop was held on 22-23 September 2010 at Imperial College London, UK. It was targeted at new researchers in this field and covered all aspects of organic field effect transistors, both unipolar and complementary. For the purpose of this training event, the POLARIC project consortium joined up with the COSMIC project consortium, the other large integrated project funded by the same EC funding call in this research area.

Subjects and speakers were:

- High mobility solution processed p- & n- channel OFETs by Thomas Anthopoulos (Imperial College London) (Invited Tutorial Presentation - 90 minutes)
- Sheet-to-sheet printed High Mobility Organic Complementary Devices and Circuit by Romain Gwoziecki (CEA LITEN DTNM LCI) (Contributed Presentation – 30 minutes)
- Improving organic transistor building blocks by technology and design by Jan Genoe (IMEC) (Invited Tutorial Presentation - 90 minutes)
- Bringing Organic Electronics to the Roll by Gerhard Klink (Fraunhofer EMFT) (Invited Presentation - 60 minutes)
- Dielectrics for OFETs by Joachim Steinke (Imperial College of Science) (Invited Tutorial Presentation - 90 minutes)
- p- & n- type OSCs for OFETs by Martin Heeney (Imperial College London & Flexink) (Invited Tutorial Presentation - 60 minutes)
- Organic ambipolar transistors and circuits by Adrian von Mühlenen (CSEM) (Invited Tutorial Presentation - 60 minutes)

In addition there were a number of poster presentations covering areas such as gravure printing, organic field effect transistors and fabricating and measuring of organic complementary inverters. The poster session was held in the same room as the lunch and tea and coffee breaks.

The total number of attendees was 52. Attendees travelled from throughout the UK and Europe.

Within the POLARIC and COSMIC consortia, 28 researchers from Imperial College London, 3D-micromac, Fraunhofer EMFT, Obducat Technologies, IMEC, Joanneum Research Forschungsgesellschaft, CEA-LITEN, University of Cardiff, BASF Switzerland, The Swatch Group R&D Ltd - Division Asulab, AMO, VTT, CSEM, Eindhoven University of Technology and Flexink attended the event.

Outside the consortia, from academia 16 new researchers from the Universities of Oxford, Manchester, Surrey and Kingston, and Imperial College London (non-POLARIC) attended the event. From industry, 8 researchers from Plastic Logic and Merck attended the event.

Figure 22. Presentation session by Gerhard Klink (Fraunhofer EMFT) at the POLARIC/COSMIC Workshop 2010: Organic Complementary Devices and Circuits.

Printed Electronics and Foil Assembly 2011

In 2011 the POLARIC summer school and workshop was titled “Printed Electronics and Foil Assembly” and held at Fraunhofer EMFT, on 7-10 June, 2011, in Munich, Germany. The event was targeted at new researcher on the field of organic electronics and covered a wide range of the area. Secondary target was to disseminate information among parallel EU projects, thus the collaboration in organising the event with COSMIC, Inter Flex and Smart EC. The event covered a workshop part with 19 presentations and a summer school part with 7 different sessions/topics.

Figure 23. Presentation session by Zbigniew Szamel (CSEM) at Printed Electronics and Foil Assembly 2011.

There were a total of 40 attendees in the summer school/workshop from all around Europe. Out of these, 23 attendees were from research institutes, 10 from universities, and 7 from companies. 39 attendees participated to the workshop and 16 attendees took part in the summer school courses.

POLARIC session Multi Material and Micro Manufacturing conference (4M 2011)

A special session dedicated for the POLARIC project was organised at the 4M conference, which was held on 8-10 November 2011 in Stuttgart. The conference was targeted at researchers in the micro manufacturing field. The POLARIC special session covered selected aspects of micro and nano manufacturing for organic electronic applications.

More than 110 persons have attended the 4M 2011 conference. The POLARIC special session covered the following topics:

- Master tool fabrication for the replication of micro and nano features (Hassan Hirshy, Cardiff University, United Kingdom)
- High Volume Nanoimprint Lithography: application area organic electronics (Torbjörn Eriksson, Obducat Technologies, Sweden)
- Towards roll-to-roll manufacturing: Organic thin film transistors based on Nanoimprint lithography technique (Teemu Ruotsalainen, VTT, Finland)
- Process chain development for the realization of embedded capacitors using polymer-based nanocomposites filled with bimodal barium titanate (T. Hanemann, KIT, Germany)

Figure 24. Audience at the POLARIC session as a part of 4M 2011 conference.

3.3 Standardisation activities

During the course of the project, standardisation activities of interest to the project were identified and followed. In this context, the most important international standardisation activity turned out to be the IEC Technical Committee 119 – Printed Electronics.

The International Electrotechnical Commission (IEC) is the world's leading organization that prepares and publishes International Standards for all electrical, electronic and related technologies. Technical Committee 119: Printed Electronics was established September 2011 with a scope of standardization of terminology, materials, processes, equipment, products and health/safety/environment in the field of printed electronics. TC 119 has currently (August 2014) 12 participating member countries and 8 observer countries. The work in TC119 is currently organized to 5 official Working Groups, 2 Ad-hoc groups, and TC119 Advisory Group. The Working Groups are following: WP1 – Terminology, WP2 – Materials, WP3 – Equipment, WP4 – Printability, and WP5 – Quality assessment. The Ad-hoc groups are Ad-hoc Group 7 – Printed Products and Ad-hoc Group 8 – Roadmap.

From the POLARIC project partners, VTT is actively participating in international standardisation work as one action to promote the industrialization of printed electronics. Dr. Kari Rönkä from VTT is currently a member of the IEC SK 91 Electronics assembly technology national committee in Finnish electro-technical standardisation association SESKO which covers also activities in TC119. Dr. Rönkä has been a participant in the IEC 119 Technical Committee meetings as a head of Finnish delegation and he is member of the WG2, WG3, WG4 and TC119 Advisory Group. At VTT, he has updated the POLARIC coordinator Kimmo Solehmainen on the progress in TC119, who has then been able to inform the consortium about this important standardisation activity of printed electronics.

3.4 Collaboration

The POLARIC project had close collaboration with the COSMIC project, which was another large integrated project funded in the same FP7 call as POLARIC. The main motivation for this came from the strong links and shared objectives between the projects, both aiming for the development of organic electronics, but from different angles. The practical collaboration was focused in organising shared events, which was well justified for the purposes of sharing information, as well as not competing for the attendees or speakers. In organising the events, there was also collaboration with Inter Flex and Smart E-C, both of which were other FP7 projects in the area of flexible, organic, and large-area electronics. The POLARIC consortium had also an opportunity to closely follow the progress in the EU FP7 NoE project FLEXNET (www.noe-flexnet.eu), where the consortium members VTT and CSEM were represented. The collaboration covered also the EU CSA project 4M2020, which is focused on building upon the durable integration mechanisms/structures and innovative chains in the field of multifunctional miniaturised products and their applications in energy, medical, optoelectronics and micro optics, printed electronics and ultra precision engineering,

The POLARIC project was presented at the Organic and Large Area Electronics (OLAE) Cluster meetings on 14 –15 June 2010 in Brussels (Belgium), 13 July 2011 in Thessaloniki (Greece), and 8 October 2012 in Dresden (Germany).

3.5 Exploitation of the results

The exploitation of the POLARIC results within and outside of the consortium is based on the business plans and strategic goals of the individual partners, with the following focus:

- For the industrial partners, the exploitation is directly linked to their products and offerings.
- The research organisations focus on the technology development which will give new research and commercialisation opportunities in public and private sectors.
- In addition to the research opportunities, the universities utilise the results in the teaching and training activities.

The exploitation plans within the consortium were updated during the spring 2014. In this context, a preliminary business plan for roll-to-roll based thin film transistors technology was established. It covered the industry background, business description, market size for the different applications, potential customers and business model, production cost analysis, cost drivers, cost down scenarios, business environment analysis (PESTE – Political, Economical, Social, Technological and Environmental), SWOT analysis, and the roadmap for the commercialisation.

3.5.1 Preliminary business plan for roll-to-roll based thin film transistors

Industry background

Transistor is a basic building block in electronics, to be used as an electrical switch, amplifier, or a memory element. The production of these devices takes currently place in large semiconductor factories, which produce a huge amount of components in small silicon chips. The conventional electronic production is very capital intensive, investments in to the processing equipment and manufacturing facilities accounting for most of the manufacturing costs. Even though the transistors produced on the silicon chips have revolutionized the world, they do not naturally fit for every electronic application. Challenging applications in this sense are especially new emerging products, which require transistors over a large area. Large-are flexible displays, electronics for sensor systems, and memory elements for various purposes (smart cards, tickets, toys, games) are some examples of those.

Business description and greater investment needs

For the emerging products where the conventional silicon based electronics is not an optimal solution, thin film transistors fabricated by using material additive roll-to-roll techniques offers a competitive technology approach. This manufacturing technology offers benefits such a low-cost large-area manufacturing concept, mechanically flexible and light products, durability against mechanical shock. Furthermore, the roll-to-roll production does not require as large investments to the processing equipment and manufacturing facilities as the conventional electronic production. A production facility investment to manufacture silicon chips typically costs about $2 billion, whereas for printed chips it will be about $10 million. This can open the doors for more developers and exciting innovations rather than the industry being confined to a few high-end companies. Also, the changes in the production, allowing agile product changes, are cheaper to implement compared to the conventional electronics. All these benefits form a good basis for new products enabled by this disruptive technology.

Market size

In VTT's business database, there are about 700 companies in the world who include transistors in their business. The total turnover for these companies, calculated from the last available figures, was $224 billion. The same data base listed 31 companies with thin film transistors in their business, with the total turnover of $19 million. If the thin film transistor chip production is estimated to form 10% of the business for these companies, the current market size for the thin film transistor technology provider can be estimated as about $2 million. This is roughly in line with the market analysis provided by IDTechEx, giving a market size of $3 million in 2013 for printed and thin film transistors[4]. The same IDTechEx report states that the printed and thin film transistor circuits will become a $180 million market in 10 years, showing a similar market growth as silicon chip market experienced during 1978-1998.

The main potential applications for the roll-to-roll fabricated transistors developed in this project are identified to be the flexible displays, sensors, and memories. From the total printed electronics market, about 80% is covered by the display and lighting applications. Sensor applications cover currently about 5%, but according to Frost & Sullivan, they have a potential for a significant growth[5]. For memory elements, the key differentiation to conventional electronics will not be the cost per bit, but rather enabling electronic functionality where intelligence has not been possible or economically viable before. As the technology will be developed further, the memory applications are expected to increase from its current 1% share of printed electronics market.

Potential customers and business model

Since the aim for the POLARIC project is not a product development or final commercialisation phase, the commercialisation route for the technology has not been fixed. However, some considerations for the business development routes or potential customers for the technology can be given. The first option is that a new company, purely focusing on electronic chip production will be established. This new company should find its customers from the end application producers, such as display providers, smart tag providers, or companies operating in packaging, logistics, or security business. Another option is that the new company tries to establish a portfolio of end products,

[4] "Printed and Thin Film Transistors (TFT) and Memory 2013-2023: Forecasts, Technologies, Players", by Peter Harrop and Raghu Das, IDTechEx, 2013.

[5] "Global Printed Electronics Market—Analyzing the True Potential", Frost & Sullivan analysis NB8A-28, Nov. 2012.

providing e.g. smart objects for service business. A third option is that the technology is licensed to an existing company, boosting its business with the help of the developed technology.

The insufficient maturity of the roll-to-roll fabricated transistor technology developed within the POLARIC project hinders the possibilities for wide commercialisation. Example of a current business case is a technology developer to sell its technical expertise for the product development elsewhere in the value chain. Thus, a material provider for organic/flexible electronics might order a contract research project from the RTD organisation to test the new material in the developed transistor fabrication platform. Alternatively, a company interested in the applications might want to order a contract research project to test the viability of the TFT technology in some specific application. However, further development actions are required before wider commercialisation routes given above can be specified. The key action point here is the continued collaboration within the whole value chain – material providers, manufacturing equipment providers, component/system developers, and end users – to develop the technology to a sufficient maturity level.

Production cost analysis

To assess the production costs for the roll-to-roll production of the thin film transistors, it was first necessary to make some basic assumptions for the analysis. In the project there were two R2R based demonstrators, being 1) load modulator (Demonstrator 3) and 2) antenna capacitor and rectifier unit (Demonstrator 4) to be used for in the front end of the RFID tag. Since the antenna and logic circuitry were not realised, the R2R demonstrators did not complete an stand-alone end product such as RFID tag. However, based on the information gained during the course of the project, one can derive some basic assumptions for a real end product, which could be achievable for the current technology and which could be basis for the analysis.

For the analysis, it was assumed that the end product was a flexible chip with a moderate complexity of a few hundred transistors. This level of complexity is comparable to that of an RFID tag. The minimum chip area for this using our current R2R process flow was estimated to be about 5 cm times 5 cm, containing the transistors, wiring, registration margins etc.

Further assumptions for the production details necessary for the cost estimation were determined. The equipment related values were based on VTT's R2R pilot lines. Here, it must be kept in mind that the equipment is used in research and pre-commercial pilot manufacturing studies, and therefore the parameters do not necessarily match with those of the real commercial production. The material costs were estimated based on the R2R process flow developed in the project. Finally, the fixed costs not related to the direct material cost were assumed. For this, costs for investments, labour, facilities, energy, tooling, and maintenance were estimated.

The main results of the production costs analysis are shown in the form of a pie diagram in Figure 25. The analysis shows that the material costs dominate the cost-of-production, being 72% for production volume of 5 million pieces. Since the material costs are heavily dominated by the semiconductor material with about 85% contribution of the total material costs, it is necessary to cut down the prices and/or quantity used of this critical material in order to guarantee the competitiveness of the technology.

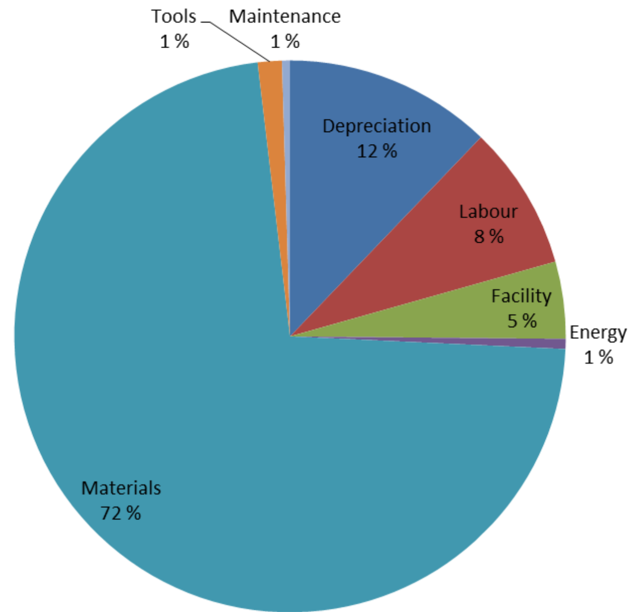

Figure 25. Share of the different cost items in the cost-of-production analysis for an annual production of 5 million flexible chips fabricated with the current R2R fabrication technology.

The main cost drivers for the roll-to-roll fabricated transistors are the materials costs, technological evolution of the materials, fabrication equipment as well as processes, and the ability to take full potential of the large-area throughput capability. The most important of the cost drivers is the production volume, as seen in Figure 26. With low production volumes below 100,000 pieces annually, the total production costs per piece are very high and dominated by the fixed costs. To be economically viable, the production volumes need to be upscaled to hundreds of thousands or millions in order to minimise the contribution of fixed costs. In this regime, the materials costs dominate the production costs, and the business viability is determined by the need in the markets for the components.

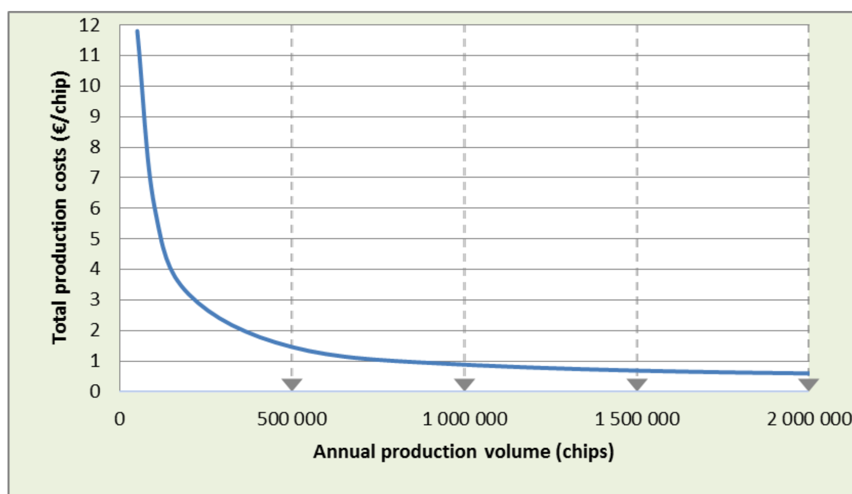

Figure 26. The relation of total production costs to production volume.

SWOT analysis

Based on the technology, environmental, and business environment assessments, a SWOT analysis (Strengths, Weaknesses, Opportunities, Threats) was made. The summary of the assessment is given in Table 10).

Table 10. SWOT analysis results.

<table>
<tr><td>Strengths
• Free form factor (thin & flexible)
• Large area processing
• Scalable production (high throughput possible)
• Lightweight
• Durability against mechanical shock
• Temperature of processing (low)
• Low environmental impact
• Hybrid integration possible</td><td>Weaknesses
• Technology maturity not sufficient at the moment (performance limited)
➢ complicated processes for current roll-to-roll mass volume processing equipment
➢ limited performance of the functional materials
• The reduction of material costs still to be done
• Standardisation incomplete
• Limited funding in Europe vs. Asia</td></tr>
<tr><td>Opportunities
• New products enabled by disruptive technology
• Low cost large area processing
• Integration to other printed functionalities
• Small investment need
• Agile production
• Expanding market
• Fast development</td><td>Threats
• Conventional electronics as a moving target – a valid commercialisation route is demanding
• Acceptance of new electronics
• Lack of application developers
• Competition with numerous technology developers world wide</td></tr>
</table>

Roadmap for the commercialisation

To present a plan for the future steps in roll-to-roll transistor technology development, a technology roadmap for 6 years was created. The roadmap is presented in Figure 27.

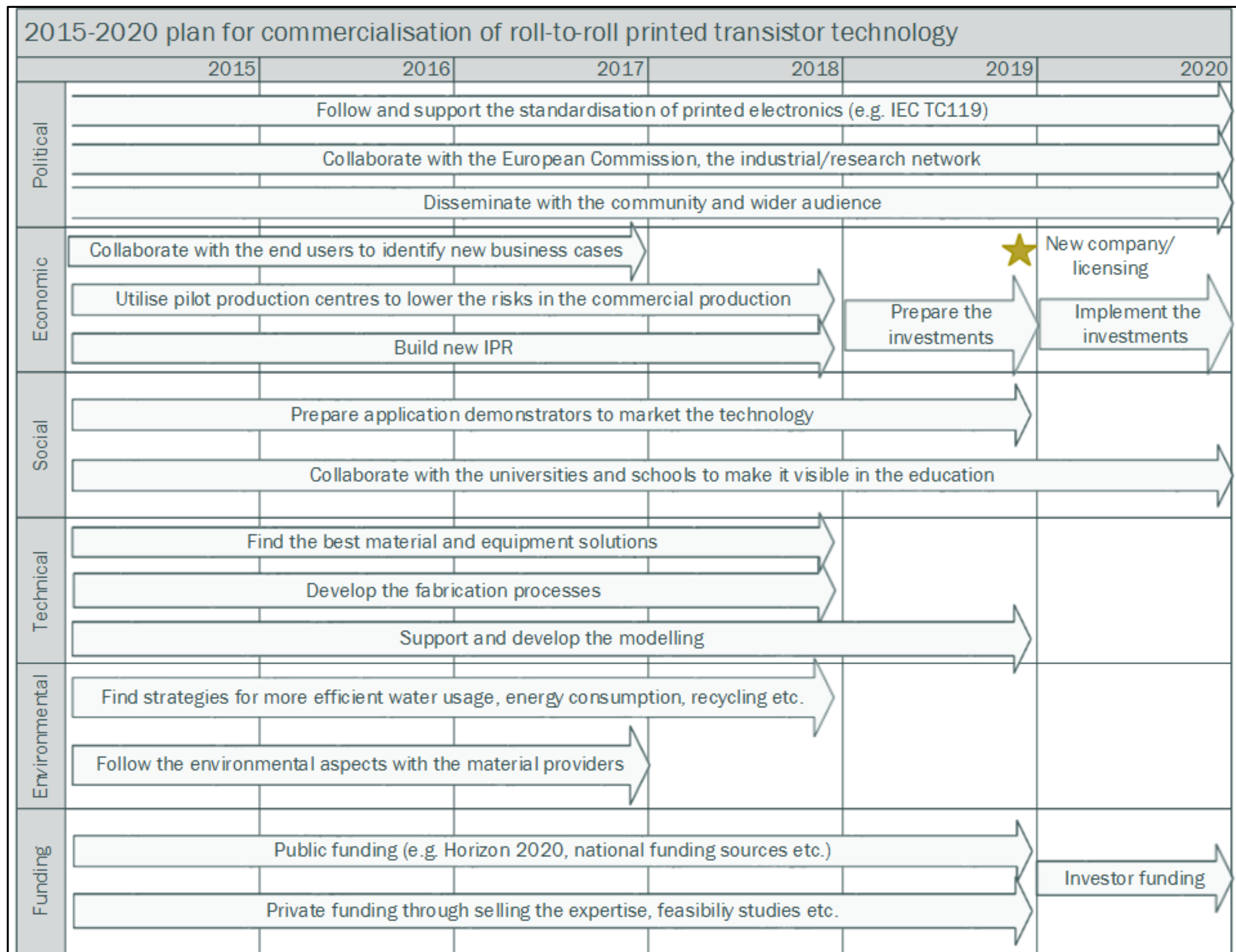

Figure 27. Roadmap for the roll-to-roll transistor technology for the next 6 years.

3.5.2 Future prospects

For the purpose of continuing the work towards the important targets of the POLARIC project, connections to a CSA project called 4M2020 were established (http://www.4m2020.eu/). The main aim of 4M2020 is to help the EU to leverage the results of past projects and to identify trends and hot topics which might be relevant for future funding in H2020. The scope covers publically funded projects in the area of multifunctional miniaturised products and their applications. The 4M2020 project is currently in the process of identifying key projects that have been funded by the FP7 programme, and assessing the key application areas, and their main findings. The POLARIC project has been identified relevant to these aims. The POLARIC consortium, with VTT as the intermediary organisation, will study if the 4M2020 activity will be suitable for advancing some of the themes studied in the POLARIC project.

The FP7 Cooperation/ICT project POLARIC

- **FPT theme:** FP7-ICT-2009-4
- **FP7 call:** Challenge 3 - Components, systems, engineering, Objective ICT-2009.3.3: Flexible, Organic and Large Area Electronics in ICT call 4
- **Grant Agreement number:** 247978
- **Budget:** Total costs 13.8 M€, EC contribution 9.9 M€
- **Project duration:** 1.1.2010 – 30.6.2014

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List of abbreviations

µC-P	Micro-contact printing
ACMO	Acryloyl morpholine
AMLCD	Active matrix liquid crystal display
DoW	Description of Work - Annex I (or "Technical Annex") of the Grant Agreement
FIB	Focused ion beam
HE	Hot-embossing (same as thermal NIL or T-NIL)
LCD	Liquid crystal display
NIL	Nanoimprinting lithography
OSC	Organic semiconductor
OTFT	Organic thin film transistor
R2R	Reel-to-reel (or roll-to-roll)
PDMS	Poly(dimethylsiloxane)
PHEMA	Poly(2-hydroxyethyl methacrylate)
PMMA	Poly(methyl methacrylate)
PTAA	Poly(3-thiophene acetic acid)
PVCi	Polyvinylcinnamate
RFID	Radio frequency identification
S2S	Sheet-to-sheet (means the same as batch processing)
T-NIL	Thermal nanoimprinting lithography (same as hot-embossing or HE)
TCO	Transparent conducting oxide
UV-NIL	Ultraviolet nanoimprinting lithography
x-PMMA	Crosslinkable poly(methyl methacrylate)