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**Theme ICT-2009.1.1**  
***The network of the future***



**Deliverable D4.4**

**Work Package 4 – Spectrum Aggregation in practice**

**D4.4 SA Schemes Implementation Report**

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## Executive Summary

This deliverable represents the final outcome of WP4. The material presented here is the summary of the latest investigations carried on within the project that constitutes the building blocks that will be implemented in WP5 and assessed in WP2.

The first building block presented is related to the real-world evaluation of inter-carrier interference reduction techniques. This set of algorithms, already presented in the SAMURAI context, are here evaluated with the means of a hardware testbed, providing insights on the impact of real-world limitations of the equipment.

The second building block shown is related to issues that test equipment faces when generating and analysing multi-carrier signals. In particular, theoretical investigations focused on how to re-sample the signal for optimizing the performance of signal generators and spectrum analysers, and how to perform the optimal filtering for displaying real-time signals in the analysis phase with the lowest complexity possible.

The third and last building block is instead related to the final definition of the Autonomous Component Carrier Selection (ACCS) algorithm. The flowcharts of the version implemented in the light system level simulator and the one implemented in the PoC testbed are shown, evidencing which are the differences between the two versions.

The algorithms here described have been carefully considered and deeply investigated, both from a simulation/theoretical viewpoint and from an implementation/practical one. Most of them have been already made available to WP5 and WP2 for the final implementations and validation procedures.

Such building blocks, apparently far from one another, reflect the entire value chain of the real-world implementation of SA. They represent the skills and core interests of all the partners of the SAMURAI project, ranging from the development of transceiver chains supporting CA, through the methodologies and tools for testing them, ending into the network impact of CA and ACCS.



## Definitions, symbols and abbreviations

3GPP	Third Generation Partnership Project
ACCS	Autonomous Component Carrier Selection
ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
AMC	Adaptive Modulation and Coding
Arb	Arbitrary Waveform
AWGN	Additive White Gaussian Noise
BCC	Base Component Carrier
BCH	Broadcast Channel
BER	Bit-Error-Rate
BIM	Background Interference Matrix
BLER	Block-Error-Rate
BCC	Base Component Carrier
BS	Base Station
CA	Carrier Aggregation
CC	Component Carrier
CCRAT	Component Carrier Radio Allocation Table
ChE	Channel Estimation
COTS	Commercial Off The Shelf
CQI	Channel Quality Indicator
CSI	Channel State Information
DL	Downlink
DLC	Data Link Control
DUT	Device Under Test
EDA	Electronic Design Automation
eNB	Evolved NodeB (E-UTRAN NB/BS)
EVM	Error Vector Magnitude
eICIC	Enhanced ICIC
FDMA	Frequency Division Multiple Access
FFT	Fast Fourier Transform
GUI	Graphical User Interface
HARQ	Hybrid ARQ
ICIC	Inter Cell Interference Coordination
IF	Intermediate Frequency
IMT	ITU global standard for International Mobile Telecommunications
IMT-A	IMT-Advanced
KPI	Key Performance Indicator
LA	Link Adaptation
LTE	Long Term Evolution of UTRA(N)
LTE-A	Advanced Long Term Evolution of UTRA(N)
MAC	Medium Access Control
MCS	Modulation and Coding Scheme
MIMO	Multiple Input Multiple Output



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NAS	Non-Access Stratum
NTP	Network Time Protocol
OFDMA	Orthogonal Frequency Division Multiplexing Access
OTAC	Over-The-Air Communication
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PCC	Primary Component Carrier
PCell	Primary Cell (Carrier)
PER	Packet-Error-Rate
PDCCH	Physical Downlink Control Channel
PHY	Physical Layer
PRB	Physical Resource Block
PS	Packet Scheduling
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QoS	Quality of Service
QPSK	Quaternary PSK
RB	Resource Block
RF	Radio Frequency
RLC	Radio Link Control
RLF	Radio Link Failure
RRM	Radio Resource Management
RRAT	Radio Resource Allocation Table
RRC	Radio Resource Control
RSSI	Received Signal Strength Indication
Rx	Receiver
SA	Spectrum Aggregation
SCC	Supplementary Component Carrier
SCell	Secondary Cell (Carrier)
SC-FDMA	Single Carrier Frequency Division Multiplexing Access
SFN	Single Frequency Network
SIB	System Information Blocks
SINR	Signal to Interference plus Noise Ratio
SIR	Signal to Interference Ratio
SISO	Single Input Single Output
TDD	Time Division Duplexing / Test Driven Development (software)
TDMA	Time Division Multiple Access
TTI	Transmission Time Interval
Tx	Transmitter
UCI	Uplink Control Information
UE	User Equipment
UTRA	UMTS Terrestrial Radio Access
WiMAX	Worldwide Interoperability for Microwave Access





## 1 Introduction

This deliverable represents the final outcome of WP4. The investigations span from the RF/PHY to the higher L2/L3 algorithms.

The deliverable is structured as follows:

In Section 2 the investigations related to the RF/PHY feasibility of multi-carrier signal reception, generation, and signal analysis are presented.

In Section 2.1 the signal reception has been studied by using a simple WiMAX hardware testbed, in particular implementing and evaluating the performance of the techniques presented, together with their simulation results, in D4.3. Such techniques are related to the suppression of inter-carrier interference that arises when neighbouring subcarriers are selected.

In Section 2.2 the signal generation and analysis in test equipments have been instead investigated from a theoretical point of view. Specifically, in Section 2.2.1 the target are the re-sampling techniques required for generating or acquiring multi-carrier signals. In Section 2.2.2, instead, a stronger focus on the filtering structure for optimal and low complexity performance in real-time signal acquisition and displaying is considered for next generation spectrum analysers.

In Section 3 the investigations related to the ACCS simulation and implementation are presented. The algorithm has been finalized and the two different versions (the simulated one and the implemented one) are presented and compared for a full understanding of the algorithm possibilities. Additional analysis related to the signalling and control channel needs of the algorithm has been also included.

Section 4 draws the conclusions of this deliverable, by providing also a synthesis of the discoveries that this WP and the SAMURAI project have highlighted. How all these investigations are related to the rest of the SAMURAI project is also included.



## 2 Carrier Aggregation at RF/PHY Layer

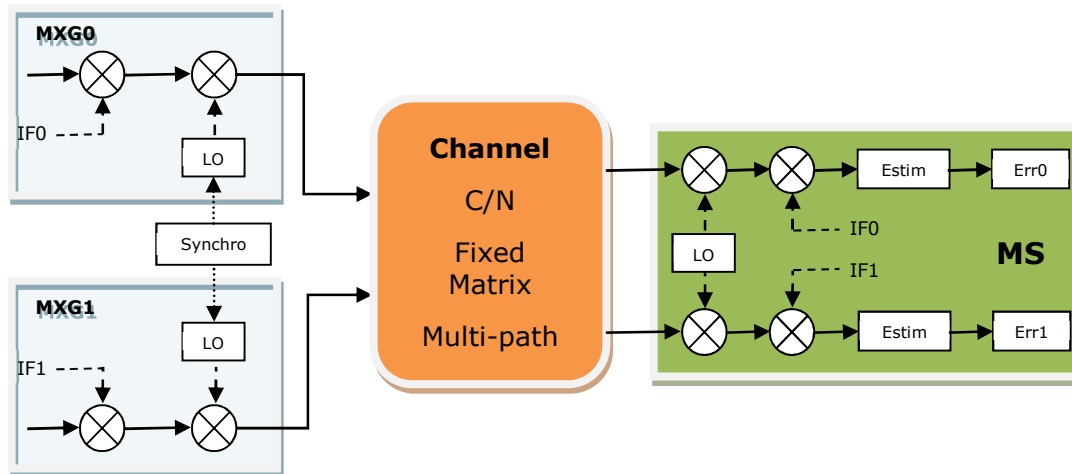
### 2.1 Inter-carrier interference mitigation techniques

In deliverable D4.2 [2], we have introduced the problem of interferers on WiMAX systems in a contiguous carrier aggregation case. It has been shown that even with a very robust modulation and coding scheme (MCS), spurious interferer may prevent the receiver from decoding properly the transmitted data. Then, in deliverable D4.3 [6], we have introduced the techniques to mitigate such interference under the constraint of low implementation complexity. Namely, we have focused on subcarrier erasure and we have shown the effect of pilot copy when the interferer effects the pilot carrying subcarriers.

In this contribution, we will focus on the tests from real implementation and will present the performances of the proposed interference mitigation method presented in [6].

#### 2.1.1 Implementation advances

In order to assess the performance of the proposed interference mitigation method we have focused on the following setup.



**Figure 1 Setup configuration used for performance assessment.**

In this setup, the two signal generators (MXG) emulate a single base station with two component carriers. Both MXGs and the mobile station (MS) are in RF mode. The LO of the BSs and MS are synchronized in frequency, that allows to align perfectly in time and frequency the transmitted signal. As a result, contiguous carrier aggregation could be emulated. In addition, we



used an interference generation equipment which is also synchronized with the BSs and the MS. In such a scenario, the frequency offset between the BSs and MS RFs are zero and the location of the interferer (the spur(s)) can be exactly known.

In the described setup, we have used

- Spirent SR5500M for noise generation
- SMJ100A for interference generation
- VSA for BS power and spur generation calibration

The proposed algorithm to mitigate spur has been implemented in the receiver firmware and integrated in the WiMAX USB dongle.

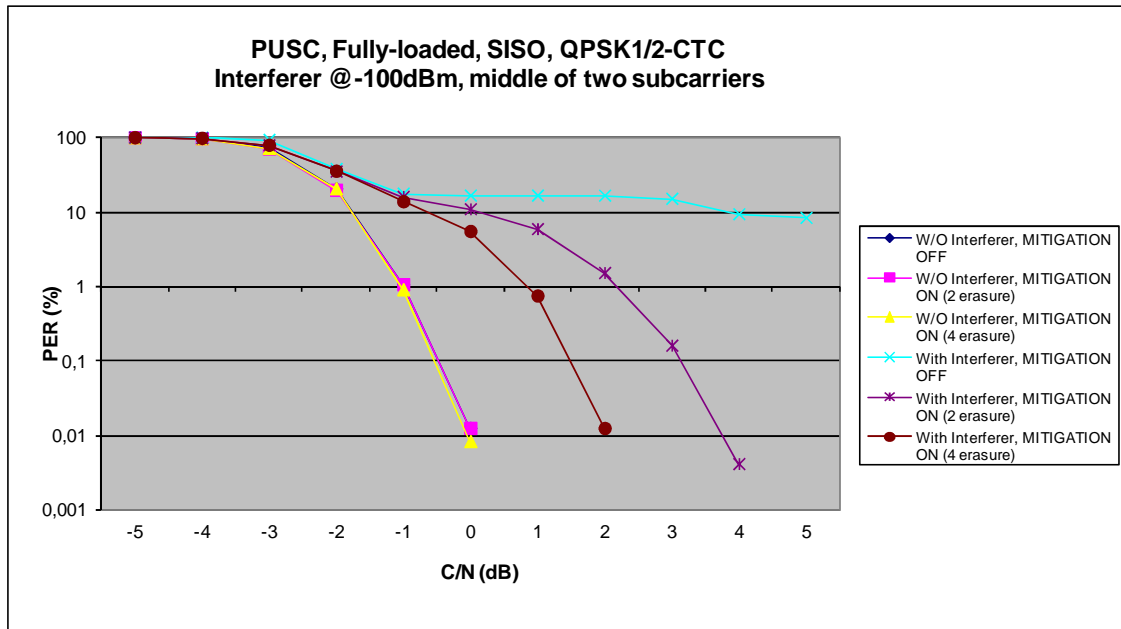
### 2.1.2 Performance evaluation

The performance figures of the proposed mitigation method have been already presented in deliverable D4.3 [6]. The effects of erasure and pilot copy have been shown using both single transmit antenna (SISO) and Matrix A transmission modes. In this section, we will focus on the same transmission modes and present the results we obtained from the setup explained above. We will focus only on the worst case interferer scenario where the level of interference can go up to -100 dBm.

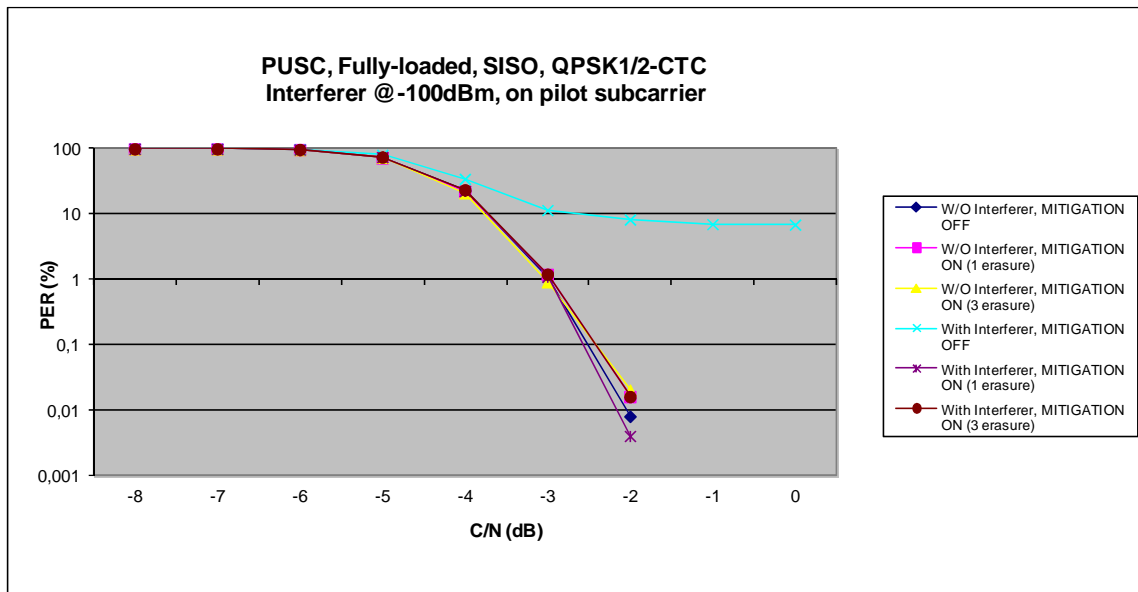
We will first show the results for SISO transmission in Figures 1-4 and focus on AWGN channel. In Figure 2, we see the effect of interferer mitigation based on subcarrier erasure in the worst case scenario, i.e., the interferer fall in the middle of two subcarriers (see [6] for more details related to the effect of interferer position). Square and triangle labeled curves show that the erasure of 2 and 4 subcarriers does not degrade the performance when there is no interferer (actually, the curves are superimposed on the figure). In the presence of the interferer, if the mitigation is not enabled we can see that the receiver will face with the error floor on the order of 10% PER. Note that in the simulations previously done and presented in [6] we did not include HARQ and in this case the target PER should be 1% in order to satisfy the performance requirements of WiMAX. When the mitigation is enabled we can see a remarkable improvement with erasure of 2 closest subcarriers. With increasing the number of erasure to 4 allows us gain at least 2 dB more and approaches to the case when there is no interferer. However, in this worst case, more than 4 subcarriers are affected and the gap is still large though it is acceptable. In Figure 3, we show the effect of the interferer when it drops on the pilot position. Since the pilots are indispensable for channel estimation, the erasure is not appropriate. As explained in [6], we copy the nearest pilot to the position of the pilot affected by the interferer while we continue to the erasure for the data subcarriers. When the mitigation is disabled the error floor is present as in Figure 2. However, we can see that when we enable the mitigation algorithm and perform the pilot copy operation, we recover almost all the loss. We show also the effect of additional erasure since taking into account any error in the position calculation. In this case, we may go for



more erasure and this will result in some degradation which is acceptable in these scenarios.



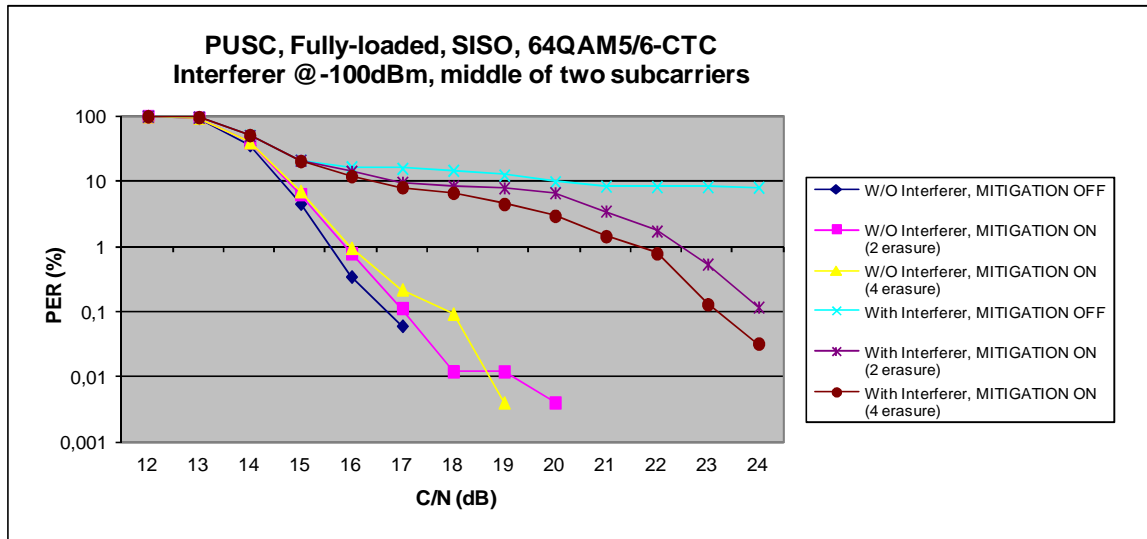
**Figure 2 Performance comparison for SISO, QPSK 1/2 CTC when interferer is in the middle of two subcarriers.**



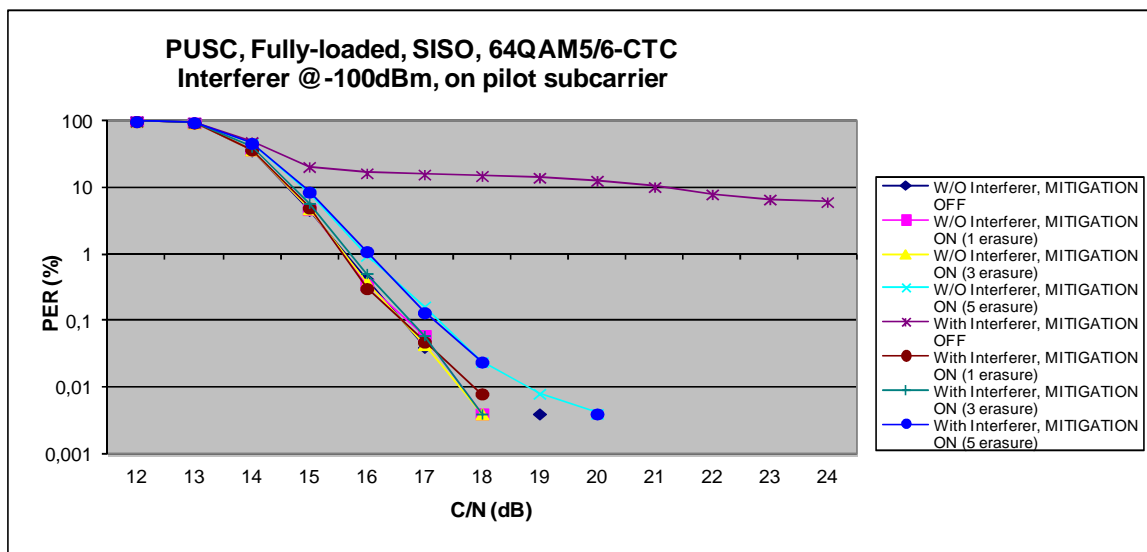
**Figure 3 Performance comparison for SISO, QPSK 1/2 CTC when interferer is on pilot subcarrier.**



In Figure 4 and Figure 5, we repeat the same test with the highest possible MCS defined for WiMAX which is 64QAM5/6. One can see that the previous conclusions are still valid and the mitigation algorithm provides highly satisfactory results even in the worst case for interferer.



**Figure 4 Performance comparison for SISO, 64QAM 5/6 CTC when interferer is in the middle of two subcarriers.**

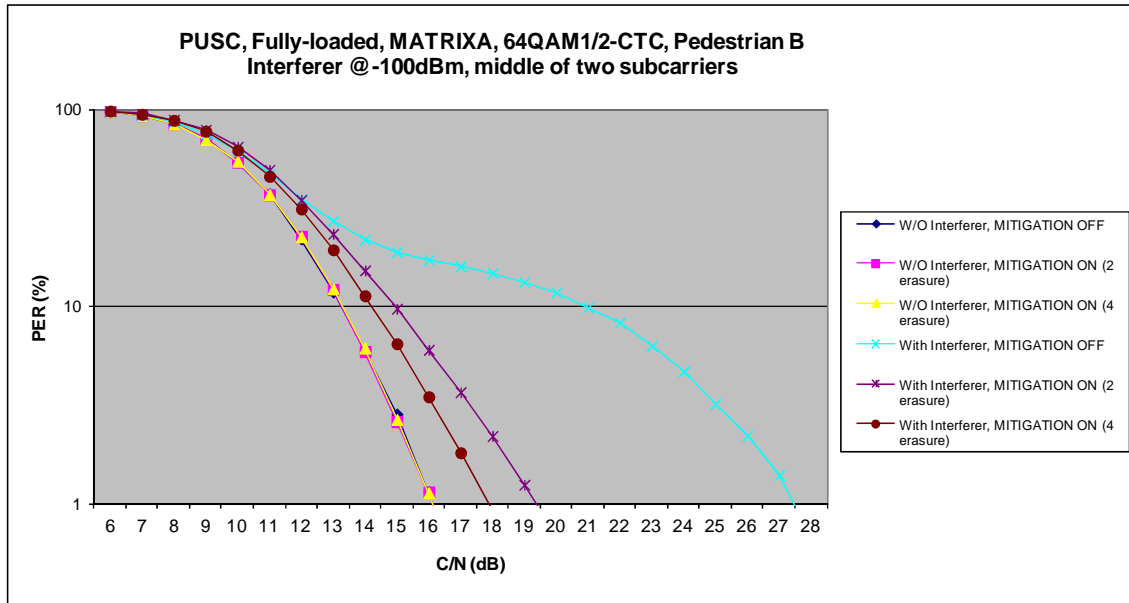


**Figure 5 Performance comparison for SISO, 64QAM 5/6 CTC when interferer is on pilot subcarrier.**

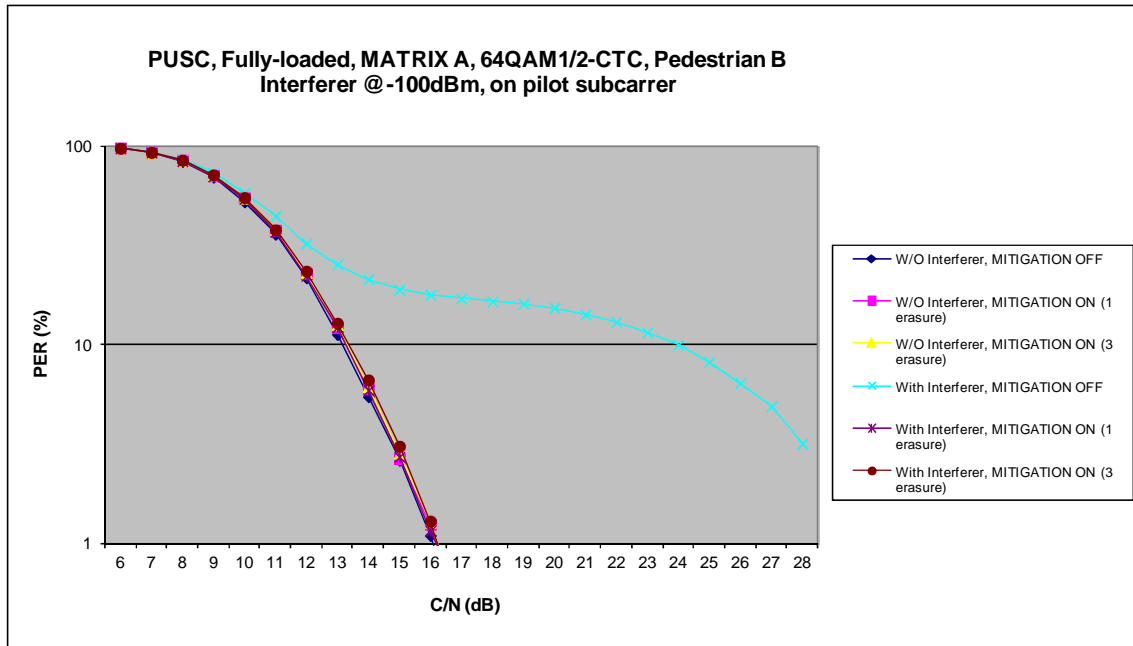
For the sake of completeness, we provide in Figure 6 and Figure 7, performance comparison for Matrix A in Pedestrian B channel. Thanks to the diversity inherent in this transmission mode, the effect of the interferer is less compared to the AWGN channel. When the mitigation algorithm is not



enabled, the target PER is achieved for an SNR level far beyond the nominal value. However, with the mitigation algorithm enabled the loss compared to the best achievable performance is on the order of 3 dB with 2 subcarrier erasure and drops to 1.5 dB with 4 subcarrier erasure. Figure 7 shows the effect of the pilot copy where the degradation is negligible even with 3 subcarrier erasures.



**Figure 6 Performance comparison for Matrix A, 64QAM 1/2 CTC when interferer is in the middle of two subcarriers.**



**Figure 7 Performance comparison for Matrix A, 64QAM 1/2 CTC when interferer is on pilot subcarrier.**



## **2.2 Carrier Aggregation Test Measurements Support**

### **2.2.1 Resampling Techniques**

From the test perspective, the signal generator instrument will need to accommodate multiple carriers of the IMT-Advanced signal along with the interference signals in order to adequately address the needs of the device under test in various carrier aggregation scenarios. Thus resampling of individual carriers and the expected interferences to a common upsampling rate is one of the essential tasks.

In the following sub-section we investigate the resampling techniques in order to accommodate the multi-waveform signal generation test support.

Some of the important test applications that can be addressed are:

- carrier aggregation
- interference testing, etc

In a multi-carrier or more generically in a multi-standard radio signal generation, one needs to match the sampling rate of each individual waveform to a final common desired up-sampling rate. This common up-sampling rate is determined by the total bandwidth that needs to be supported for each individual waveform in addition to the offset between these waveforms. Thus in a multi-waveform baseband signal generation one needs to first resample or in this case upsample the signal to a common sampling rate, then modulate the signal to include the frequency offset and finally add all the baseband signals.

The common sampling rate should always be large enough to provide the support for all the offsets involved. The last two operations that are the offset and the addition of waveforms in baseband is straightforward and thus we will further focus only on the feasibility study of the resampling with respect to signal generation.

A simple example can be the generation of a contiguous aggregation of two 5 MHz bandwidth LTE-Advanced carriers. In this case the native sampling rate of the individual carriers as specified by the standard is 7.68 MHz. Thus initially the two carriers are generated at their native sampling rate of 7.68 MHz. Since the carrier aggregated composite signal has to support the two waveforms, the final sampling rate should be able to accommodate the individual offsets and the total contiguous bandwidth. The straightforward solution here is to upsample the individual carriers by the factors of 2, which in this case is 15.36 MHz, and then offset or modulate the two waveforms by -3.84 MHz and +3.84 MHz carrier respectively. The two carriers are then summed resulting in a composite baseband contiguous carrier aggregated



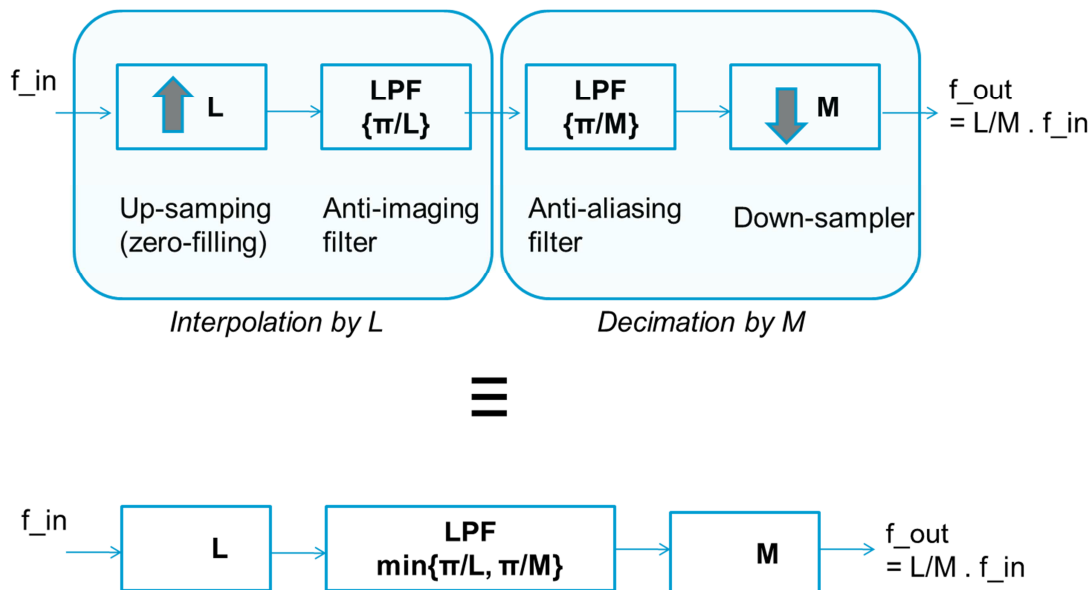


signal. In this example the interpolation is an integer factor of 2 which can be performed by first expanding the input vector of individual waveforms to the correct length by inserting one zero between the original data values. Then a special symmetric FIR filter is designed such that the filter allows the original data to pass through unchanged and interpolates between so that the mean-square errors between the interpolated points and their ideal values are minimized. It should be noted that the length of the FIR filter is directly dependent on the interpolation factor. Thus lower the interpolation factor, the lower is the computational complexity. For this example, we consider the native signal not to exceed the bandwidth=0.9n, for which the low pass FIR filter length design based on our software calculations turns out to be 73 taps long. Finally the FIR filter is applied to the input vector to produce the interpolated output vector.

In the case of non-contiguous mode, the final upsampling rate or the interpolation factor is usually considered to be the least integer multiple of the native sampling rate which can still accommodate the offsets. Thus for a non-contiguous carrier aggregation of two 5MHz signals with an offset of 10 MHz in-between the carriers, the least integer multiple of the native sampling rate is the interpolation factor of 4. Thus it is better to upsample the individual carriers to  $7.68 \times 4 = 30.72$  Mhz, and then offset the individual carriers by -5 and +5 Mhz respectively. For this configuration of interpolation factor of 4, our filter design software calculates the FIR filter length to be 145 taps long.

It is possible to do the same with a 20 Mhz carrier (with single IFFT) having two 5 Mhz edges. However here we are looking at signals that have already been formulated by individual IFFTs. Thus the resampling process here is a post IFFT and independent process.

It should be noted that any number of carriers with different bandwidths can also be easily aggregated for LTE-Advanced based on simple interpolation operation. This is because all the LTE-Advanced bandwidths from 1.4 to 20 MHz carriers follow the sampling rate that is an integer multiple of 1.96 MHz. For the same reason, W-CDMA signal can also be easily aggregated with LTE or LTE-Advanced signals as they all share the same native sampling rate of 1.96 MHz.



**Figure 8: Fractional sampling of a waveform**

However when it is required to aggregate signals of mixed waveforms with different sampling rates, then a simple integer interpolation operation may not be sufficient. This scenario is useful for interference testing. For example it is required to monitor the behavior of LTE communication when a third party user switches on the GSM or some other connection and thus resulting in an interference with the LTE communication. In order to perform a multiple radio signal generation tests, a GSM signal with native sampling rate of 270 KHz will have to be aggregated with the LTE signal. In this case the GSM will have to be fractionally upsampled, and this requires a two step process of first interpolation and then decimation. Thus if GSM has to be upsampled to 3.84 Mhz, a fractional upsampling factor of  $L=4608$  interpolation followed by  $M=325$  decimation factor will have to be performed. In order to perform this fractional upsampling, an interpolation operation is followed by an anti-imaging filter, and in the next step an anti-aliasing filter is followed by the decimation operation. This is also shown in Figure 8. Finally both the anti-imaging and the anti-aliasing filters can be combined into one. Typically if the interpolation factor is large compared to the decimation, then the filter length is dependent only on the interpolation order. Thus in this GSM case for the interpolation  $L=4608$  factor, our software computation results in a filter order of 167,057 taps. This filter order is extremely high and may not be practically implementable due to very large computational requirements. Thus this example shows that for mixed waveforms, the fractional resampling may sometimes result in a prohibitively large filter orders. This may also result in a very high processing complexity, large memory requirement, and thus limit the simulation time in dynamic



scenarios. In addition to large filter design requirements, a large fractional sampling, may also slowdown the waveform generation process as the input vector first needs to be interpolated with the required number of zeroes, and then finally the decimation of the redundant samples is performed in order to bring the signal down to the required sampling rate.

In order to speed-up and lower the filter design requirements, it is possible to split the fractional filter design into a cascaded solution. The cascades here are based on divide and conquer methodology, where the large fractional number is split into several manageable small fractions. The filter length requirement for each fraction is then small and practically implementable. For example the fraction  $L/M=4608/325$  can be further split into several small fractions such as  $L/M= 6/5. 6/5. 16/13. 8$

The cascading results in the following advantages:

- Reduced filter design effort
- Reduced computational cost
- Reduced storage requirements

In the cascade methodology every forthcoming fraction can exploit the stop band or the anti-imaging results coming out of the previous stage and thus increase its own transitional bandwidth specifications. As a result the filter requirements for the forthcoming fraction are further reduced and a filter with a broad transitional bandwidth can be employed, this results in a minimal filter order. This optimization can be understood more clearly from the following example.

For example, let us consider the upsampling of a waveform with a factor of 30 for a signal whose bandwidth equals  $\omega_0=0.9\pi$ .

In this case a one stage interpolation filter will result in a transitional bandwidth =  $(2\pi - 2\omega_0) / 30$ . The filter length from the computational software in this case = 1010 taps. It should be noted that a one stage design also results in 1010 multiple operations per input sample.

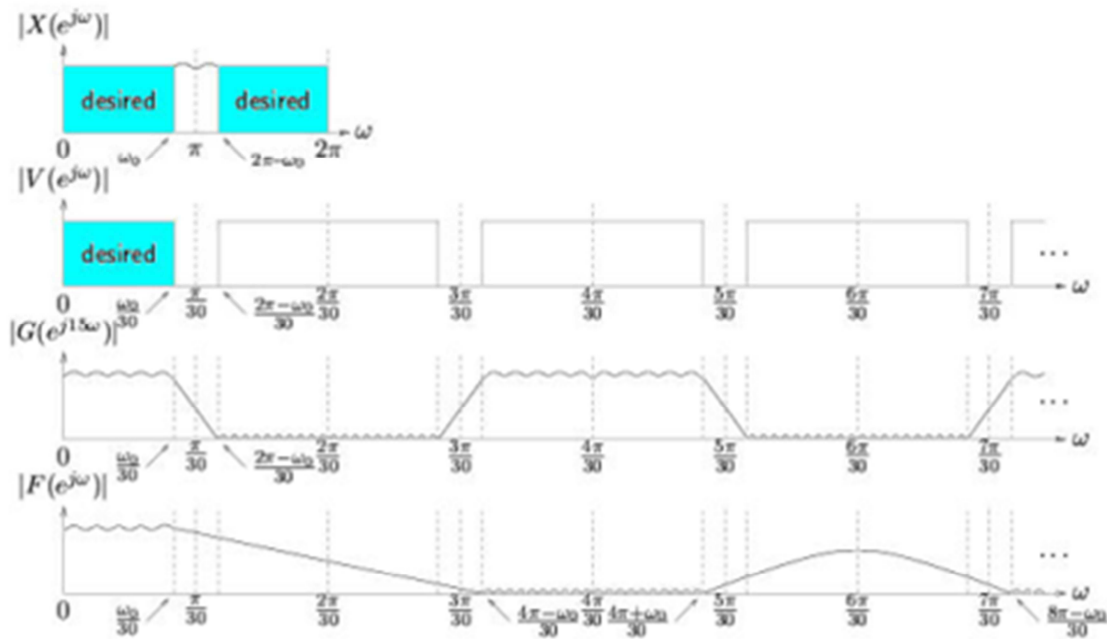
Whereas in a two stage cascaded solution, the factor 30 can be split into a factor of 2 and 15 respectively.

- Transition BW1 for factor 2 =  $\pi - \omega_0$ , and the filter length in this case=73 taps.
- Transition BW2 for factor 15 =  $(4\pi - 2\omega_0) / 30$ , and the filter length in this case = 88 taps.



Thus the total computational cost in the second case =  $73+2*98=269$  multiple operations per input sample.

Thus due to the two stage cascaded structure about  $1010-269=741$  operations can be saved. It should be noted that the second cascaded step exploits the stop band or the anti-imaging results coming out of the first step. This helps the second stage filter design to consider the increased transitional bandwidth and hence reduce the filter length requirements. Figure 9 shows this two stage cascaded upsampling process.



**Figure 9: Two stage upsampling**

Table 1 shows the computational cost requirements for various upsampling factors when compared with one, two and three stages cascaded upsampling structure. The table shows that for the factor 30 in row 3, it is possible to save more computational cost by up to only 183 operations by splitting the factor into 3 cascaded stages of 2, 3, and 5. Thus for increasing upsampling factor, multiple stages result in increased computational saving.



**Table 1: Computational cost for various cascade stages**

Final SR MHz	W/f MHz	Factor P/Q	1 stage		2 stage cascade P1/Q1, h1, P2/Q2 h2			3 stage cascade P1/Q1, h1 P2/Q2, h2 P3/Q3 h3		
			Fil. Order	Comp	Cas order	Filter order	Comp	Cas order	Fil order	Comp
		2	73	<b>73</b>						
		6	218	218	2,3	73, 20	<b>112</b>			
		30	1010	1010	2,15	73, 98	269	2, 3, 5	73, 20, 12	<b>183</b>
61.44	20	383/125=3.07	109	109	6/5, 64/25	218,928	83.77	6/5, 8/5, 8/5	218, 101, 47	<b>79.5</b>
80	15.36	125/24=5.208	184	184	5/4, 25/6	182, 323	106	5/4, 5/3, 5/2	182, 64, 32	<b>95</b>
80	20	4	145	145	2, 2	73, 14	<b>98.86</b>			

The following conclusions can be drawn from the table:

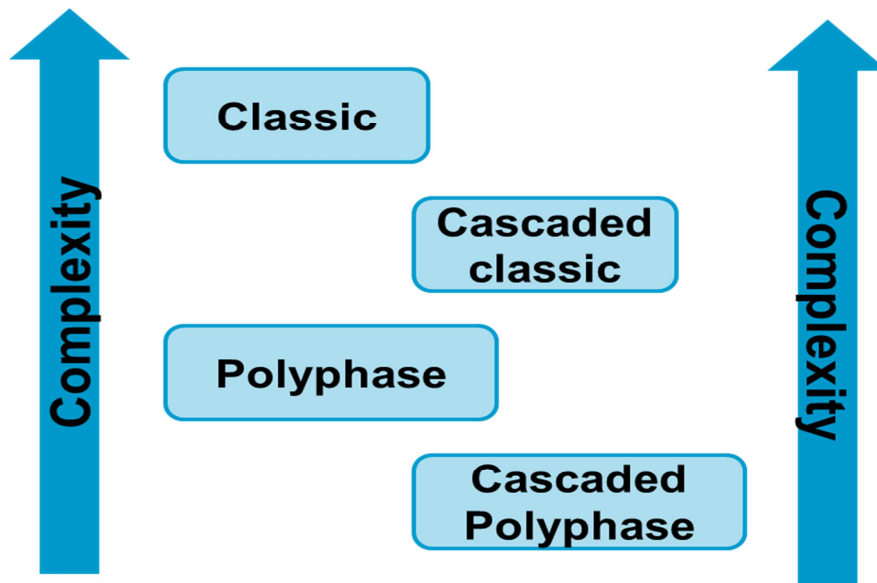
- Higher interpolation rates result in higher filter order and complexity
- Cascading is beneficial for interpolation fraction ratio > 2
- 3 stage cascading provides increasing benefits for interpolation fraction ratio >4
- For integer interpolation multiple, cascading shows increased benefits – see row no. 3,4,5.
- For very high order interpolation > 50– more than 3 stages may provide computational benefits – for example: GSM to be multiplexed with WLAN

For very high order resampling requirements, the choice of factorization may not be straightforward due to multiple fractional choices and the number of cascaded stages that can be selected. Hence this selection can be difficult to optimize. The work around solution to this would be to build a look-up table for very high order resampling factors.

Further optimizations can be done by implementing cascaded integer comb (CIC) or polyphase based filter in order to further reduce the complexity in cascaded structure. Figure 10 shows the various filter design versus the



complexity. The figure shows that cascaded based polyphase structure will typically result in the lowest computational requirement.



**Figure 10: Various filter design versus complexity**

Figure 11 shows the carrier aggregation of multi-waveforms. In this example, eight wireless standard signals are combined at  $F_c = 1$  GHz. Here is the list of the source signals and their respective carrier frequencies (Characterization Frequency,  $F_c$ ), Bandwidth (BW),

- LTE1:  $F_c$  1002.5 MHz, BW 5 MHz, FDD mode
- LTE2:  $F_c$  1007.5 MHz, BW 5 MHz, FDD mode
- WCDMA1:  $F_c$  997.4 MHz, BW 5 MHz
- WCDMA2:  $F_c$  992.4 MHz, BW 5 MHz
- GSM1:  $F_c$  988.4 MHz, BW 0.6 MHz
- GSM2:  $F_c$  987.8 MHz, BW 0.6 MHz
- EDGE1:  $F_c$  1011.6 MHz, BW 0.6 MHz
- EDGE2:  $F_c$  1012.2 MHz, BW 0.6 MHz

All the signals have been upsampled to the common sampling rate of 30.72 MHz.

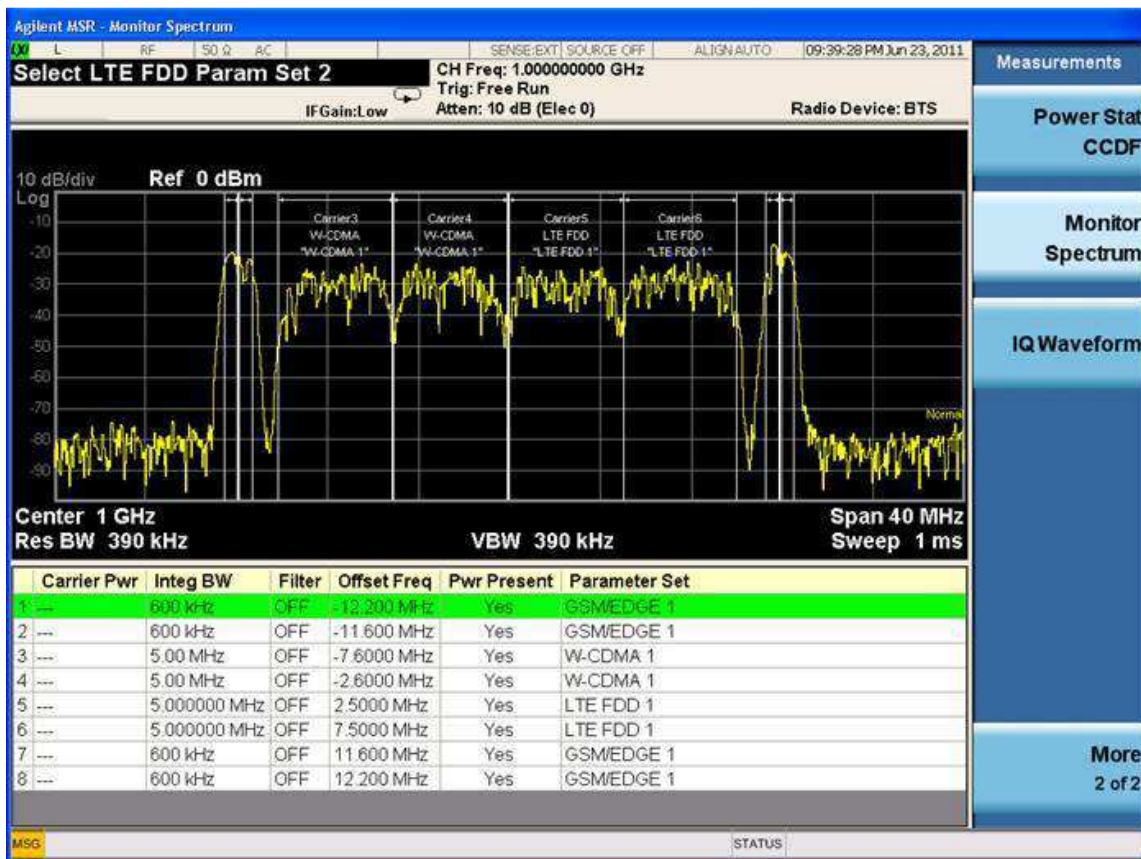


Figure 11: Carrier aggregation with various waveforms

## 2.2.2 Carrier Aggregation Spectrum Analysis

### 2.2.2.1 Motivation

So far, mostly, we have focused on the transmit side: how to build the stimulus signal to test carrier-aggregation powered receivers. As a matter of fact, the analysis (= to test a CA transmitter) side is also worth a study. Carrier aggregation comes along with new challenges: wider bandwidth and multi-channel property. Obviously, analysing  $N$  carriers simultaneously could be done using a set of  $N$  analyzers stacked in parallel. However, not only would it be an expensive solution, synchronization issues would also arise.

Within the SAMURAI project, we have also focussed on the channelization aspect of analysis: that is how we can extract a set of narrowband channels from a single wideband signal. Thus this work will eventually help in defining cheaper and more effective testing solutions, providing an integrated system for CA signal analysis. The outcome of this theoretical work will lead, within the end of the project to a hardware PoC solution.

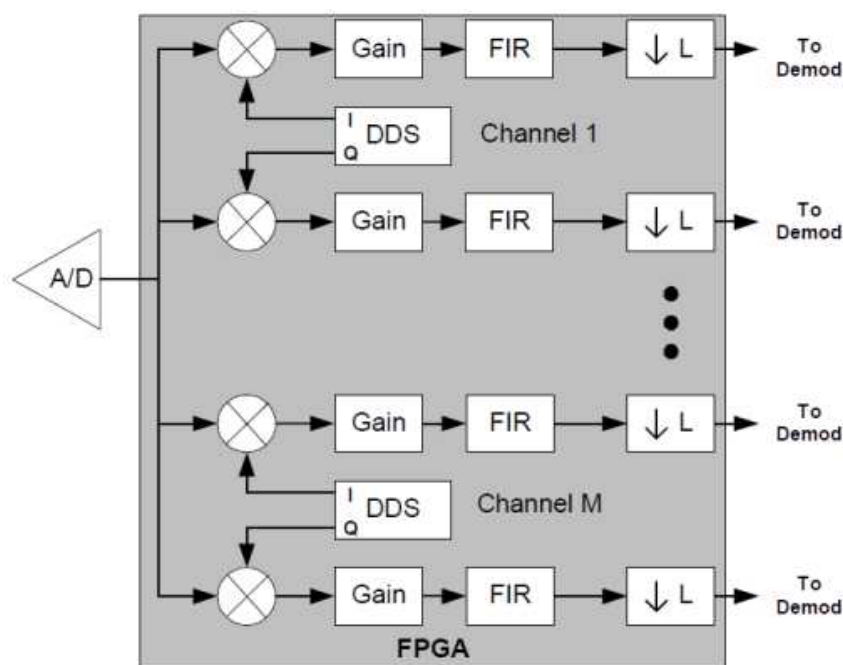




### 2.2.2.2 Technical description

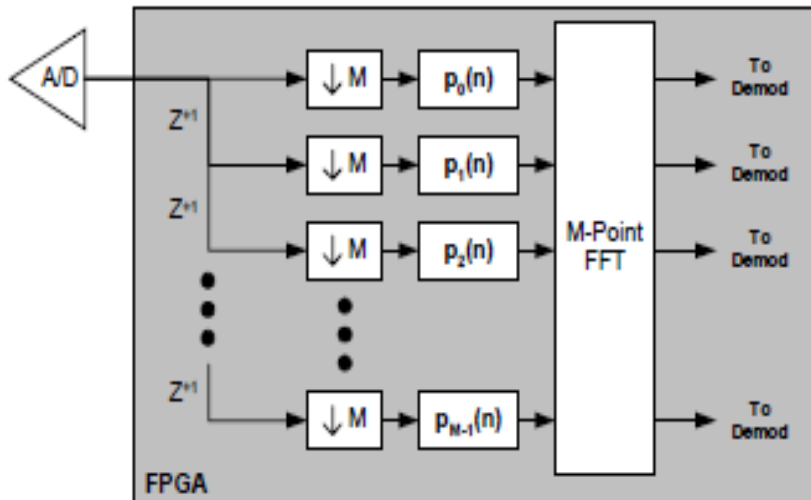
The FFT channelizer is a fast implementation of the Fourier transform that was developed in 1965. It has since become a cornerstone in modern digital signal processing. The polyphase channelizer, a more recent development, implements the frequency channels using standard FIR filters while taking advantage of the processing speed of the FFT. This gives the polyphase approach greater flexibility in terms of shaping the channel gain response (with respect to frequency) without unnecessarily sacrificing processing speed.

A digital down converter (DDC) provides the channelization function through a classic heterodyne technique. In this technique, the wideband signal is mixed with a synthesized carrier at the carrier frequency of the channel of interest to baseband of that channel. The resulting signal is then filtered and decimated to isolate and extract the channel of interest from the wideband signal and reduce the overall sample rate to the minimum necessary to support that channel. The primary advantages of the DDC techniques are the flexibility in selecting both the carrier frequency and channel bandwidth. However, for complex channel structures where both wideband and narrowband channels may occupy the same input signal a mix of down converter technologies may be required, complicating the architecture of the channelizer block.



**Figure 12: Multichannel digital down converter (DDC)**





**Figure 13: Filterbank - FFT**

In signal analysis, windows are used to suppress undesirable sidelobe effects which occur when the Fourier transform is used on finite length data blocks. In the channelizing application, higher sidelobes translate to higher interference from signals appearing in channels that are close in frequency to a given channel. This can become a problem in dense signal environments where the goal is to demodulate a target signal in the presence of strong inband signals.

Sidelobe suppression comes at the expense of frequency resolution, which results in a larger channel bandwidth. Although this reduces selectivity and thereby increases the sensitivity to adjacent channel interference, the overall reduction in sensitivity to inband interference can be a desirable compromise for many applications.

Regardless of the window, the filter gain drops towards the edge of the channel. This is not a desirable behaviour since it reduces the ability to detect signals near the channel edges when the signal-to-noise is low, and can lead to distortion effects for modulated signals due to frequency to amplitude conversion. Hence the need of overlapping data blocks are used which in turn increases the sampling rate.

One of the shortcomings of the FFT channelizer is that it has very little flexibility in terms of shaping the gain response of the frequency channels. This can lead to cochannel signal interference when there is very strong



inband interference relative to the desired signal, as well as reduced detection sensitivity and distortion effects.

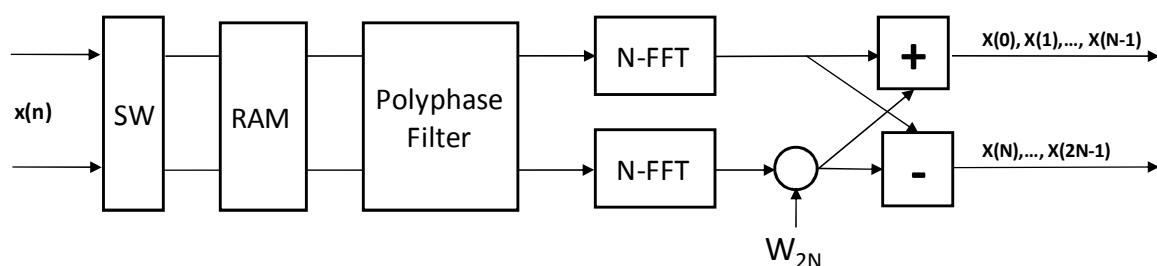
Overall, the polyphase channelizer yields a more desirable channel response than the FFT channelizer with a flatter passband, greater stopband suppression, and a more rapid transition between the passband and stopband. The disadvantage is that more data is required to compute the channel values, resulting in a larger observation time for a given frequency resolution.

### Tradeoffs

- Single channel based : DDC
- Multichannel : DDC, FFT based, Polyphase FFT
- Channel filter response: flatness, transition BW, etc
- Sampling frequency, BW, throughput, data overlapping, HW clock tradeoffs
- Channel spacing, resolution bandwidth

The reduction in gain away from the center due to coarse tuning of the channel will reduce the effective SNR of signals whose center frequency is not aligned with the center frequency of the channel or modulated signals whose bandwidth is not small relative to the channel width.

The high side lobes significantly degrade the ability to detect (and demodulate) weak signals in the presence of strong adjacent signals. Filtering can be used to reduce the side lobes to more acceptable levels and improve detection performance when strong signals are present.



**Figure 14: 2-phase Flexible Polyphase FFT Channelizer**



Fs (Ms/s)	Overlap	FFT size	Throughput	RBW ?-window parameter Uniformwindow (?=1)	Channels	Clk
Fs (x clk)	0	128 - 2N	Fs	?/2N	1	clk
Fs(x clk)	50%	128 - 2N	Fs/2	?/2N	1	clk
Fs/2 (x clk)	0	128 - 2N	Fs/2	?/2N	2	clk
Fs/2 (x clk)	50%	128 - 2N	Fs/4	?/2N	2	clk

**Table 2: Parameter Tradeoffs**

### 2.2.2.3 Implementation

The main focus of Agilent in this task is on the implementation side. The team is currently busy implementing some of the described methods. Basically, FPGA coding is performed on a Xilinx Virtex 6 around an ADC platform. A demonstration is planned for the end of the project.



## 3 Carrier Aggregation at MAC Layer1-Layer3

### 3.1 ACCS algorithm for simulation and platform implementation

This section summarizes the development and features of the Matlab™ simulator platform and PoC demonstration platform implementation used to investigate the ACCS algorithm proposed within the SAMURAI project [1][2][3][6]. The description highlights the main PoC implementation blocks, addressed in Work-package 5 [5].

Naturally, the detailed SW/HW PoC implementation (C/C++ based with advanced multi-threading) and the Matlab™ simulation platform (linear scripting language) differ and both have specific coding details and solutions, which are not described in this document. The main ACCS functionalities are, however, fully aligned between the Matlab™ simulations and PoC implementation and, these are the focus of the description in the following Sections.

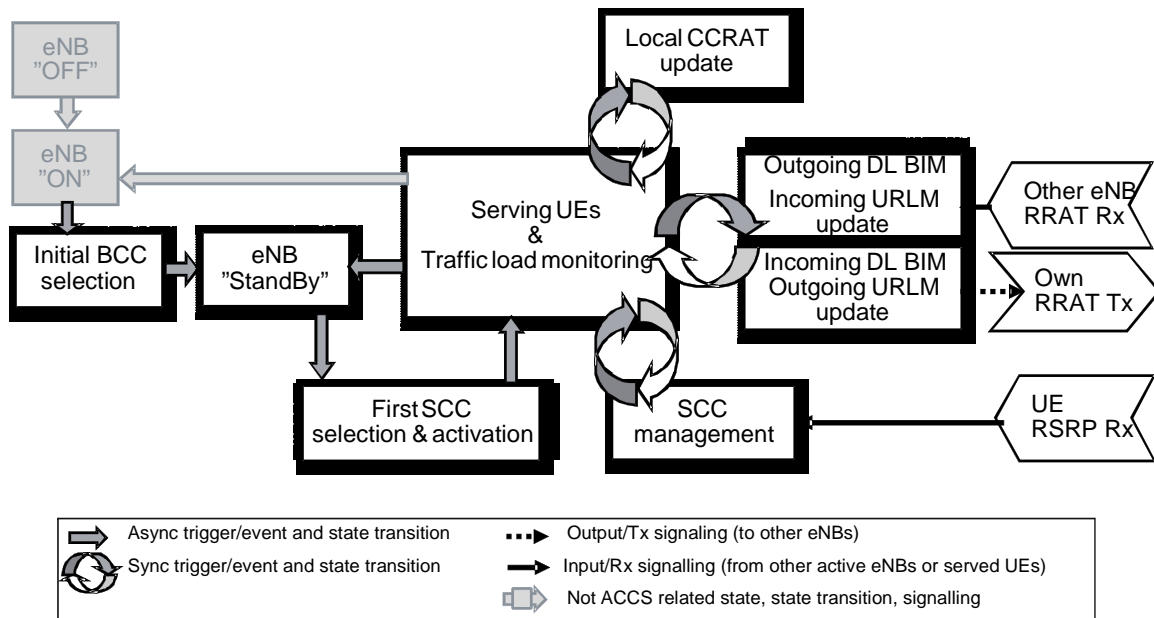
In Section 3.1.1 we describe the most relevant details of each the main ACCS blocks using simplified flow-chart diagrams. The rest of the diagrams are provided in the Appendix 6.1. Details on the related simulation solutions are provided in Section 3.3. Details on the related PoC implementation solutions are provided in Section 3.2.

#### 3.1.1 Functionalities

The main functionalities of the proposed ACCS algorithm, which have been addressed in both the simulation platform (Matlab) and the PoC implementation, are presented in Figure 15.

Each of the other main blocks is described using flow-chart diagrams in the following sections. The shaded block are not in the scope of the ACCS development and are represented only for completeness.

The implemented signalling mechanisms differ between the PoC implementation and simulation platform and are described in the corresponding Section 3.2.1.4 and Section 3.3.1 respectively.



**Figure 15: Main ACCS functionalities, addressed in both the simulation platform and the PoC implementation.**

The diagram in Figure 15 shows a simplified version of the similar figure presented earlier in Deliverable D4.2 and D4.3 [2][6]. The reason for this simplification is the targeted full alignment between the simulation and PoC implementation features. This allows us a more streamlined evaluation of the proposed ACCS mechanisms and tuning of the related system-wide parameters. Furthermore, the PoC deployment scenario and simulation scenario can also be better aligned as summarized in Table 3-1 and explained in detail in Deliverable D2.2 [7].

Unless otherwise specified all the proposed ACCS procedures depicted in Figure 15 run autonomously and asynchronously in all the simulated / analyzed Femto eNB cells.



**Table 3-1: Summary of the parameters for the ACCS evaluations. For the results presented in Deliverable D2.2 different settings were used depending on the analyzed deployment scenario [7].**

Parameter	Setting/ value
System BW / #CC	10 MHz / 3 CCs
Frequency band	2 GHz, in scenario #1 5 GHz, in scenario #2
Total Tx Power (fixed PSD per active CC)	20 dBm, in scenario #2 0 dBm, in scenario #2
Number of UEs per eNB (CSG)	Random: 1 to 4, in the scenario #1 Fixed: 1, in scenario #2.
eNB deployment ratio	{25, 100} %, in scenario #1 100%, in scenario #2
eNB (cell) activation ("switch-ON")	Spatially random sequence with 1 eNB activated per SF
Total time-duration simulated	Scenario dependent #SF.
UE buffer size	Full buffer or 20 Mbit per UE, in scenario #1 Full buffer or 80 Mbit per UE, in scenario #2
UE average OFF-time	{10.0, 5.0, 1.0} s
<i>PLThreshold</i>	{140, 120, 100, 90, 80, 70} dB
<i>ACCSSubFrameLength</i>	1 SF = 100 ms
<i>ACCSTimeFrameLength</i>	5 SF = 500 ms
<i>BCCInitSel_MaxTimer</i>	{1, 2, 10, 20, 40} SF*
<i>BCCInitSel_TimerWin</i>	{1, 2} SF*
<i>CoI_Target_BCC</i>	20 dB**
<i>CoI_Target_SCC</i>	8 dB**
eNB-to-eNB/ eNB broadcast signalling channel delay	1 SF

### 3.1.2 ACCS building blocks and flow-charts

A map of the main ACCS building blocks, procedures and their interdependency is presented in Figure 16. In the Sections 3.1.2.1 and 3.1.2.2 we describe the most relevant details of each the main blocks using simplified flow-chart diagrams.

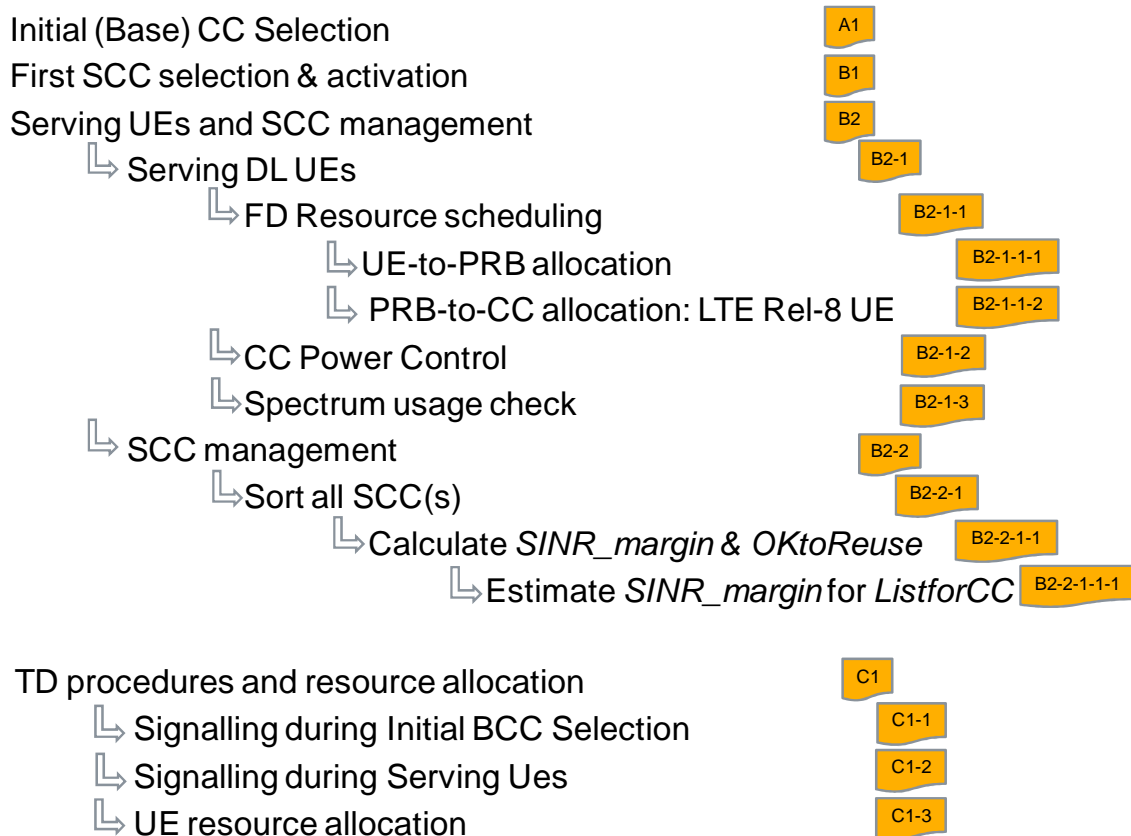
Along with the functionality blocks we also indicate which blocks have been considered in the simulations (*S*) and/or implemented in the PoC (*P*). The blocks which are not marked with neither *P* or *S* labels were not considered relevant for the evaluation of the proposed ACCS mechanisms, although they may be needed in a real commercial platform implementation due to other system constrains and consideration, e.g. the specifics of LTE RF/PHY, time-frequency scheduler, etc.

As a general rule, any procedure which in practice would need to be run at a higher time granularity than set by the *ACCSSubFrame* system parameter is



not simulated in the L2-L3 simulator platform. The *ACCS\_Frame* system parameter is a integer multiple of the *ACCS\_SubFrame* and determines the rate of the main ACCS procedures. All ACCS related sub-procedures run at the rate set by the *ACCS\_SubFrame*. Both *ACCS\_Frame* and *ACCS\_SubFrame* have well defined meanings and specifically set values in the PoC implementation and the simulations.

In terms of network level synchronisation, only a relatively loose synchronisation between all Femto eNBs is assumed at the *ACCS\_SubFrame* timing level. This means that the start (and end) of the *ACCS\_Frame* periods can be fully desynchronized between the Femto eNB and the minimum desynchronisation time is assumed to be *ACCS\_SubFrame*. In practice this is easily achievable by listening and decoding the broadcast transmission of each Femto eNB (similar to UE RACH procedures).



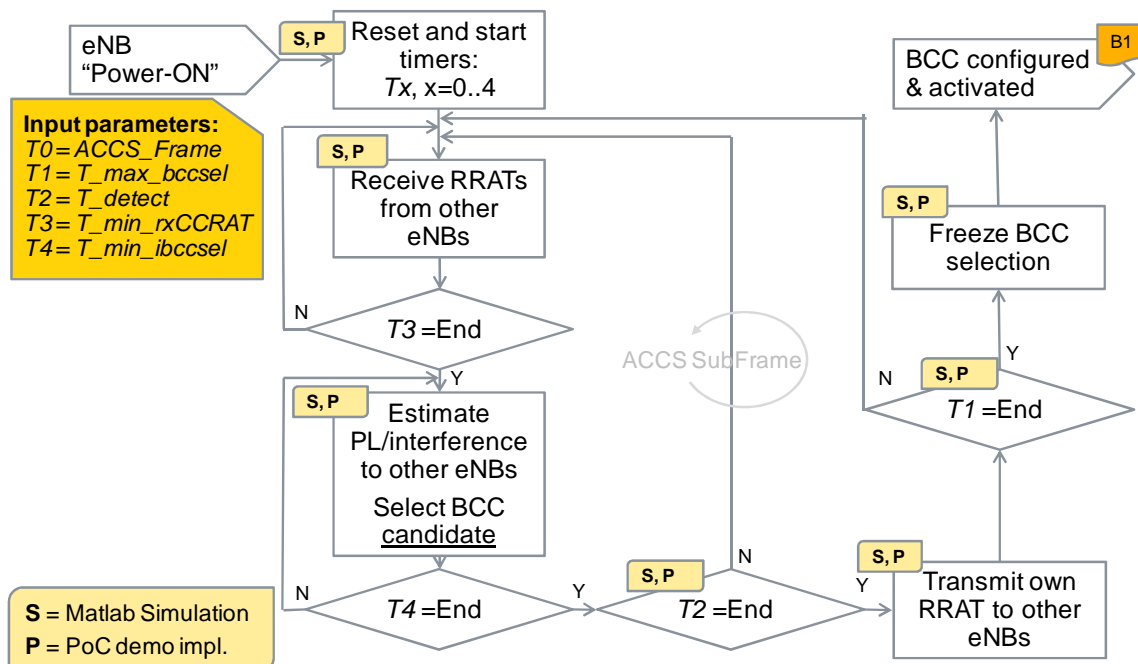
**Figure 16: Map of the main ACCS building blocks and procedures. The labels on the right-hand side are used to identify the corresponding flow-chart Figures in the Sections 3.1- 3.2 and Appendix 6.1.**



### 3.1.2.1 Initial BCC selection

The flow chart for the Initial BCC selection algorithm is given in Figure 17. The listed  $T_x$   $x=1..4$  timers have been described in Deliverable D4.3 [6]. The chosen PoC implementation and simulation solutions do not need to use the timers  $T3$  and  $T4$ . The  $T0$  timer equals the selected  $ACCS\_Frame$  length.

For the BCC-only simulation studies presented in Deliverable D2.1 [3] and D2.2 [7] this is the evaluated mechanism.



**Figure 17: A1 - Initial BCC selection. The  $T_x$  timers have been described in Deliverable D4.3 [6] .**

### 3.1.2.2 ACCS mechanisms

In Figure 18 and Figure 19 we show the flow-charts for the 'First SCC selection and activation' and the 'Serving UEs and SCC management' procedures. The two main building blocks for the latter procedure are further detailed in Figure 20 and Figure 21.





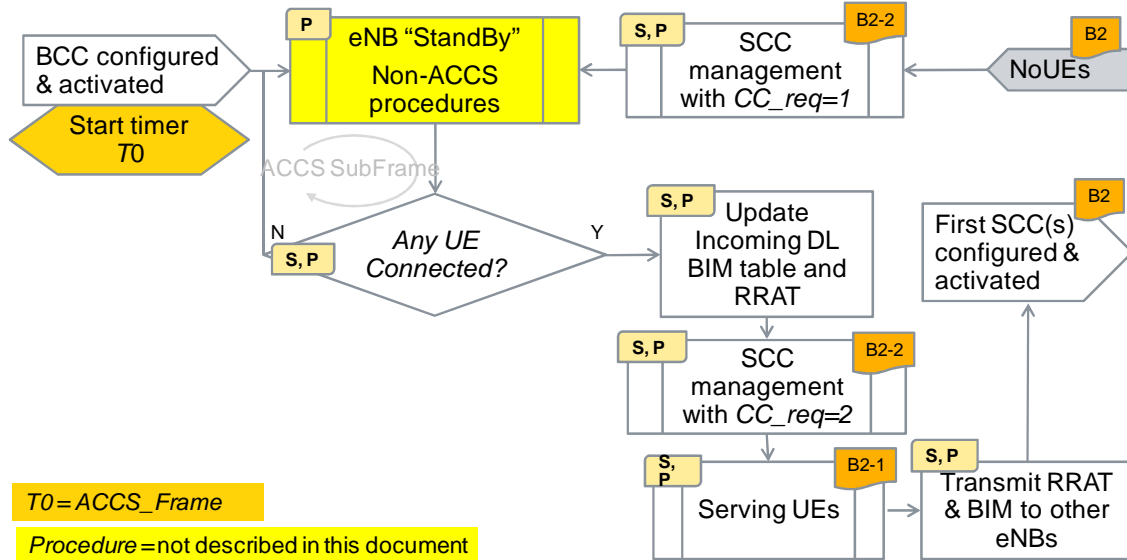
The '*First SCC selection and activation*' (Figure 18) procedure is used after the '*Initial BCC selection*' has finished and when there is at least one UE to be served (active UE) in cell. In our simulation/PoC studies, the number of required CCs is set by default to BCC + 1SCC ( $CC_{req} = 2$ ) in order to analyze and run the system only in the load region of interest. For all BCC-only simulation studies presented in Deliverable D2.1 [3] and D2.2 [7] the '*Initial BCC selection*' procedure is evaluated combined with the '*Serving UEs*' procedure, i.e. the SCC management procedures are disabled by setting  $CC_{req} = 1$ .

The '*Serving UEs and SCC management*' (Figure 19) procedure uses an outer loop performed with *ACCS\_Frame* periodicity and an inner loop running with *ACCS\_SubFrame* periodicity.

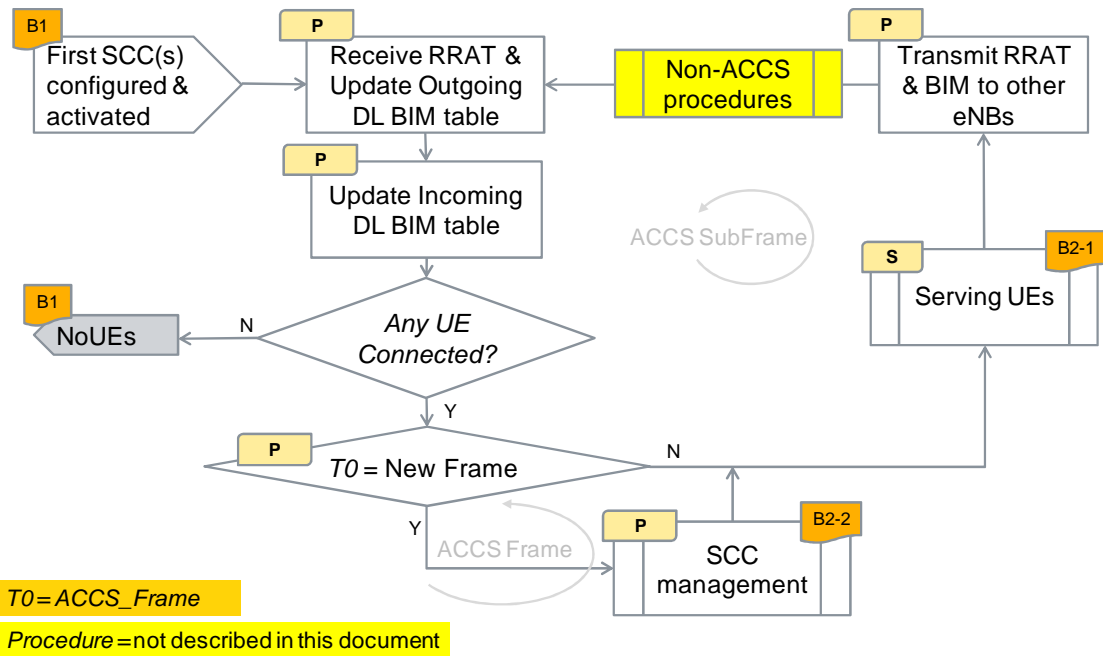
In the simulation platform the mechanism related to '*Serving UEs*' (Figure 20) and resource allocation for the served DL UEs are modelled via a simple time-frequency abstraction, presented in Section 3.3.2 and Appendix 6.1. These mechanisms are, however, not implemented in the PoC platform and all UE radio-link related KPIs are derived based on estimated DL wideband SINR as presented in Section 3.2.1.2. The '*Serving UEs*' procedure runs with *ACCS\_SubFrame* periodicity. Naturally, in a real-life system implementation this block involves also the per TTI scheduling and fast-link adaptation procedures.

The '*SCC management*' procedure (Figure 21) runs with *ACCS\_Frame* periodicity and sorts all the available SCCs (all possible CCs except own BCC) based on an estimated wideband SINR quality metric, without using UE measurement reports (see also Appendix 6.1).

Currently, the selection/activation of more SCCs and de-selection/de-activation of already active SCCs can be performed based on the same ranking mechanism. The full 'de-activation' mechanism is currently neither simulated nor implemented and a simple de-activation of all SCC is used instead when there is no traffic to be served in the cell. However, a more performance mechanism for de-activation of active SCC is to actually use the RSRP/RSRQ measurement from the connected UEs on all configured SCCs. This option will be explored in the last phase of the PoC development and evaluations (June 2012).



**Figure 18: B1 – First SCC selection and activation.**



**Figure 19: B2 – Serving UEs and SCC management.**

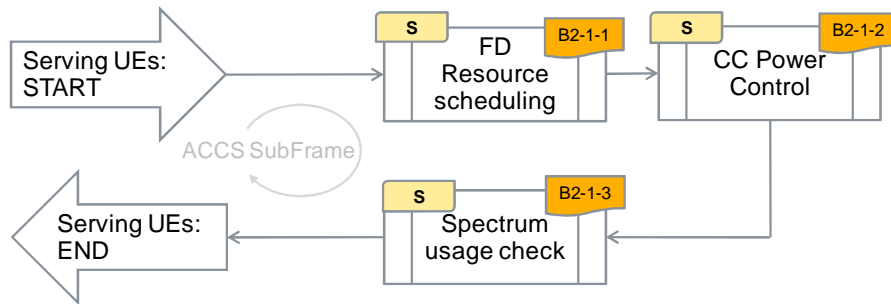


Figure 20: B2-1 – Serving DL UEs (simulations only).

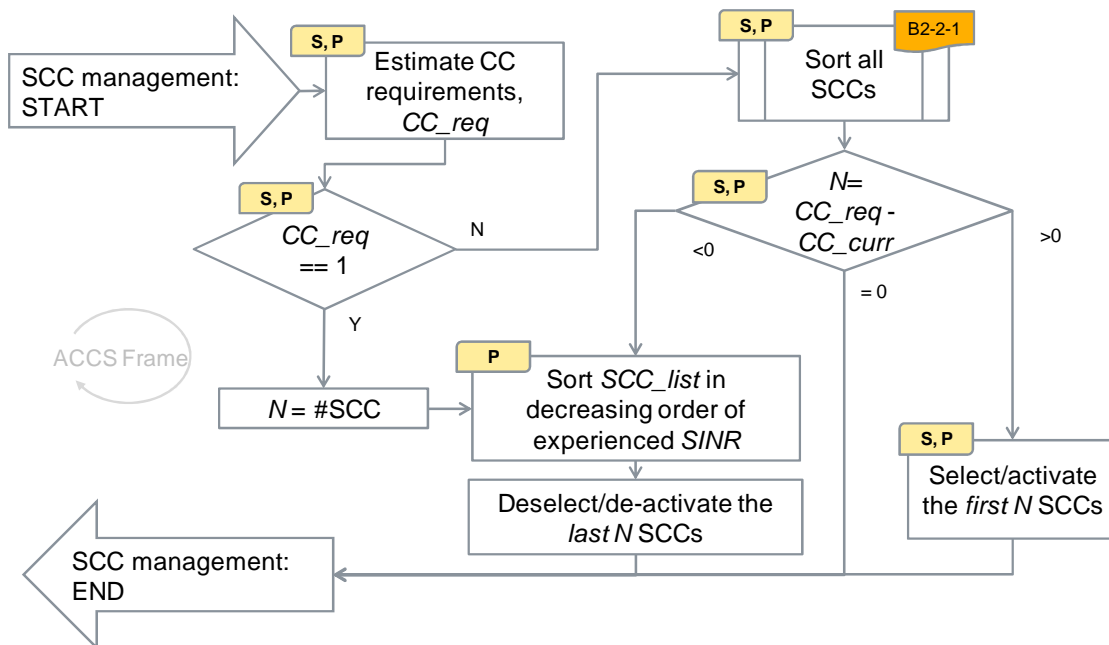


Figure 21: B2-2 – SCC management. The full 'de-activation' mechanism is currently neither simulated nor implemented and a simple de-activation of all SCC is used instead.

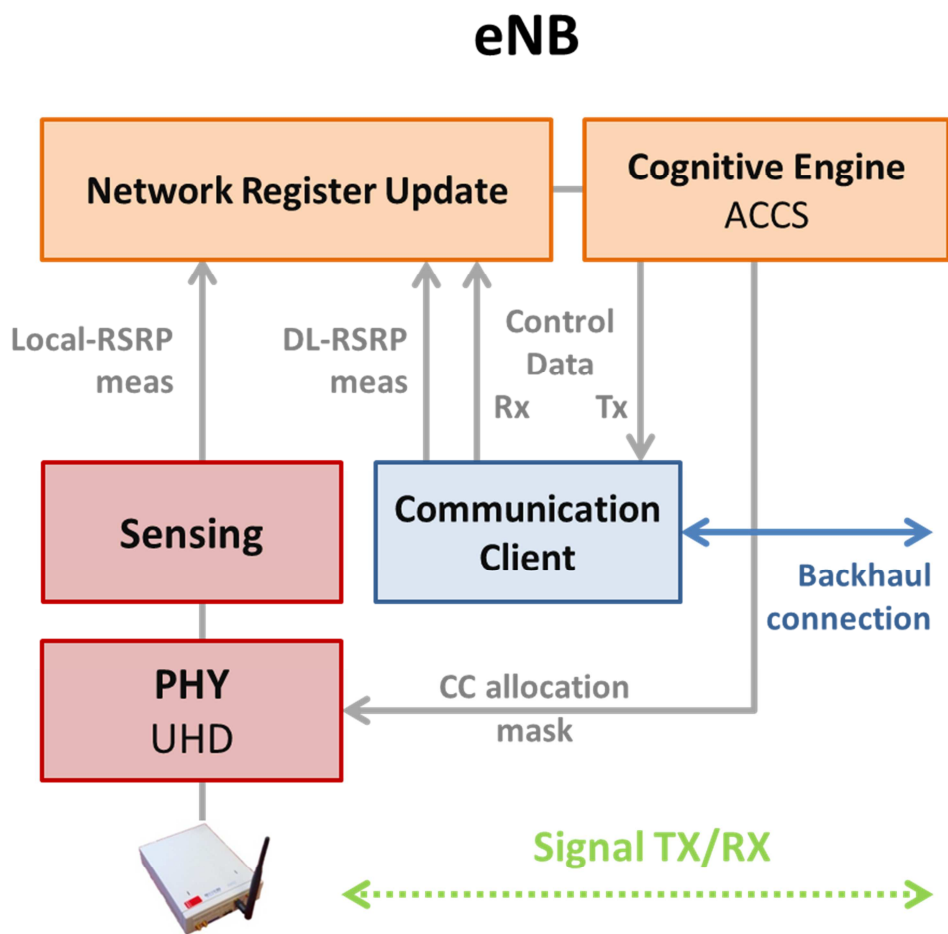


## 3.2 ACCS PoC Implementation

### 3.2.1 Implementation advances

#### 3.2.1.1 BCC Selection

The Initial BCC selection process occurs at the eNB side. The implemented software architecture for the eNBs is depicted in Figure 18.



**Figure 22 - eNB software architecture**

The BCC selection operations flow is implemented according to the scheme of Figure 13. At bootstrap, the eNB is activated in RX mode; the PHY component feeds the Sensing component which computes RSRP values for each CC and each node ID.

The RSRP measurements are then combined to the allocation information data received from the control channel, and used to perform a BCC selection.



The ACCS component performs BCC selection and takes care of signalling the CCRAT over the control channel. When the BCC selection is completed, the ACCS component generates a CC mask that is used to configure the PHY component.

### 3.2.1.2 UE Role

In the developed setup the UE has a mere performance measurement role. This is also due to the fact that the focus of the SAMURAI project is on DL. The UE is hence a simplified entity that measures the channel conditions and reports them to both the server (that controls the demonstrator) and its serving eNB.

In Figure 19 is depicted the implemented UE software architecture. The RSRP measurements generated by the Sensing component are fed back to the affiliated eNB through the backhaul connection. The testbed server takes care of managing the UE affiliation.

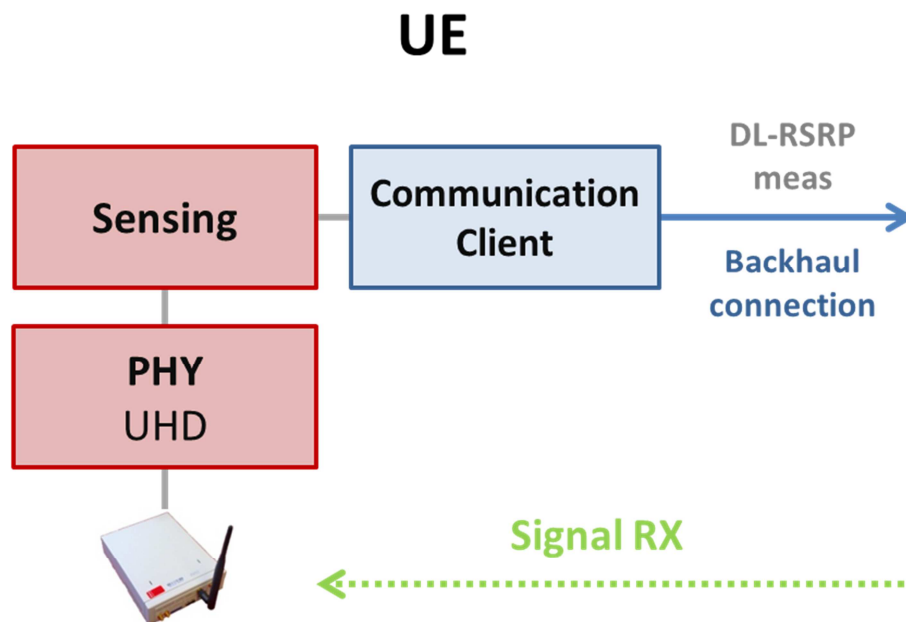


Figure 23 - UE software architecture

### 3.2.1.3 SCC Selection

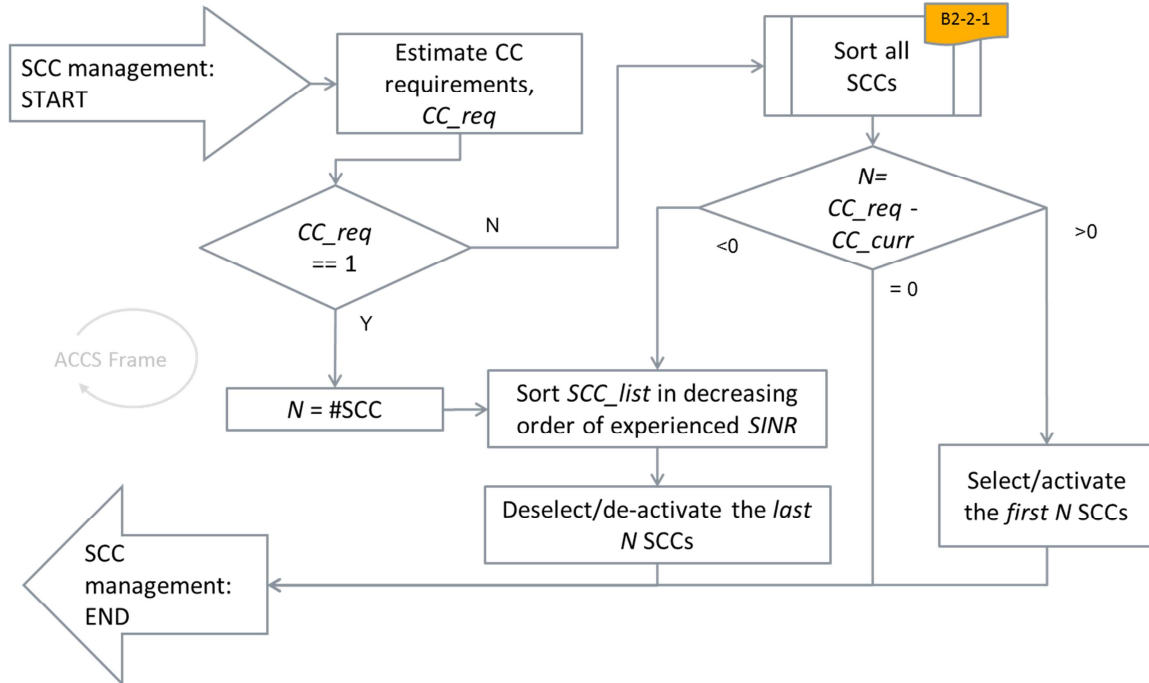
The implemented SCC selection process is illustrated in Figure 21 and Figure 20. The activation of additional SCCs is based on the computation of DL SINR margins; the de-activation of SCCs instead, is based on the experienced SINR over the active SCCs.

The SCCs with higher DL margin values are activated first, while the SCCs with lowest experience SINR are the first to be released.



## SCC management

B2-2



**Figure 24 - B2-2 SCC Management procedure at eNB**

Figure 21 depicts the sorting process for additional SCCs selection. CCs already in use as BCC or SCC, are discarded; the remaining CC are sorted according to the minimum DL SINR margin, and discarded if the margin is negative.

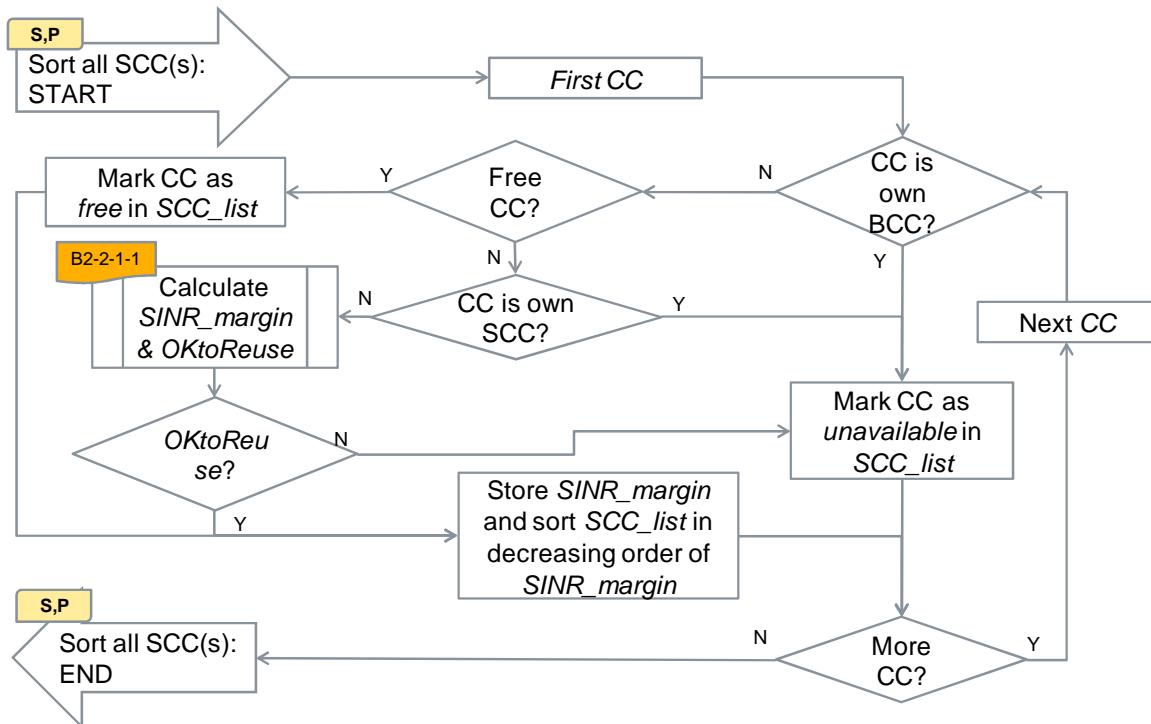


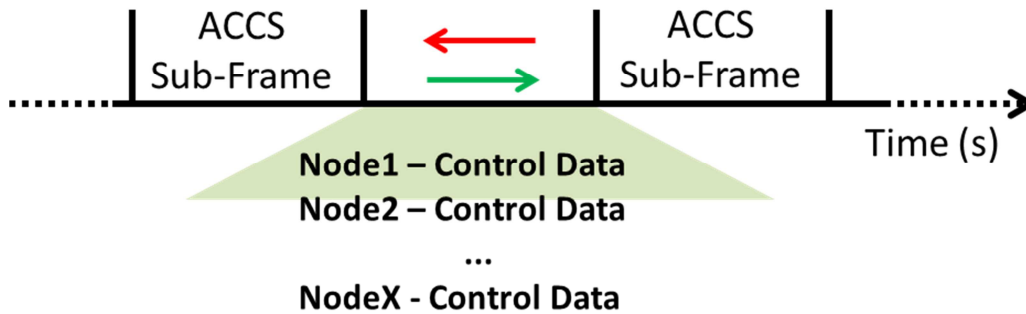
Figure 25 - B2-2-1 SCC sorting for SCC selection

### 3.2.1.4 Control channel

The control channel is used by the eNBs to exchange control data during the BCC and SCC selection process: in the demonstration testbed, it is implemented with TCP socket connections over the WiFi backhaul network connecting all the nodes.

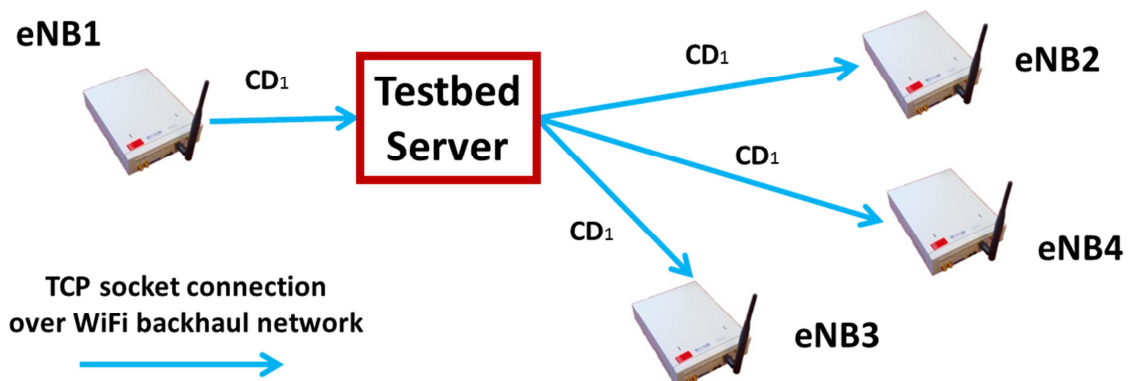
At the eNB side, a communication component provides interfacing with the testbed server that acts as a router of control data among the nodes.

During the ACCS execution process, control data are delivered on a sub-frame basis. On the practical point of view this means that all active eNBs in the network are able to send and retrieve all generated control data within a single ACCS sub-frame.



**Figure 26 - Data exchange over the Control Channel**

Figure 20 describes how the communication process among eNBs, occurs over the control channel. All testbed nodes are synchronized through NTP protocol and have common framing reference; every ACCS sub-frame each eNB transmits a single control data unit that is broadcasted to the other eNBs by the routing server (Figure 21).



**Figure 27 - Routing of control data over the backhaul network**





### **3.3 ACCS Simulation implementation**

This section provides details on the simulation methodology of some of the ACCS procedures, namely the model used for the signalling between (Femto) eNB and the model of the resources allocation.

These are provided in order to highlight the simulation requirements and give a better understanding of the simulation tool used to evaluate the proposed ACCS concept. It has to be noted, that the actual modelling solutions are not unique and different system-level simulation tools may successfully use different models as long as the outlined requirements are met. The important message is that regardless of the exact implementation, the simulation tool has to capture these main mechanisms in order to be able to evaluate the proposed ACCS and any ACCS-like autonomous carrier based interference management mechanisms.

#### **3.3.1 Signalling between eNBs**

The ACCS mechanism rely on the availability of a low-capacity signalling link between the (Femto-)eNBs. With reasonable assumptions, the exact physical layer of this signalling is irrelevant for the understanding and evaluation of the proposed ACCS mechanisms. For example, in commercial systems this signalling can be implemented either using the LTE/LTE-A X2 signalling link (possibly via Home-eNB gateway). For next generation systems a more advanced over-the-air, broadcast or point-to-point, communication link can also be envisaged.

The main requirements for the ACCS related inter-eNB signalling model are:

1. Every eNB should be able to signal to all other eNBs, or to one selected eNB, its radio resource allocation table (RRAT) and incoming background interference matrix (incoming BIM)
2. Every eNB should be able to signal to one selected eNB indicating specific request on the CC usage (e.g. interference reduction request, etc)
3. The signalling channel should model certain time-delays in order to account for PHY-layer procedures (re-transmission, etc).

#### **3.3.2 Downlink resource allocation**

The resource allocation is another important block in the ACCS simulator. Given the L2-L3 nature of the core ACCS procedures, the resource allocation



needs to be appropriately modelled and the simulation of full time-frequency domain L1-L2 RRM mechanisms can be avoided.

Naturally, because ACCS is primarily a carrier based ICIC scheme the focus is on the frequency-domain resource allocation model. The time-domain resource allocation model is important when considering the bursty traffic load in the cells and the timing aspects of the proposed ACCS mechanisms.

The main requirements for *frequency-domain resource allocation model* are:

1. Frequency domain resources and all available CCs in the system bandwidth need to be modelled, optimally, at the level of PRBs or sub-band (group of PRBs).
2. Power allocation on the frequency domain resources (CCs for DL and sub-band for UL).
3. Labelling and identification of the BCC and SCC type of CC resources. The BCC resources are always available to any of the served UEs.
4. Basic assumption on the eNB specific BCC/SCC mapping to UE specific Pcell/Scell.

*An optional feature* of the frequency-domain resource allocation is the possibility for differentiation between the allocation mechanisms for UEs which support scheduling on only one CC (e.g. LTE Release 8) and for UEs which support scheduling on multiple CCs (e.g. LTE-Advanced); support for potential mix of UE types in the serving cell.

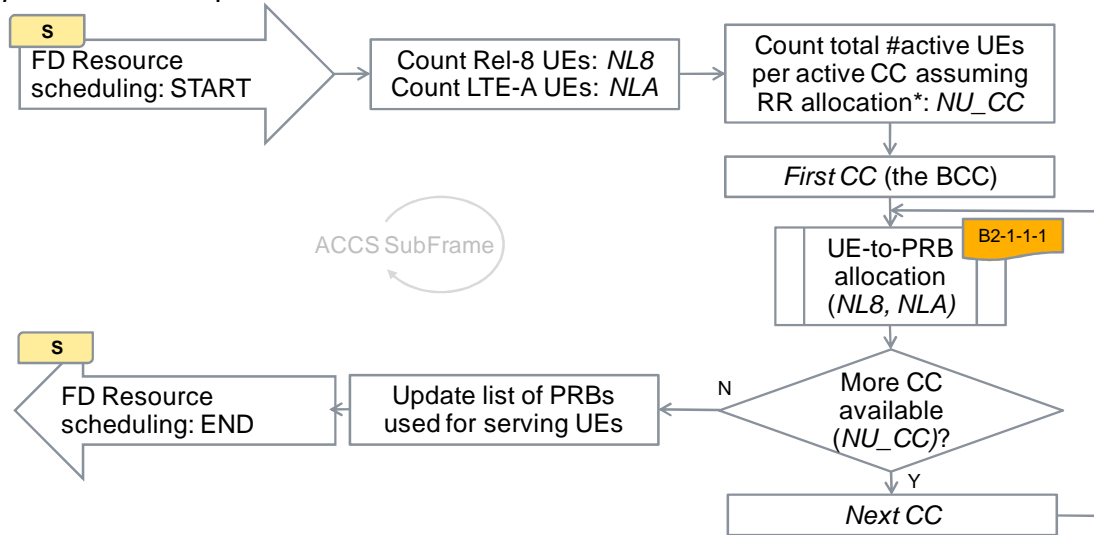
Figure 28 shows the flow-chart of the for *frequency-domain resource allocation model* implemented in our simulator.

The main requirements for *time-domain procedures and resource allocation model* are:

1. Maximum time granularity of *ACCS\_SubFrame* for all eNB and UE related mechanisms. This involves:
  - a. eNB scheduling: PRB/sub-band re-allocation decisions/changes are made only at maximum rate of *ACCS\_SubFrame*; CC re-allocation decisions/changes are made only at maximum rate of *ACCS\_Frame*
  - b. UE traffic model: bursty, finite buffer, traffic model to account only for the changes at maximum rate of *ACCS\_SubFrame*; e.g. simple ON-OFF models, or an exponentially distributed OFF-time traffic model can be used
2. The ACCS decisions (CC allocations, re-allocation, etc) are modelled to be available/possible only at maximum rate of *ACCS\_Frame*

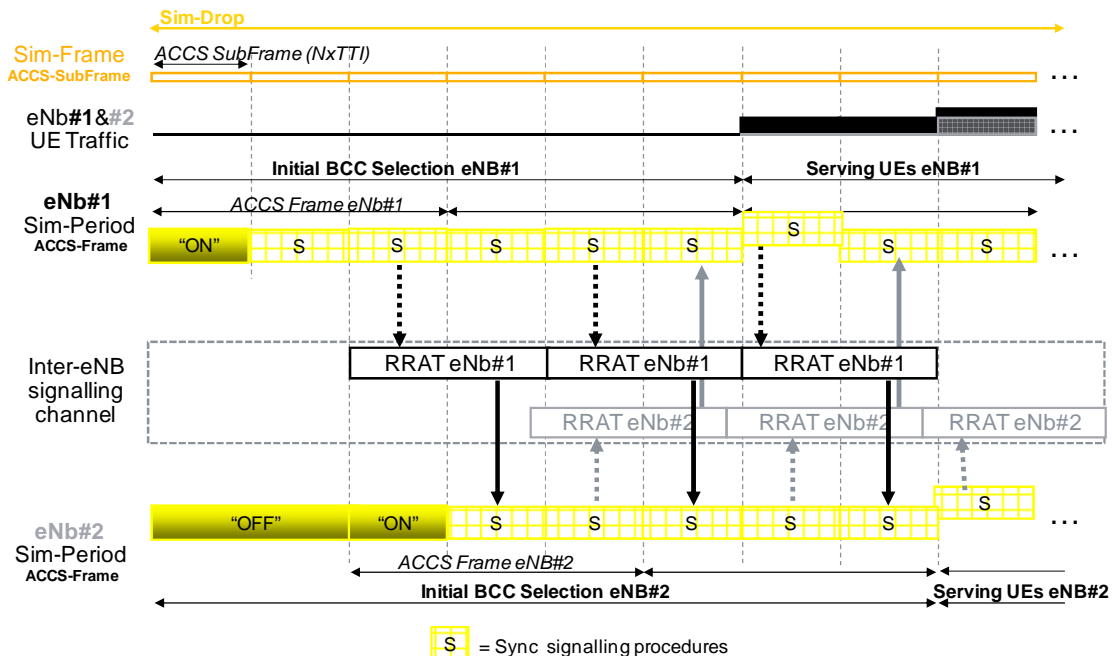


Figure 29 and Figure 30 show the time-line examples for the *signalling procedures* implemented in our simulator.

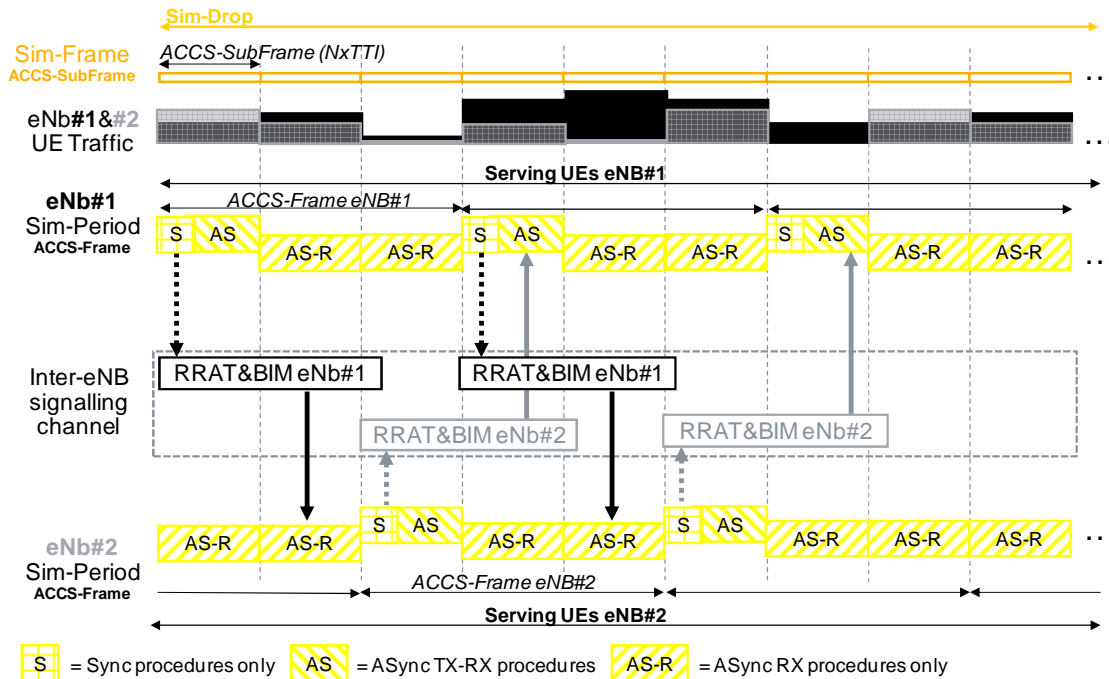


\* LTE Rel-8 UE can be active only one CC; LTE-A UEs are assumed to be active on all available/configured CCs

**Figure 28: B2-1-1 – Frequency domain resource allocation (simulations only).**



**Figure 29: C1-1 – Example time domain signalling procedures during Initial BCC selection(simulations only).**



**Figure 30: C1-2 – Example time domain signalling procedures during Serving UEs (simulations only).**

## 4 Conclusions

### 4.1 CA at RF/PHY Layer

In Section 2.1 we have summarized the development and results of inter-carrier interference reduction techniques, introduced together with simulation results in D4.3, in a real test hardware platform. The results prove that the selected techniques, besides being effectively feasible to be implemented in hardware, provide a gain compared to the situation where no counter-measure is taken to fight against the out-of-band leakages.

In Section 2.2 we have instead introduced the issues that arise in the test and measurement equipments when CA signals need to be generated and analyzed. In particular, in Section 2.2.1 how to optimize the sampling and filtering techniques in generating in hardware and software multi-carrier signals is introduced. An efficient usage of cascade and polyphase techniques is considered for trading off complexity and performance of the method. In Section 2.2.2 how to efficiently perform a FFT for real time signal analysis is presented. Even in this case, the efficient usage of parallelism and cascading is used to



trade off complexity and accuracy of the system, for following the stringent requirements of real-time analysis.

## **4.2 CA at MAC Layer1-Layer3**

In Section 3.1 we have summarized the development and features of the Matlab™ simulator platform and PoC demonstration platform implementation, respectively, both used to investigate the proposed ACCS algorithms. The description highlights the main PoC implementation blocks, addressed in Work-package 5. We described the most relevant details of each the main ACCS blocks using simplified flow-chart diagrams, highlighting the specific simulations (Matlab) and implementation (ASGARD) solutions. In Section 3.2 we detailed the hardware/software solutions including the control plane implementation. In Section 3.3 we described the main characteristic and requirements for an ACCS capable system simulation platform.

The system-level evaluation results using the specific PoC scenarios and characteristics are reported in Deliverable D2.2 (January 2012) and the final results will be included in Deliverable D2.3 (June 2012)

## **4.3 Link to other WPs**

The methodologies presented in this deliverable have strong connections with the other WPs. In particular, the ACCS algorithm is simulated in WP2, while the software radio development performed in this WP has already been made available to WP5 for finalizing the building blocks for the final PoC testbed demonstration. Furthermore, the implementation of the inter-carrier interference reduction techniques has evidenced specific technology issues that will be presented in D5.2.



## 5 References

- [1] FP7-INFISO-ICT-248268 SAMURAI- Work Package 4: Deliverable D4.1  
"Scenarios and requirements for SA", June 2010.
- [2] FP7-INFISO-ICT-248268 SAMURAI- Work Package 4: Deliverable D4.2  
"Intermediate report on SA schemes and implementation feasibility  
study", December 2010.
- [3] FP7-INFISO-ICT-248268 SAMURAI- Work Package 2: Deliverable D2.1  
"Year 1 System Level Evaluation Report", December 2010.
- [4] FP7-INFISO-ICT-248268 SAMURAI- Work Package 3: Deliverable D3.1  
"Intermediate report on MU-MIMO design and implementation  
feasibility study" December 2010.
- [5] FP7-INFISO-ICT-248268 SAMURAI- Work Package 5: Deliverable D5.1  
Proof-of-Concept definitions, December 2010.
- [6] FP7-INFISO-ICT-248268 SAMURAI- Work Package 4: Deliverable D4.3  
"Final report on SA schemes and implementation feasibility study",  
June 2011.
- [7] FP7-INFISO-ICT-248268 SAMURAI- Work Package 2: Deliverable D2.2  
"Year 2 System Level Evaluation Report", December 2011.



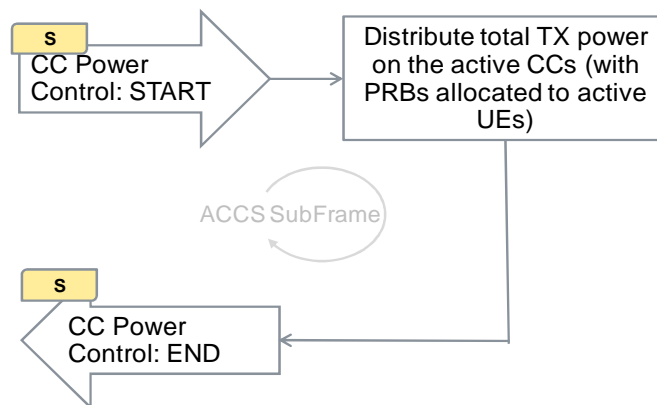
## 6 Appendix

### 6.1 ACCS algorithm for simulation and platform implementation

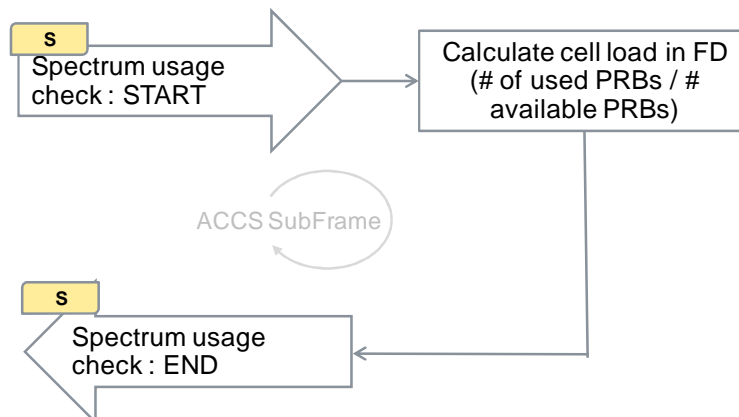
This section provides the additional flow-charts for the main ACCS procedures described in Section 3.1 and Section 3.3.

The UE scheduling related procedures described in Figure 31 to Figure 34 are simulation platform related only.

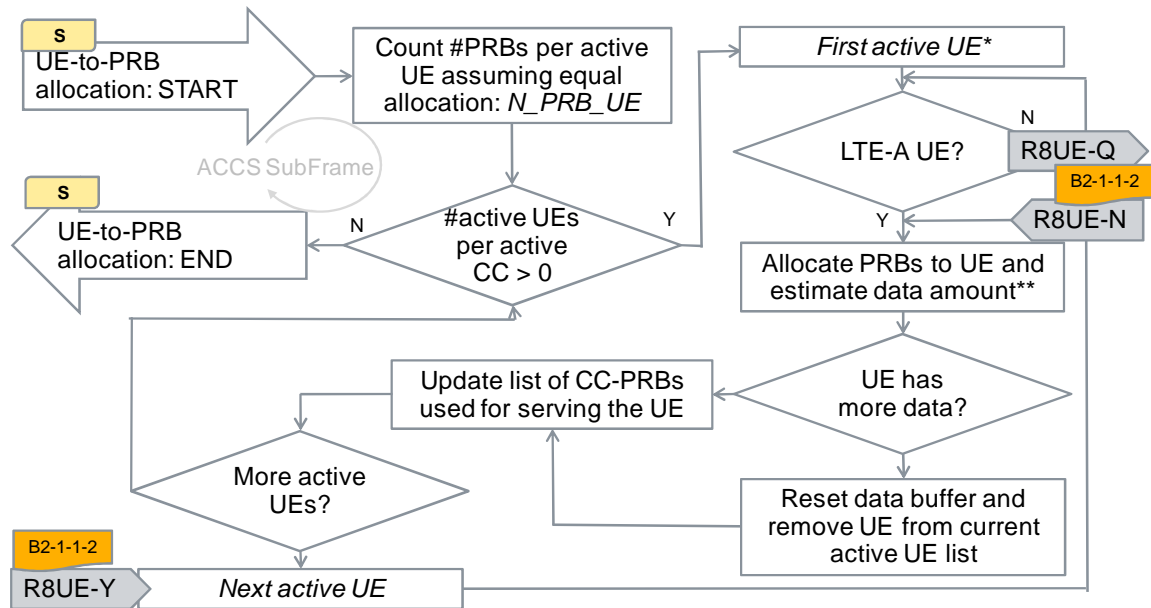
The 'Sort all SCCs' related procedures in Figure 35 to Figure 37 are valid for both simulation and PoC implementation.



**Figure 31: B2-1-2 – CC power control/allocation (simulations only).**



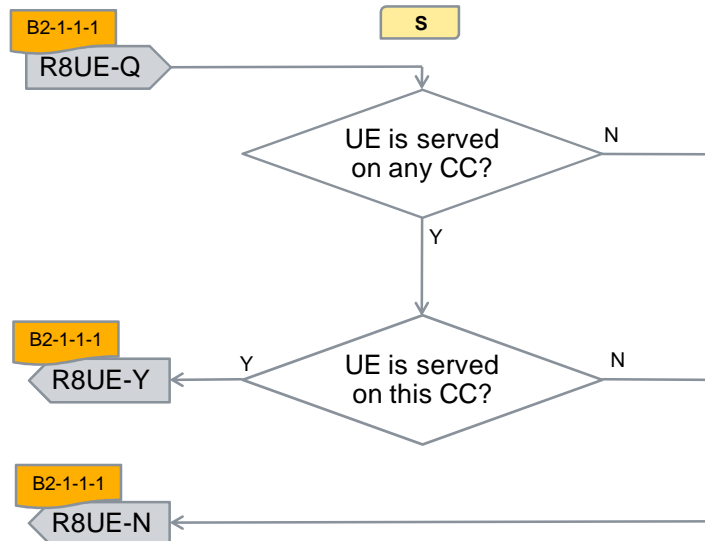
**Figure 32: B2-1-3 – Spectrum usage check/estimation (simulations only).**



\*The active UEs are not sorted and simple RR allocation is used

\*\*The past average throughput per PRB is used in the estimation

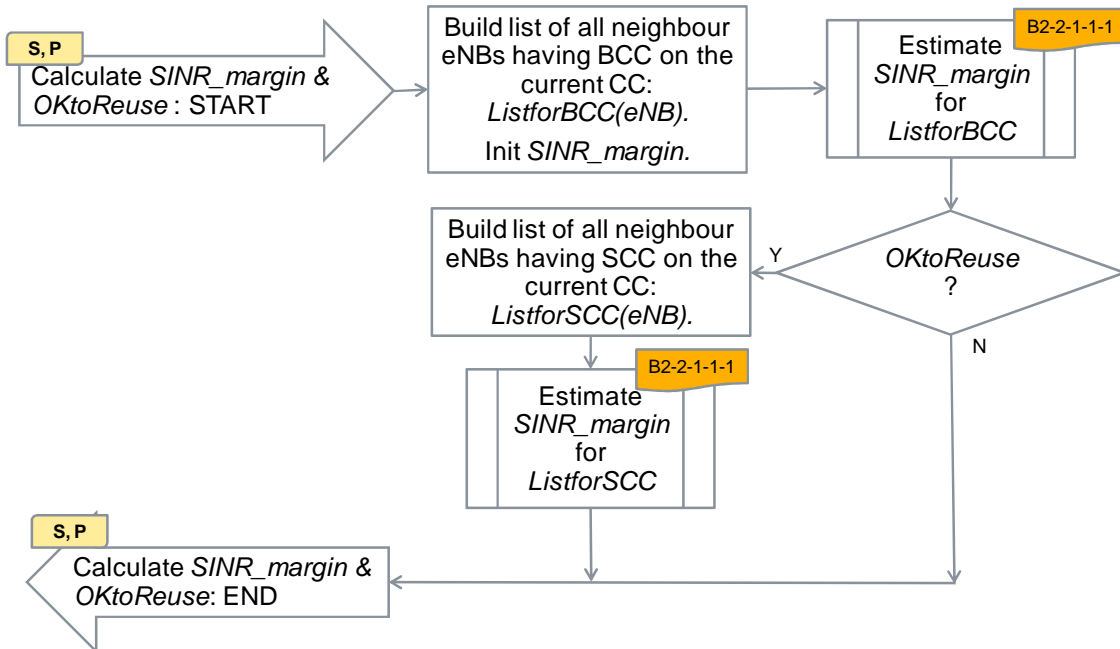
**Figure 33: B2-1-1-1 – UE-to-PRB resource allocation (simulations only).**



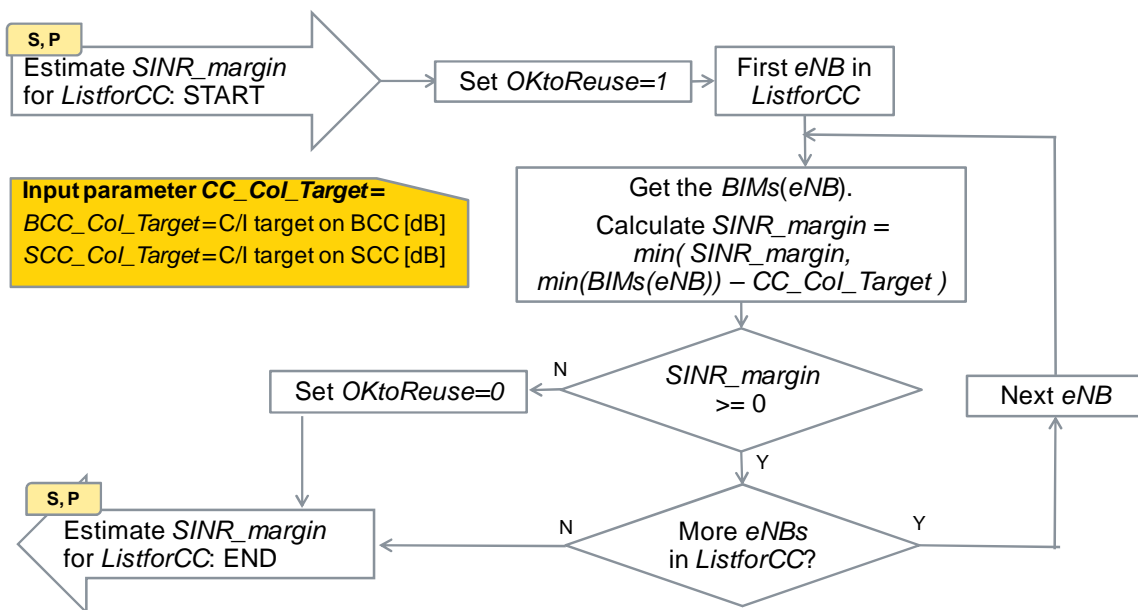
**Figure 34: B2-1-1-2 – UE-to-PRB resource allocation for LTE release 8 UEs (simulations only).**

**Figure 35: B2-2-1 – Sort all SCCs.**





**Figure 36: B2-2-1-1- Calculate *SINR\_margin* & *OKtoReuse* condition.**



**Figure 37: B2-2-1-1-1- Estimate *SINR\_margin* for *ListforCC*.**