1. Publishable summary

The Synaptic project goal is to perform research and development of methods and tools to cope with the design challenges in the next generations of technology processes. The consortium believes that there is a requirement for a design methodology that effectively extracts and preserves logic and structural regularity across the top-down design flow and directly maps the high-level circuit description onto a reduced set of highly-optimized lithography-friendly layout fabrics.

The Synaptic consortium also expects to apply its findings from the research and development phases of the project to commercialise innovative EDA tools implementing a regularity-centric design flow.

In order to achieve these objectives the consortium split the work into five research and technological development (RTD) work packages, together with a dissemination and exploitation work package. The next subsections detail the work performed and describe the results achieved so far for each of these work packages.

Work Package 1: Architectural and System Level

Work package 1 covers the identification and analysis of regular i.e. repetitive structures at the architectural level and abstraction of their functionality for implementation at the structural level.

In the first year we performed a survey of the art of computing architectures and engines found both in state-of-the-art academic proposals and in commercially available solutions eligible for deployment in embedded systems relevant to the Synaptic project; based on it we fully specified two sets of test benches to be used in the other work packages.

The first test-bench, the fine grained one, is a Single-Instruction Multiple-Data architecture based on a set of identical Processing Elements (PE) executing in parallel an operation on different data.

The second test bench, the coarse grained one, instead is based on a streaming architecture developed by STMicroelectronics, where a host processor is connected to a 'streaming engine'.

Both test benches are particularly well adapted to the Synaptic project since they present a lot of regularity and repetitive structures at different levels of abstraction.

Selected parts of both test benches have been fully developed and delivered to the other work packages in the first year.

Work Package 2: Design Synthesis

The aim of this work package is to develop, validate, and provide the design community new regularity-aware synthesis methodologies that, given an application represented in a high-level (or Register Transfer Level) hardware description language (e.g., Verilog or VHDL), perform the following tasks:

- Transformations of the original netlist preserving the RTL inherent regularity, but also driving the logic and topological optimisation such as transistor count minimisation
- Identification of the complex Boolean functions and regular logic structures that can be directly mapped onto feasible, optimized, and regular compound gates and macrocells
- Covering of the original netlist with the identified macrocells and compound gates considering a fully application-specific library generated from the synthesized circuit as well as a general purpose standard cell library extended with a few optimised application-specific compound gates or macrocells.

The technological challenges to be tackled are:

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- Regularity extraction and preservation in logic synthesis
- Enhancement of the logic synthesis process to map to extendable libraries of regular standard cells and on-demand generated regular macro cells and fabrics.

Nangate has specified and is implementing an API that will allow the partners to make use of an industry standard flow to read, manipulate and export design and library data following the same industry standards. Furthermore, the integration of the methodologies developed on this work-package will be based on Nangate's Design Optimizer flow. The general flow of such integration is specified but not yet detailed and implemented.

POLIMI has defined an efficient algorithm for the identification of the Boolean functions on AIGs that are not contained in the initial standard-cell library. It combined this approach with a state-of-the-art algorithm for Boolean matching, based on NPN-transformations. This allows determination of equivalent functions and minimisation of the number of cells to be effectively generated.

UFRGS has specified an algorithm for circuit partitioning, based on KL-cuts, that is the basis for the netlist synthesis. This algorithm identifies multi-output blocks, which can directly represent complex cells to be created in WP3 or a pre-processing scheme for speeding up the identification of compound gates. As a result, it produces the Verilog gate-level netlist of the input design.

The work package 2 will progress beyond the current state of the art through the development of tools and methodologies which extract regularity at the structural level and use this to drive the optimised generation of application specific custom Boolean functions. This approach will overcome the limitations of traditional synthesis methods which rely on a standard library alone.

Work Package 3: Cell Design

In work package 3 the Synaptic consortium is developing techniques and methodologies for the creation of logic and memory elements employing regular physical structures. The focus in the first year of the project has been on two tasks: (1) Circuit Synthesis for non series-parallel (non-SP) CMOS Logic Cells and (2) Layout Synthesis under Regularity Constraints.

The objective of non-SP circuit synthesis is to generate optimized transistor networks from Boolean equations, exploring techniques beyond the industrially widely adopted complementary series-parallel transistor network topologies. UFRGS has achieved partial results for this task with the development of circuit synthesis algorithms based on binary decision diagrams (BDDs), enabling the automatic synthesis of bridge network topologies from Boolean expressions.

The goal of layout synthesis under regularity constraints is to develop algorithms for cell layout considering different levels of regularity constraints. During the first year of the project ST Italy carried out a thorough study in order to demonstrate that by implementing application-specific Boolean functions using compound gates it is possible to achieve significant area saving and delay reduction against traditional standard cell-based physical implementation. Nangate has proposed a regularity constrained cell layout generation flow, with the development of specific regularity-aware algorithms for transistor placement, intra-cell routing and port placement. In the scope of the same task UPC has explored two regular cell architectures: (1) Via-Configurable Transistor Array (VCTA): an extremely regular fabrics and (2) ALARC (Adaptive Lithography Aware Regular Cell): a more conventional regular cell with design restrictions imposed by lithography limitations.

Work Package 4: Metrics

In work package 4 the aim is to evaluate regular proposals developed in other work packages and compare the results with a conventional design flow. The evaluation considers area, timing, power and lithography distortion. During the first period, benchmarks identified in WP1 have been described at RTL level by Thales and ST. These benchmarks are then prepared for physical implementation following a standard design flow in order to serve as reference to regular flows

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developed in the project. Physical implementation and characterization of these benchmarks will take place during the second period.

While these benchmarks are still in development, some open source designs were implemented and characterized by Leading Edge during the first period using early versions of regular layout cells developed in WP3 (by Nangate and UPC). This activity provided early feedback comparing area and timing of regular layout versus current ST cell library and gave first ideas of what to improve in terms of regular cells area.

Also in this period the impact of several transistor netlist design styles on cell characteristics was studied by UFRGS. The project aims to evaluate the use of non-series-parallel (non-SP) networks as a way to reduce transistor count, and the study performed in WP4 showed the differences and impact of SP and non-SP networks.

Finally, regarding lithography evaluation, Imec defined the litho process variability aware methodology for the target 40nm technology to characterize SRAM variability. UPC worked during the first period with the open source FreePDK45 lithography kit while ST prepared the simulation setup of the target 40nm technology that will be used for logic design. FreePDK simulations allowed us to identify relevant effects and how to counteract them with pattern regularity. Lithography simulations using the target 40nm technology are planned for the second period.

Work Package 5: Dissemination and Exploitation

The main objective of this work package (WP) is to cover project awareness and dissemination actions both externally and internally. In addition the work package will cover planning of exploitation and technology transfer activities in order to ensure adoption of project results in industry practice and further research.

In the initial phase of the project, the WP work will mainly focus on internal and external dissemination (for the European electronic design community) of project objectives and on preparation of the Dissemination and Use Plan as well as on competition analysis with regard to the planned commercial exploitation of project results after the end of the project. In the advanced stages of the project, all appropriate means and dissemination channels will be used to raise awareness of the project in the partners' organisations and the European industry as well as the research/academia community.

The expected final result of the WP is the dissemination of the project results and the preparation of the commercialisation of EDA tools developed during the lifetime of the project. Successful commercialisation hinges on the awareness and acceptance of an alternative design flow by the design community and the expected result of the dissemination activities includes the widespread understanding of the benefits of regularity-centric design.

Work Package 6: Prototype Tools and Flow

In Work Package 6 the Synaptic Consortium is developing prototype tools and design flows which exploit regularity at all abstraction levels, while ensuring compatibility of these tools with existing industry-standard digital design flows.

In the first year of the project the group has already prototyped and integrated a circuit synthesis tool into the Nangate library generation flow. Furthermore a regularity constrained standard-cell generation flow was defined and prototyped in Nangate Library Creator, enabling the automatic generation of libraries with configurable levels of regularity.

The expected final result of the project is the commercialisation of EDA tools implementing a regularity-centric design flow. Since the proposed flow is intended to augment rather than replace existing design flows it is crucial that the content and format of any generated views must be compatible with industry-standard flows. With this goal in mind Leading Edge has worked in

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cooperation with ST Italy, ensuring that the initial regular reference libraries created by UPC and Nangate are compatible with industrial physical implementation flows.

For further information about the Synaptic project please visit the consortium website in http://www.synaptic-project.eu.

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