Publishable Summary

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1. Publishable summary

The Synaptic project goal is to perform research and development of methods and tools to cope with the design challenges in the next generations of technology processes. The consortium believes that there is a requirement for a design methodology that effectively extracts and preserves logic and structural regularity across the top-down design flow and directly maps the high-level circuit description onto a reduced set of highly-optimized lithography-friendly layout fabrics.

The Synaptic consortium also expects to apply its findings from the research and development phases of the project to commercialize innovative EDA tools implementing a regularity-centric design flow.

In order to achieve these objectives the consortium split the work into five research and technological development (RTD) work packages, together with a dissemination and exploitation work package. The next subsections detail the work performed and describe the results achieved so far for each of these work packages.

Work Package 1: Architectural and System Level

Work package 1 covers the identification and analysis of regularity i.e. repetitive structures at the architectural level and abstraction of their functionality for implementation at the structural level. This includes a qualitative analysis of advantages and disadvantages of different programmable and accelerated complex functions by way of distributed on chip multiprocessing and programmable IPs, done in the first year of the project; the delivery of suitable RTL for the test-benches to be use in the other WPs; and the definition of a regular architecture template description entry level as a way to create an iterative design flow that can span across the functional architectural exploration levels down to the optimized compound gate library definition and implementation for a specific instantiation.

In the last year of the project we delivered the two parametric test benches defined in the previous years; the impact of the microarchitecture implementation of a component on the results given by the tools flow was analyzed and finally the implementation of the prototype tool for the validation of the high-level design flow was completed.

Work Package 2: Design Synthesis

In Work Package 2 the Synaptic Consortium developed and validated a new regularity-aware synthesis methodology that, given an application represented in a high-level (or Register Transfer Level) hardware description language (e.g., Verilog or VHDL), performs the following tasks:

- Identification of the complex Boolean functions and regular logic structures that can be directly mapped onto feasible, optimised, and regular compound gates and macrocells;
- Exploration of the alternative technology variants to identify the most suitable candidates to compose the target library, while discarding (and not creating) the others;

- Covering of the original netlist with the identified macrocells and compound gates considering a fully application-specific library generated from the synthesized circuit as well as a general purpose standard cell library extended with a few optimised application-specific compound gates or macrocells.

In the last period of the project, WP2 main effort has been spent to improve the methodology that identifies Boolean functions preserving regular logic structures (Task 2.1) and in the re-synthesis of the original netlist (task 2.2). The re-synthesis now is capable of handling timing constraints and is able to exploit regular logic structures identified extracted and assessed by the prototype tool developed by Polimi. Additionally, the mapping tool, developed by UFRGS, is able to target the number of good dies per wafer, by using a cost function jointly developed by UFRGS and UPC (for the whole circuit), coupled with metrics for cell printability (developed by UPC).

Work Package 3: Cell Design

In work package 3 the Synaptic consortium researched and developed algorithms, architectures and methodologies to efficiently implement regular physical structures for combinational logic and SRAM blocks.

The layout generation of combinational logic is generally implemented in a two-step flow: (i) circuit synthesis followed by (ii) layout synthesis. The circuit synthesis step is responsible for implementing Boolean functions using transistor networks as the basic building blocks. The layout synthesis receives a transistor network as input, creating polygons implementing transistors and their interconnections according to the rules and layers of a specified technology node.

The focus of work package 3 for circuit and layout synthesis of combinational logic was to implement complex Boolean functions with efficient transistor networks while using regularity constrained architectures and algorithms for layout synthesis. The key idea of this proposal was to eliminate the density penalty imposed by regularity with the generation of complex Boolean functions not usually available in commercial standard-cell libraries.

The consortium explored cell layout architectures with a range of strategies considering different density versus regularity tradeoffs. The results for combinational logic cell layout point to promising improvements in cell density (up to 55% cell area reduction) for regular layout architectures when compared to a non-regular implementation of the same functionality using cells from a base library.

The design of regular SRAM cells is also an essential part of the physical design flow implementation, and the same regularity constraints applied for the combinational logic were considered for designing memory cells. The consortium designed and analysed four SRAM cell layouts: a classical SRAM reference design (non-gridded, industrial standard) and three gridded designs with different levels of regularity constraints, matching the constraints explored for the combinational logic. The designs were compared in terms of density (cell area) and key electrical characteristics. The results show that SRAM designs implemented respecting the regularity constraints used for logic development in the Synaptic project remain competitive when compared to best in class non-regular industrial designs.

Work Package 4: Metrics

In WP4 the work by the consortium partners is directed to the evaluation of the new synthesis tools developed in the project in terms of area, performance and regularity. To this end, the

Synaptic methodology has been applied to a set of circuit benchmarks, and the obtained physical design has been characterised and compared to the same benchmarks implemented using the standard design tools and flow.

In previous periods (M1 through M24) tasks T4.1, T4.2, T4.3 were completed providing the required benchmarks ready for physical implementation, a regularity metric, and an evaluation of cell in terms of the netlist style, respectively.

In this last period of the project (M24 through M39) the remaining tasks T4.4 and T4.5 have been completed.

T4.5 finished in M27 according to plans. The purpose of this task was to extend a framework for statistical memory analysis to incorporate the impact of layout restrictions in SRAM implementations. The methodology for evaluation takes into account device models, variability data, layout, and/or circuit-level netlist, to compute timing, area, power and yield aspects. The framework is used to benchmark and compare to unrestricted SRAM cell layout styles.

T4.4 had the objective to evaluate the implementation of the benchmarks defined previously in terms of area, timing, power and regularity. A first batch of results was delivered in D4.5 in M27 including the evaluation of the reference implementation and the implementations with the methodologies developed up to that point. Since tool development in WP2 continued through the following months, it was decided to update the results in a final deliverable (D4.6 in M38) that includes the complete methodology of the project. In this last deliverable, a newly developed regularity metric based on the evaluation of lithography distortion and its impact of yield was also used.

Work Package 5: Dissemination and Exploitation

The main objective of the WP is to cover project awareness and dissemination actions both externally and internally. In addition the WP will cover planning of exploitation and technology transfer activities in order to ensure adoption of project results in industry practice and further research.

The WP work mainly focused its activity on internal and external dissemination (for the European electronic design community) of project objectives and results as well as on competition analysis with regard to the planned commercial exploitation of project results after the end of the project.

All the partners organised the VAMM workshop, “Variability modelling and mitigation techniques in current and future technologies” (http://www.synaptic-project.eu/vamm12/), held on March 16 during the Friday Workshops of DATE 2012.

A PhD seminar in Milan was organised and some Synaptic seminars have been promoted by UFRGS (Porto Alegre, Brazil), by inviting the academic partners to visit the University at Porto Alegre (Brazil).

Dissemination of the project results has been also performed by organizing a booth at Design Automation Conference (DAC) in San Francisco from June 4-7, 2012.

Internal industrial workshops were organised in STMicroelectronics and Thales where the main results of the project were presented and discussed. A four-page press release explaining the Synaptic project results was developed and it will published by the ST Legal and Communication Departments.

Like previous years, the scientific results of the project were published in journal, workshops and conferences. Exploitation plans have been prepared by each partner and by the consortium as a whole.

Work Package 6: Prototype Tools and Flow

In Work Package 6 the Synaptic Consortium has developed prototype tools and design flows which exploit regularity at all abstraction levels, while ensuring compatibility of these tools with existing industry-standard digital design flows.

During the third year of the project WP6 effort has concentrated on the integration of the tools developed in the Synaptic project into a homogenous design flow. The resulting flow has then been used for implementation of the four principal Synaptic benchmarks as well as several implementations of a multiplier block. The use of the tools in a complete design flow and analysis of the subsequent results enabled the Consortium to identify key areas for improvement in the Synaptic tools. New versions of the tools have subsequently been developed and integrated into the design flow, adapting the flow as necessary, and the Synaptic benchmarks have been re-implemented to ensure that the tool modifications produce the desired improvements within a flow context. This iterative process has enabled the Synaptic Consortium to produce a stable design flow which is capable of producing designs employing regularity techniques in order to reduce variability and increase yield without incurring the area penalty usually associated with geometric regularity.

The expected final result of the project is the commercialisation of EDA tools implementing a regularity-centric design flow. During the third year a prototype of such a design flow has been implemented using the Synaptic tool suite and extensively proven using the Synaptic, and other, benchmarks.