MultI-coRe, multi-level, WDM-enAbled embedded optical enGine for TErabit board-to-board and rack-to-rack parallel optics

project presentation

www.ict-mirage.eu

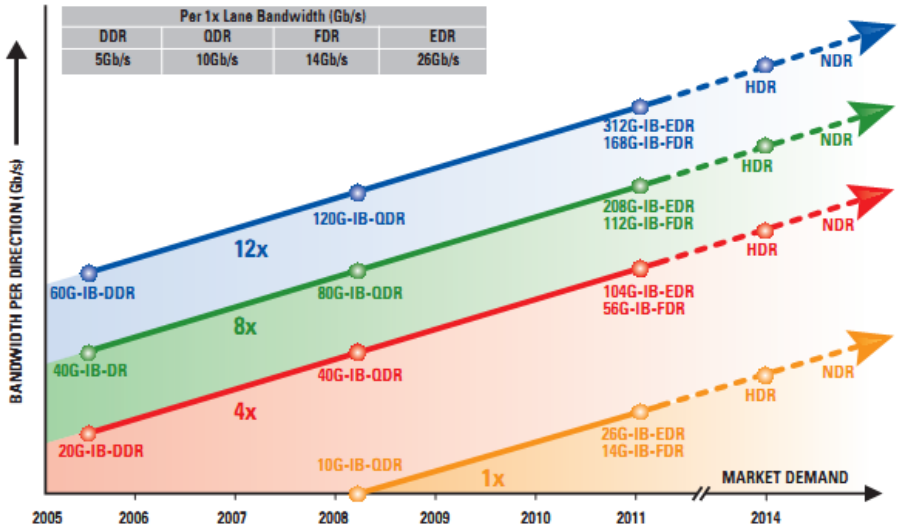
SEVENTH FRAMEWORK PROGRAMME

The team

- **Institute of Communications and Computer Systems – National Technical University of Athens (GR):** Project coordinator. Silicon chip design, component characterization and system testing
- **AMS AG (AT):** wafer bonding, 3D electronic-photonic integration
- **OptoScribe Ltd (UK):** multicore fiber glass interfaces, pigtailing
- **Technische Universität München (DE):** 40 GHz CWDM VCSEL arrays
- **Interuniversity Microelectronics Centre (BE**): transmitter & receiver electronics for multi-level modulation, self-alignment of active chips on 3D stack
- **Aristotle University of Thessaloniki (GR):** system-level modeling, silicon chip design, component characterization
- **AMO GmbH (DE):** 8” SOI line development, optical wafer fabrication

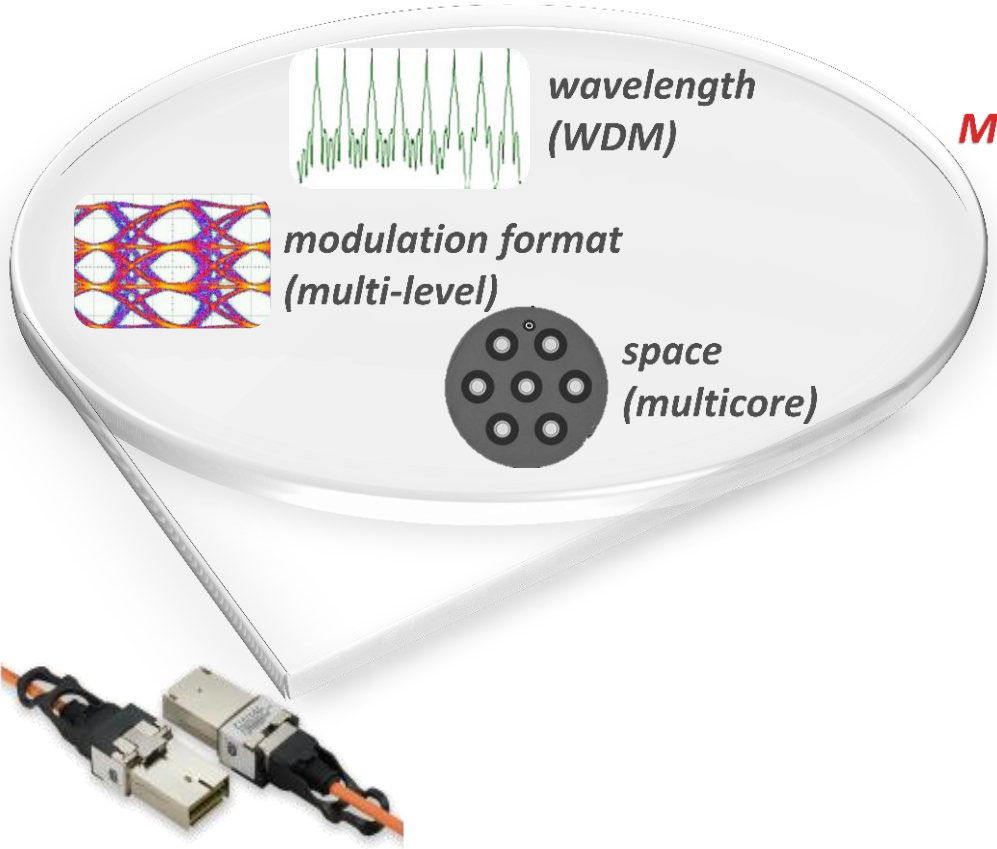
Optical Interconnects

- new applications require instant access to vast amounts of information
- data centers are becoming the “hot spots” of the internet!
- surging demand is pushing current parallel optics technology to its limits

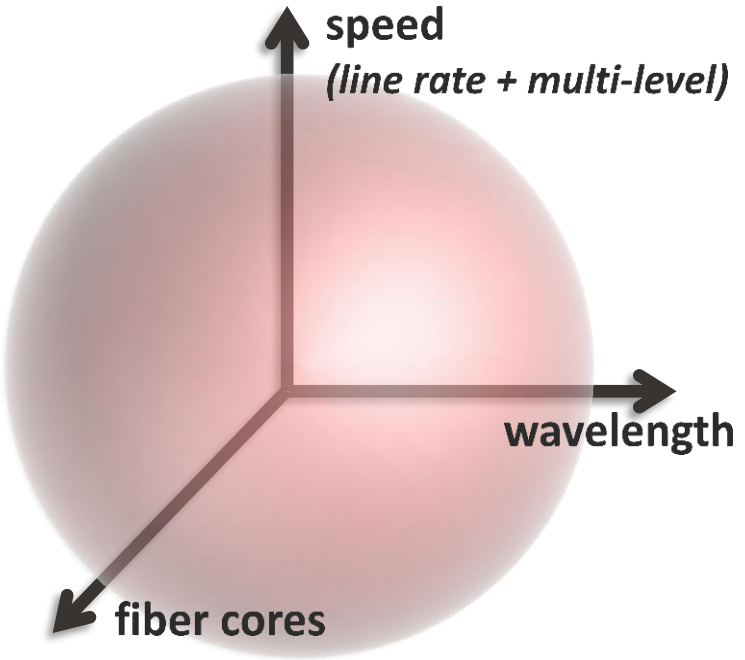


Our vision

- scale line rate to 40 G
- introduce new degrees of parallelization to upgrade data density
  - ☑ *WDM* ☑ *multi-core* ☑ *multi-level*
- fabricate a **Terabit capacity Active Optical Cable (AOC)**

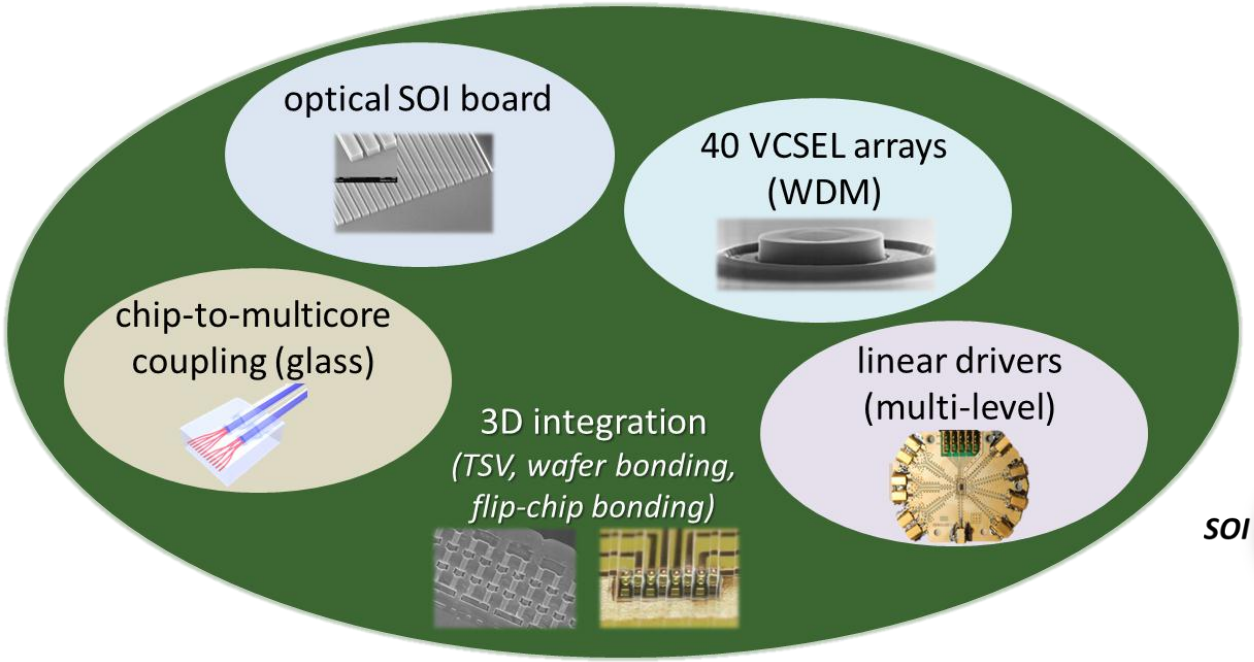


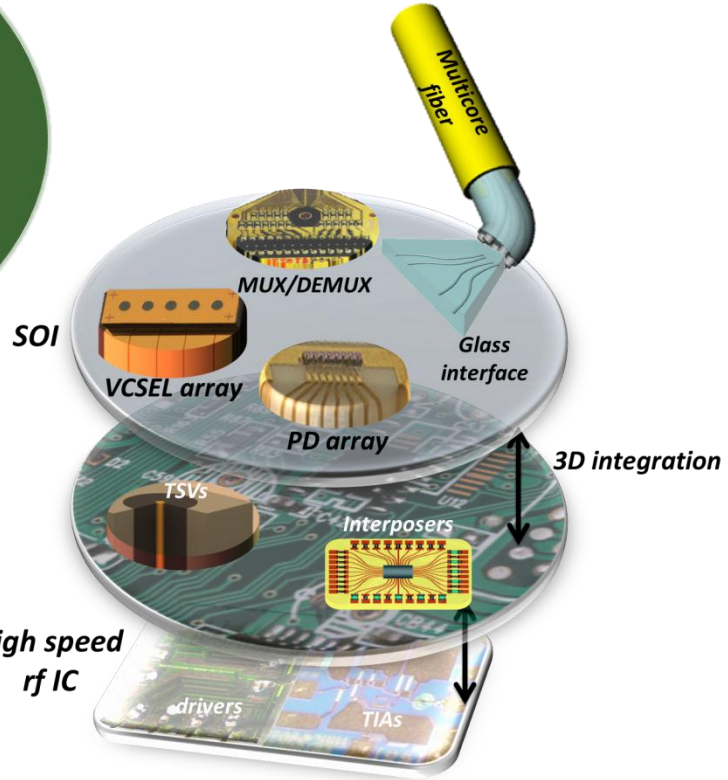
MIRAGE increasing the AOC performance envelope



How?

3D electronic/photonic integration





MIRAGE 3D integration ecosystem

Objectives (I)

MIRAGE is developing:

silicon photonic-electronic platform for 3D EPICs

- ✓ *SOI photonic board: leverage functionality of Si photonics*
- ✓ *electronic drivers (Si based)*

short-cavity VCSEL arrays

- ✓ *40 Gb/s modulation bandwidth*
- ✓ *monolithic CWDM arrays at long wavelength (C-band)*

advanced methodology for industry-compatible 3D assembly & packaging

- ✓ *40 GHz through silicon vias*
- ✓ *wafer bonding, flip-chip bonding with self-alignment*

low cost multicore-fiber coupling

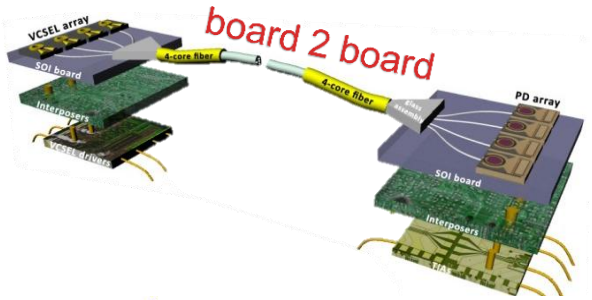
- ✓ *3D glass waveguide (in plane coupling)*
- ✓ *vertical SOI coupling*

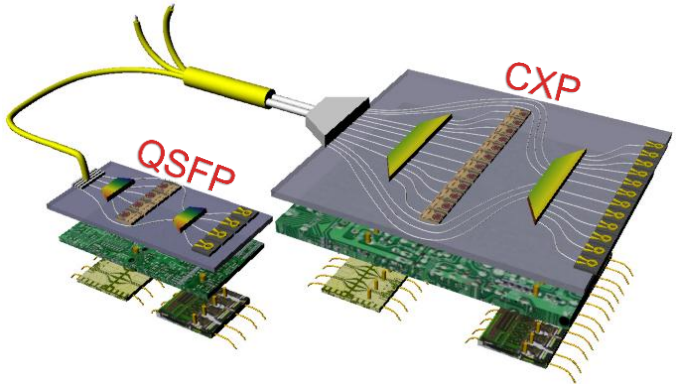
Objectives (II)

MIRAGE is using the developed "optical engine" to:

fabricate application-specific components

- ✓ *208 Gb/s board-level interconnect*
- ✓ *320 Gb/s QSFP AOC*
- ✓ *960 Gb/s CXP AOC*
- ✓ *CXP to 3xQSFP breakout AOC*





evaluate in datacom environments

- ✓ *board-to-board*
- ✓ *rack-to-rack*

Exploitation plans

MIRAGE targets a reliable, industry-compatible integration technology for value – added products.

MIRAGE functional platform will streamline the convergence of photonic integration technology for multiple application fields

Strong & broad exploitation:

Markets

- *datacom*
- *telecom*

Products

- *VCSELs*
- *chip-to-multicore coupling, multi-core fiber fanouts*
- *high-speed linear electronic drivers*
- *AOCs, board-to-board interconnects*
- *highly-functional 3D electro-optic components*

Exploitation routes (+spin-offs)

MIRAGE addresses the entire value chain:

Contact

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