Semiconductor Equipment Assessment Leveraging Innovation

Reporting Period 1 June 2010 – 31 May 2011

PROJECT PERIODIC REPORT
Publishable Summary

Covering Deliverable D19.2.2 Periodic activity report and

D19.2.5 Periodic management report

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[1] Usually the contact person of the coordinator as specified in Art. 8.1 of the Grant Agreement.

[2] The home page of the website should contain the generic European flag and the FP7 logo which are available in electronic format at the Europa website (logo of the European flag: http://europa.eu/abc/symbols/emblem/index_en.htm logo of the 7th FP:

1. Publishable summary

SEAL is an integrated project consisting of 17 equipment assessment sub-projects in the area of semiconductor manufacturing equipment. The assessment themes are equally spread amongst processing and metrology equipment, heading beyond the current state-of-the-art both for More Moore and More than Moore applications. The strategic objective of SEAL is to effectively combine efforts, resources and expertise in the joint assessment of novel equipment supported by cross-cut R&D dedicated to the identified needs of the assessment sub-projects. In the following the objectives and status of all sub-projects after 12 months are reported separately. There is not report on SP9 because this SP will start after months because of some changes. A contract amendment is in preparation.

The address of the public project website is: www.seal-project.eu

Sub-Project 01 - R&D

Sub-project 1 covers cross-cut R&D for the equipment assessment activities in SEAL. The main objective is to identify common problems and challenges amongst the SEAL sub-projects, and to work on overall and sustainable solutions. Several common challenges have been identified during the proposal setup of SEAL and were clustered in five R&D areas, reflected in dedicated work packages in SP1. New activities were identified in the first 12 months of the SEAL project and added to the areas of this sub-project. All workpackages started their activities, the following topics were already processed: predictive maintenance, plasma simulation, discrete event simulation, cost of ownership calculations and equipment assessment metrics and metrics. Furthermore, a set of 'virtual' seminars as well as real training events will be organised. The first real training event is planned during the SEMICON Europe in October 2011. The identification of new topics, tasks and challenges will be continuously discussed with all partners.

Sub-Project 02 – EUVMTP

The objective of the sub-project 02 is the qualification of the MaskTrack*Pro* tool EUV mask cleaning tool platform with respect to intrinsic cleanliness of specific EUV equipment units, capability of particle removal on the backside of EUV masks used in an EUV scanner, and the reliability of the hardware and software of the equipment meeting high volume EUV manufacturing. In preparation of the intrinsic equipment qualification specific methodologies for qualifying mask equipment in a wafer ded-

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http://ec.europa.eu/research/fp7/index_en.cfm?pg=logos). The area of activity of the project should also be mentioned.

icated fab environment were defined. After identifying most common types and sources for particles on the backside of an EUV masks initial cleaning tests showed cleaning capability for this specific contamination type of backside particles. Detailed investigations of the contamination disclosed that not all detected defects, like surface damage, can be addressed by cleaning. Repair would be required but is not considered possible due to the unpredictable nature of damage. The cleaning therefore got a preventative role, as to avoid that such damages can happen. The expected sub-project outcome will be an improved readiness of the 3 collaborating partners on the specific aspect of EUV mask cleaning. Because the results are given additional visibility via IMEC's Advanced Lithography Program, also other chip manufacturers and stakeholders will benefit in their preparation for the implementation of EUV lithography into production of integrated circuits.

Sub-Project 03 - A2D2

In SP3 subproject, the objective for partners (Fraunhofer/Adixen and Jenoptik) is to enhance the laser based wafer dicer, successfully demonstrated by Jenoptik, in order to decontaminate the substrate of the diced wafers from water residues (side effect of the TLS approach). The water removal process is a challenging issue, currently performed at atmospheric pressure by suction. A Vacuum drying module is proposed in order to obtain a fully efficient and short drying process. In the first year, technical assessment of additional Adixen drying process, based on vacuum process, was prepared and then performed regarding specification requirements from TLS equipment and compared to other current solutions.

Sub-Project 04 – FISMA

The integration of a new flexible illumination system into mask aligners and the investigation of its impact on the lithographic performance are the objectives of this sub-project. At the beginning, Reinhard Microtech's constraints of the current lithography process were discussed and the test pattern, which has to be printed with the new illumination optics, was defined. Simulations were made at SMO and FhG IISB to evaluate the error sources. The most relevant parameters gained with the help of these simulations were exposure gap, angular spectrum, resist sidewalls (for different resists) and depth of focus. A pre-selection of illumination geometries was made for some specific applications. In order to optimize critical lithography steps, FhG IISB calculated OPC structures which were implemented onto the mask pattern and as a consequence the process window was considerably enhanced. The new illumination system was installed at RMT and is ready for the first test prints (D4.4.1) which will occur in the next months.

Sub-Project 05 – MAPA

The objectives of this sub-project are to support the industrial development of the massively parallel electron beam technology developed by MAPPER to address lithography for 32nm half pitch resolution (22 nm logic node). Furthermore mask making capability will be assessed for future integration into mask maker tool. The assessment of MAPPER technology will be done against end users requirements. This sub-project will also assess the necessary infrastructure in terms of process, data flow and proximity effect correction as well as mix and match industrial strategy.

Sub-Project 06 - E2O

The reduction in thermal budget by low-temperature oxidation of silicon is of very high importance especially for future but also for current technology nodes of silicon semiconductors. The novel application of high density microwave plasma induced electron charge enhanced oxidation of silicon in the E2O sub-project opens a new window for rapid and high quality low temperature processing. Within the first 12 month of the project the new microwave plasma oxidation equipment was designed, manufactured and tested successfully. The first basic results achieved on the alpha-tool are adequate to the data from the laboratory scale equipment. Although, the shipment of the alpha-tool to Fraunhofer-IISB in Erlangen is delayed 6 month the planned sub-project duration of 24 month is currently not jeopardized.

Sub-Project 07 - TCB300

Temporary Wafer Bonding is becoming a key process in thin wafer handling and processing for 3D integration technologies. In the sub-project 7, the consortium of IMEC, SUSS MicroTec and STM is working on the equipment and processes evaluation and optimization for temporary bonding and debonding. In the first 12 months of the sub-project ST and SUSS evaluated and defined the requirements for the equipment and processes. The equipment for temporary bonding, a SUSS XBC300 fully automated bond cluster and two semi-automated debonder were installed by SUSS at IMEC in Belgium. After installation and initial testing of the equipment an existing process based on the adhesive HT10.10 from Brewer Science has been evaluated and qualified for 200mm as well for 300mm wafers. Initial debonding experiments were successfully executed. In the upcoming months, the slide-debonding will be further examined. Also the equipment will be upgraded (Hard & Software) in order to be prepared for the evaluation and qualification new processes.

Sub-Project 08 - Plasma-Trans

Plasma doping or PIII systems are slightly replacing beamline ion implanters in applications where low energy and high doses are needed (poly & contact doping, USJ). Thanks to the previous SEA-NET Program, IBS has developed and installed a PIII tool in the CEA Clean Room. This machine, named "PULSION-nano" is dedicated to the doping of Ultra Shallow Junctions on 200mm/300mm wafers and has proved its efficiency in the 100 V- 10 kV acceleration Voltage range allowing good homogeneity, no metal contamination, and high throughput. The aim of this project is to open the applications field of PULSION thanks to equipment modifications allowing wider pressure range, better control of plasma spectrometry and energy distribution, higher acceleration voltage and wider range of temperature during implantation. Thanks to the collaboration with CEA-LETI and ST Crolles, the interest on 2 applications will be studied: defect engineering and CMOS imager (3D doping and post processing backside doping with low thermal budget).

Sub-Project 10 – IMDI

The objective of this sub-project is to asses a new inspection technology developed by Nanda Technologies. The innovative inspection approach uses a combination of bright-field and unique dark-field illumination of the whole wafer to inspect every wafer at 100% of the surface in one shot. It achieves high sensitivity of down to 0.5 µm at a high throughput of up to 120 wph. Furthermore, the unique optical design allows detecting a broad range of defects including new defects in 3D/TSV processing. In the first phase of the project, the system was installed and optimized for the process monitoring and characterization of the 3D/TSV development line at IMEC. It was used to detect unique defects in the bonding and thinning process steps. The system was optimized by creating specific inspection recipes and by optimizing image processing algorithms. The process control of thinning and grinding steps could be successfully demonstrated. Furthermore, a new method for "residual silicon thickness" measurements above copper nails was developed based on unique optical characteristics of the inspection tool.

Sub-Project 11 – NFmicroPCD

The objective of this sub-project is to carry out a feasibility study on a carrier lifetime measurement tool, which is capable of working on patterned / product wafers, using near-field microwave probing technology. This technology was originally developed to measure the dielectric constant on low-k materials. However with modifications a novel tool is created so that lifetime related information can be measured as well. To do this, an excitation source must be added to the tool for the generation of minority charge carriers, and new evaluation methods have to be developed. After the modifications

on the tool, measurement capabilities on different contaminated and non-contaminated epitaxial layers will be tested.

Sub-Project 12 – WISDoMP

Mechanical wafering process steps (sawing, grinding, lapping) become crucial for achieving wafer qualities meeting most advanced IC design rule requirements. Target of this sub-project is the development of a metrology system capable of meeting future wafer and IC requirements. The concept is to apply white-light interferometry to assess the full surface topography of 300 mm wafers after mechanical processes at to detect defects and characterize surface nanotopography as well. The FRT MPR300 TTV prototype tool has been successfully installed in the production line of Siltronic AG. After recipe development and demonstration of gauge repeatability and reproducibility, matching to established reference tools was verified with very good linearity and good matching. For shop floor integration a SECS interface for remote control of dimple, thickness and nanotopography measurement was set up. Improvement of the nanotopography assessment is currently in focus of all participants.

Sub-Project 13 – MCEB

Multi Column E-Beam inspection is becoming a reality by making progress on all the fronts defined in this project. Two (single column) systems (with the same column technology) are installed and working in a GlobalFoundries (GF) fab. A team of AMIL and GF engineers are working together on VOLTAGE-CONTRAST applications. Issues are discussed, assigned and tracked on weekly basis. The main issues are drifts correction, calibration, failures and software coverage. In parallel, a team of AMIL is working on tasks of PHYSICAL DEFECTS detection and THROUGHPUT. Physical defects detected by detecting its edge; the effort is to reduce background-diffracted electrons while increase edge-diffracted electrons. Combined ICT and AMIL teams are working on the multi-column tool reliability and stability. A 5-column tool is installed in AMIL labs and used to improve Contrast-to-Noise Ratio (CNR).

Sub-Project 14 – NaREA

The content of this sub-project addresses the assessment of a superior detector for high resolution x-ray analysis. Delivered data will be the film thickness of the functional films as well as information about chemical compositions in a combined measurement. Count rates are expected eight times higher than compared to a conventional tool. This can bring a great advantage of fast and easy analysis to the end-user especially in the cases where optical tools are less practical due to non-specular

reflecting surfaces. During this first year period the detector prototype was implemented at the R&D site and tested for performance and operation with the reference samples produced by the end user. Complementary investigations of layer thickness are running, and identification of critical microscope parameters which will have the highest influence on the results, was performed. The system is up and on duty. First cross cut activities will be performed.

Sub-Project 15 - M4

The objective of the assessment is to take the prototype high-resolution mass metrology module and build a production-ready, modular 300mm tool complete with two measurement modules, wafer automation and mini environment. Once installed in the imec R&D site, this tool will be used to assess the use of high resolution mass metrology at 20nm technology node and below. Originally planned as a 30 months project, SP15 has been extended to 36 months due to delays in the final design and specification of the production tool. These delays are solely due to resource limitations brought on by the increase in business at Metryx. So far the project is unable to report results, though significant progress has been made in the design of the prototype tool. The design of the prototype is not part of this project. At the end of the project a fully assessed high resolution mass metrology tool will be commercially available to the semiconductor industry. This will enable rapid and efficient process monitoring helping to increase yield and drive down costs for semiconductor device manufacturers.

Sub-Project 16 – WAAVE

The aim of WAAVE proposal is the development of an innovative acoustic characterization tool for wafer level inspection (200/300 mm) providing a very high resolution capability. Additionally a novel characterization method will be developed containing the capability of detecting and characterising mechanical properties of buried layers and interfaces. Up to now, the three different technologies which will be inside this innovative tool have been evaluated with specific samples, and they are now merged into one unique machine. The main target is the inspection of 3D integrated devices and monitoring during the entire integration process (various bonding steps and stacking, etc.). The acoustic inspection tool under development will combine several imaging and analysis approaches based on the propagation of alternative acoustic wave modes. This technology will give a very important advantage to the end user for developing their process, material and economic project.

Sub-Project 17 – COMBO

The COMBO project is designated towards the most accurate metrology results, via combining two methods of measurement introduced on KLA-Tencor's Archer™ platform: the first is the common method of imaging based overlay (IBO), the second method is sccatterometry, diffraction based overlay (DBO). KLA-Tencor, IMEC and Micron have been working together trying to assess the advantage of the above use case. The assessment included definition of requirements for overlay metrology in 22nm nodes and beyond, target design and implementation on reticles and R&D wafers, performance analysis and optimal sampling strategies. Using a small number of DBO targets for grid corrections in combination with a large number of IBO targets, spread within the field results in more accurate correctable terms. These terms enable a benefit from the DBO accuracy measurements on the one hand side, and reducing target's footprint within the field by using small IBO targets (which is known to be a high important issue for customers) on the other hand side.

Sub-Project 18 - HPW-ESC

The goal of the sub-project is to develop the electrostatic carrier technology, so that it can be utilized for all relevant processes in a mass production environment. Also in SP18, a handling tool which handles thin and ultra-thin wafers were planned and developed. The actual status of work is the following. The equipment specifications are done. The development and the installation of the tool are finished. The tool was installed in week 24/2011 at Lfoundry. A new T-ESC is available. In July, tests at Lfoundry will start after the ACU3000 Prototype is installed. SP18 is behind schedule. It is unavoidable to extend the sub-project for another 12 months. The new timeline is presented under 2.3 (project management).

Sub-Project 19 – Management

Important for the SEAL project is a strong and collaborative management of the Integrated Project to establish a fruitful and tight collaboration in the project covering in total 17 assessment and cross-cut R&D projects. A powerful and flexible management structure helps to manage the ambitious objectives of this Integrated Project with such a high number of sub-projects, the high number of assessment sites, the high number of SMEs and the high number of users from both IC industry and industrially oriented research institutions. The coordinator is Fraunhofer IISB. The coordinator is supported by the Management Board and by the Steering Committee especially in strategic issues and technical road mapping. After the first year all management structures have been set-up and the work in all sub-project were guided in a good way.