ConceptGraphene

New Electronics Concept: Wafer-Scale Epitaxial Graphene

Small or medium-scale focused research project

WP4 Spin transport devices

Deliverable 4.4 “Report on FET/spin-FET devices on epitaxial graphene”

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Deliverable Summary

In this report we show the gate response of epitaxial graphene Field Effect Transistors (FETs). Top gate devices with a AlO_x gate dielectric can be used to tune the charge carrier density and access both electron and hole transport regimes. We observe hysteresis and low robustness against high gate voltages, which can be explained by defects in the oxide layer.

Additionally, we observe hard to remove thin polymer films between the graphene-contact interface, arising from cross-linked resists from subsequent lithography steps in combination with oxygen plasma etching. This results in high resistive and unstable contacts, which greatly limit the spin polarization of the Co contacts. Therefore, we did not succeed in measuring spin transport in gated epitaxial graphene devices (spin-FETs).

1. **Introduction**

Since 2007 the Groningen group has successfully pioneered experimental work on spin transport in exfoliated graphene. Graphene is a promising material for spintronic devices, such as spin transistors or spin qubits, due to its high spin relaxation lengths of ~2µm at room temperature.[1] We are interested in spin transport properties such as the spin relaxation length, the spin relaxation time and the spin diffusion coefficient. Also we study the fundamental nature of spin relaxation mechanisms. So far, influence of the commonly used SiO_2 substrate seems to limit charge carrier mobility and thereby presumably spin lifetimes. Changing to epitaxial graphene gives us the opportunity to study the effect of the SiC substrate and the buffer layer on spin transport, and compare these results with previous results obtained on exfoliated graphene. Furthermore it clears the way for graphene based spintronic devices and applications in the future.

In month M18 of the ConceptGraphene project we reported on deliverable D4.1 “Report on spin transport in graphene on SiC”. In that report we described successful spin injection in en transport through epitaxial graphene on SiC(0001). We refer to report D4.1 and reference [2] for a more extensive description of the fabrication process and measurement techniques.

In month M24 we reported on deliverable D4.2 “Comparison of spin-valves of graphene prepared with different techniques including graphene on SiC”. In that report we compared the spin transport properties of different graphene systems: epitaxial graphene on the Si-face and on the C-face of SiC, quasi-freestanding epitaxial graphene by H-intercalation and exfoliated graphene on SiO_2 and on hexagonal boron nitride (h-BN).

2. Report on Report on FET/spin-FET devices on epitaxial graphene

Here we will show charge transport measurements in epitaxial graphene Field Effect Transistors (FETs). We will show the typical gate response of top gated graphene channel. So far, we did not succeed in measuring spin transport in gated epitaxial graphene devices (spin-FETs).

2.1 Methods

A possible way of getting control over charge and spin transport in epitaxial graphene is through the electric field of a gate. Especially interesting is the gate dependent spin transport in the graphene-buffer layer system, to test the consistency of the localized state model described in reference [3]. Additionally we would like to study spin transport at different charge carrier densities in both the electron and hole regime.

The proposed device geometry of a spin-FET consists of a non-local spin valve with a gold (Au) top gate (figure 1). A ferromagnetic cobalt (Co) contact is used to inject a spin current in the graphene channel, which can be detected at the other Co contact. The spin current in the middle graphene region between the Co contacts can be controlled by applying an electric field with the use of the top gate. The thin oxide layer below the Co contacts acts as a tunnel barrier for avoiding conductivity mismatch.

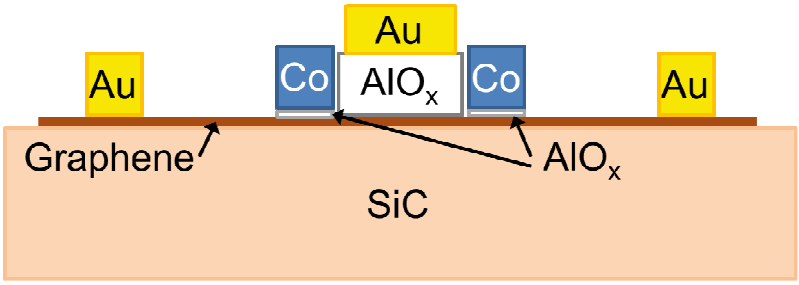

Figure 1. Device geometry of an epitaxial graphene spin-FET. A spin current can be injected into the graphene channel by one of the Co contacts and detected at the other Co contact. The spins in the transport channel can be affected by applying a voltage between the Au top gate and the graphene.

Figure 2 shows an epitaxial graphene FET with only Au contacts and a spin-FET with both Au and Co contacts, which can be used for spin transport experiments.

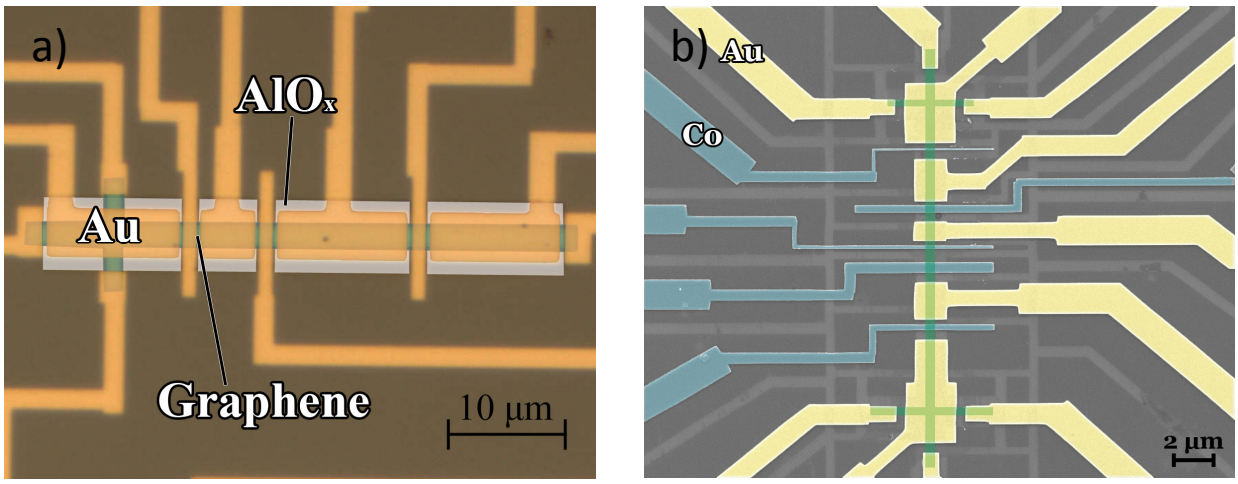

Figure 2. a) Optical microscopic image of an epitaxial graphene FET. For clarification, colors are added to the gate dielectric (white) underneath the contacts and on top of the graphene strip (green). b) Colored scanning electron micrograph of an epitaxial graphene spin-FET.

2.2 FET devices

We investigated charge transport in epitaxial graphene FETs (figure 2a) with 2 types of gate dielectrics: AlO_x (type I) and cross-linked PMMA using high dose e-beam exposure (type II). The gate response is shown in figure 2a and 2b. Breakdown of the gate occurs at ~ ±30 V and ~ ±20 V for type I and II respectively. The CNP cannot be reached with type II device due to a low breakdown voltage. In type I devices the CNP is reached only at high negative voltage. During such a sweep a hysteresis effect shifts the CNP from -24V to -11V. The increasing hysteresis at higher gate voltages can be explained by the presence of mobile charges. Applying high gate voltages results in gradual but irreversible changes to the resistivity and an overall decrease of the device quality.

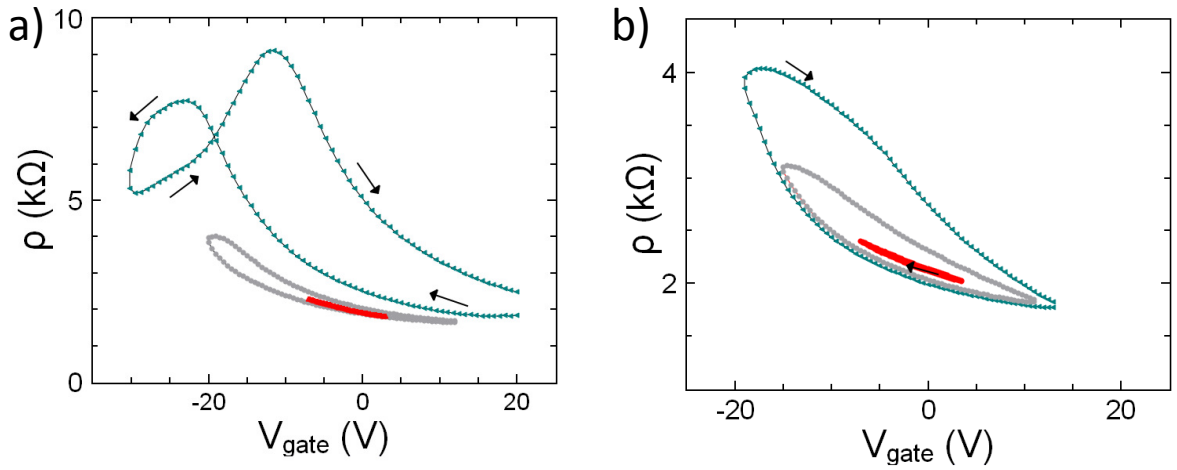

Figure 3. a) Typical gate response of a type I epitaxial graphene FET, with AlO_x gate dielectric. A hysteresis effect is observed at higher voltage ranges. b) Typical gate response of a type II FET, with cross-linked PMMA as gate dielectric. The gate response shows similar hysteresis as in type I. Breakdown occurs before the CNP is reached.

Further investigation of gate response in type I devices by varying the sweep rate confirms that the device quality greatly decreases after electrically stressing the gates for longer periods of time (figure 4a). Using the Hall-bar geometry we can see the effect on resistivity (figure 4b) and charge carrier density (figure 4c). After applying varying gate voltages for longer times, the devices show increasing resistivity and abnormal magnetic field dependence of the Hall resistance. This can be explained by the deterioration of the gate, which cause unpredictable results due to additional current paths through the gate dielectric.

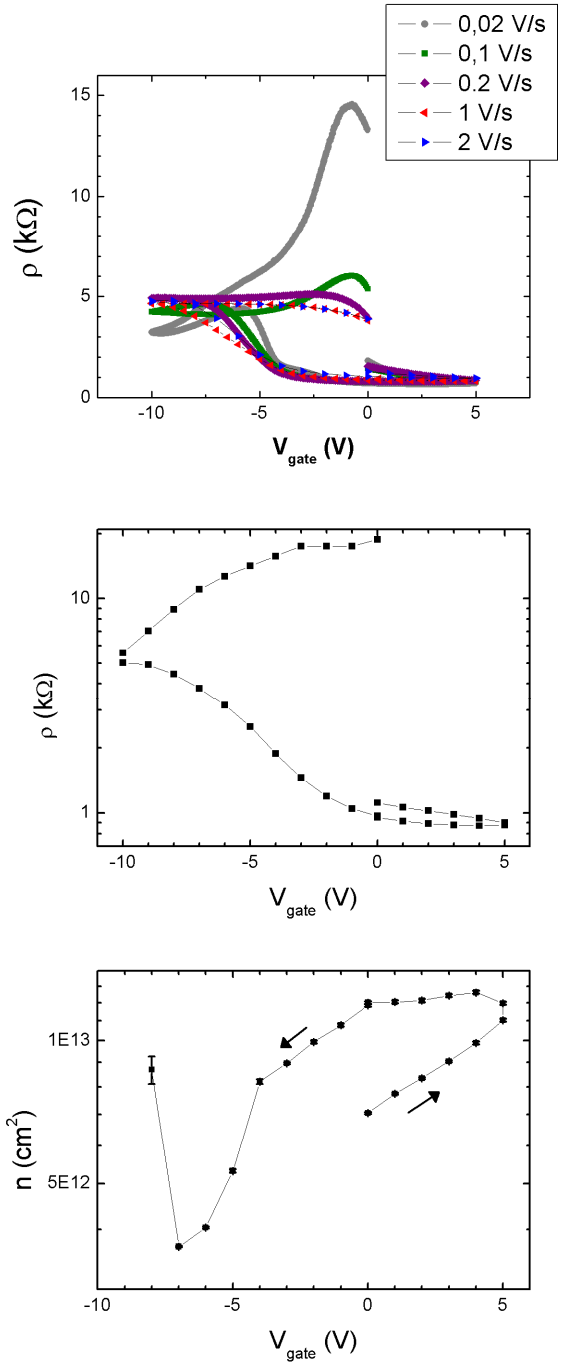

Figure 4. a) Gate response of a type I FET at different sweep rates, showing the effect of electrically stressing the gate for a long period of time. b) Similar gate response as in a) using a very slow sweep rate of ~0.1 V/min. c) Charge carrier density at every measurement point in b). The charge carrier density is obtained from measurements of the Hall effect. Towards the end of it this measurement the carrier density is less well-defined due to unpredictable magnetic field dependence of the Hall resistance

The measured hysteresis effects can be explained by the imperfect crystal structure of the AlO_x, deposited using e-beam evaporation, which is known to create defects such as oxygen vacancies. Using atomic force microscopy (AFM) and scanning electron microscopy (SEM), we found that a thin layer of resist residue (figure 5a and 5b) can have an additional effect in causing the observed hysteresis in gate response.

This thin layer probably consists of cross-linked polymer, caused by the use of several types of photo and e-beam resists during fabrication. The cross-linking can occur during reactive ion etching with an O_2-plasma, a fabrication step which is necessary to create the small patterns from the large area epitaxial graphene. The film follows exactly the shape of the etched patterns and is only visible using AFM or SEM imaging, and only after attempts to remove the layer, thereby partially folding or cracking it (figure 5). We tried to remove the layer using chemical treatment, flood exposure by deep-UV lithography and furnace annealing in Ar/H_2 flow, none of which was fully successful. The film causes high resistive contacts, with a high spread in resistance (kΩ – MΩ).

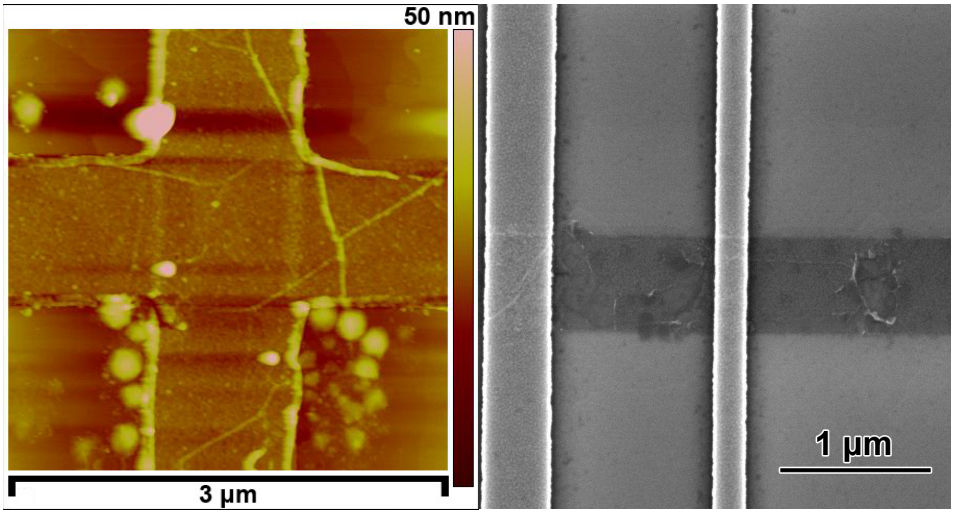

Figure 5. a) AFM image of partially cracked and rolled thin layer of polymer on top of an etched graphene Hall-cross. b) SEM image of polymer remains on a graphene strip.

2.3 Spin-FET devices

The extra fabrication steps that are necessary to fabricate a spin-FET as in figure 1, make the chance of contamination due to polymer remains very high. This results in high resistive and unstable contacts. So far we achieved a low fabrication yield, where only ~10% of the contacts show contact resistances that are acceptable for successful spin injection. Due to problems listed above, we have yet to fabricate a working spin-FET. Our current work is still focusing on cleaner ways of producing top gated epitaxial graphene spin transport devices,.

3. Conclusions and outlook

We investigated epitaxial graphene FETs and spin-FETS for studying spin transport at different carrier densities. We investigated the quality and performances of top gates in two types of FETs with different gate dielectrics. We produced working top gates with an AlO_x gate dielectric that can efficiently operate in the electron as well as in the hole regime.

As yet we have not succeeded to combine gate technology with working spin transport devices. Subsequent lithographic process steps contaminate the graphene – tunnel barrier interface with a thin layer of resist residue. This results in a low yield (< 10%) and unstable tunnel contacts with spin polarizations that are too low to detect any spin transport through the spin-FET channel.

To improve the fabrication process additional testing of different methods for etching the graphene strips is necessary. We are currently trying etching using O_2-plasma at a lower powers, using ion bombardment or using UV-ozone etching. Possible routes

to improve gate performance (decrease hysteresis and increase robustness) can be switching to high-k dielectrics like HfO_x or using photochemical or ionic liquid gating.

4. References

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