ConceptGraphene

New Electronics Concept: Wafer-Scale Epitaxial Graphene

Small or medium-scale focused research project

WP2 Characterization and integration

Deliverable 3.6 "Report on measurements on array of 100 Hall bars"

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Executive summary

A chip containing four arrays of 100 Hall bars, accompanied by other test structures, has been designed, fabricated and electrically characterized. Control measurements on the test structures, consisting of single Hall bars, demonstrated good carrier density uniformity at the level low enough to allow metrological assessment of the whole chip.

However, further inspection has revealed a fabrication fault in the array's structure, which required many more nanofabrication steps for it's fixing. As a result of these extra technological steps, the array integrity has been recovered, yet the carrier concentration in graphene has been severely affected, rising up to 3-4 times. Electrical measurements on the recovered chip demonstrate behavior consistent with the sample design, yet metrological measurements on this sample would require too strong magnetic fields, even with the polymer gate applied. Further efforts will be put to gate the devices and make them compatible with the metrological setup capabilities.

Observation of unintended doping of graphene during nanofabrication is very interesting and important on its own from the point of view of multiple devices integration. It calls for more careful inspection and assessment of existing fabrication steps, which have been considered 'safe' from the point of graphene doping.

Contributors and their input

Epitaxial graphene was grown by partner 6 – Linkoping University.
Device design has been supported by patner 3 – NPL
Device fabrication and initial charachterization has been carried out by parner 1.
Report written by all contributors.

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Deliverable Summary

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1. Sample fabrication

We have previously (D2.3) fabrication of a sample with Hall bar arrays on epitaxial graphene which showed correct scaling of transverse resistance with size of the array. However, quantum Hall regime could not be observed because of too high charge carrier density. One of possible factors responsible for higher carrier density was that photochemical gating was not efficient because densely spaced interconnecting wires affected the thickness of spin-coated polymers used for the gate.

We decided to address this issue together with some other by modifying the design. All CAD drawings of integrated circuits were computer generated, which makes small adjustments to the design easy to accomplish.

The following changes have been made:

- Openings for Hall bars between the interconnecting wires increased from 27x20 to 47x25 μm
- Pattern for the insulation layer has been modified to facilitate lift-off (Figure 2).
- It has been demonstrated that patches of bilayer graphene can lead to increased contact and longitudinal resistance in quantum Hall regime. Therefore, design of a single Hall bar was adjusted based on shape of bilayer patches on the particular substrate, based on the graphene thickness mapping, performed in advance (Figure 1).

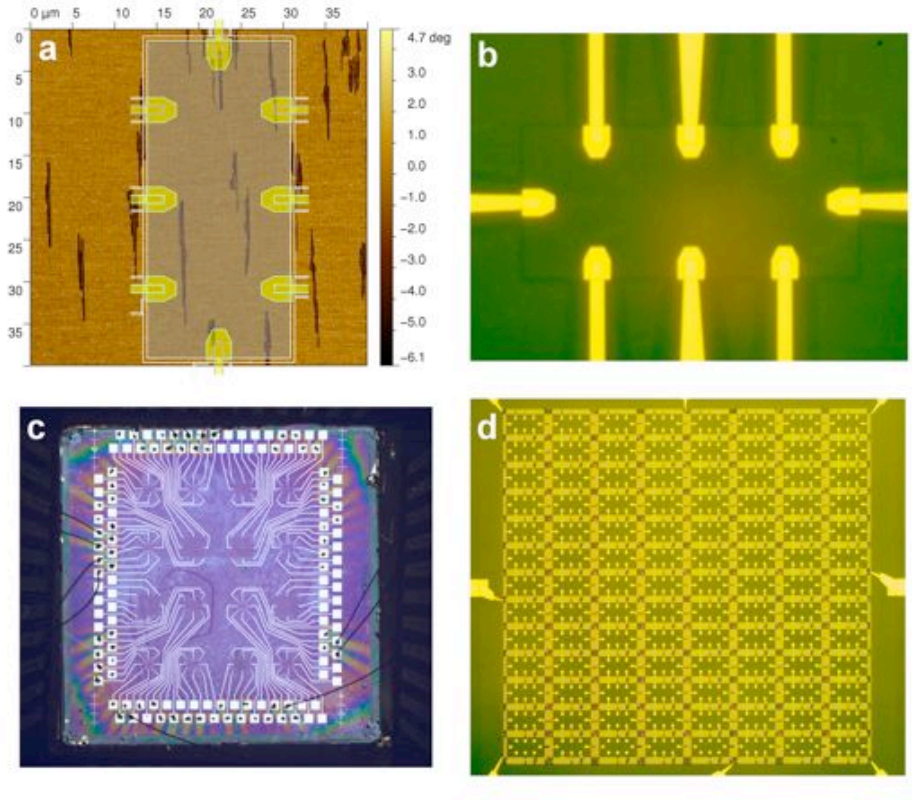

Figure 1: a) Design of a single Hall bar on top of typical AFM phase image showing bilayer patches. All Hall bars were aligned along the terraces and length of a Hall bar is twice the length of the longest bilayer patch observed

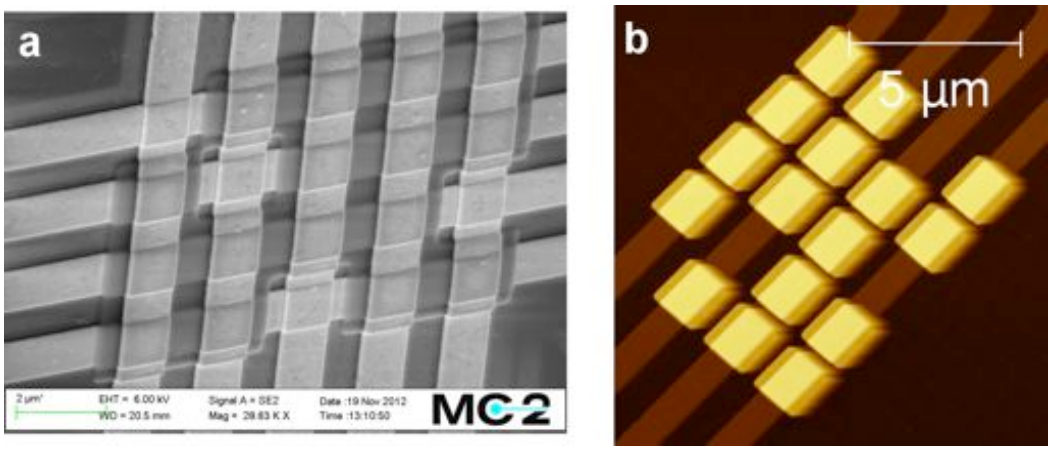

Figure 2: It has been found that design in the form of a continuous layer with openings inside can cause problems during lift-off deposition. Therefore, shape of insulation layer was changed to a set of individual squares. a) SEM image showing the old design of the insulation layer; b) AFM image showing animproved design of the insulation layer.

Apart from changes in the design, fabrication procedure was similar to the one we used for the previous sample.

2. Preliminary electrical characterization of single Hall bars

A total of 16 devices have been fabricated on the chip, as shown in the table:

Device type	amount
Single Hall bar	4
N=4 array	3
N=16 array	2
N=36 array	3
N=100 array	4

In order to assess the substrate quality, preliminary measurements of magnetoresistance, carrier density and mobility on single Hall bars at low temperature were done as an intermediate step before fabrication of the arrays was completed.

Each of 4 Hall bars was measured in a setup shown on Figure 3. A current of 1µA was applied between current contacts 1 and 5. Direction of the current was alternated for each data point, and no significant difference between data for two different current directions was observed. Three Hall voltages between voltage probes 2-8, 3-7 and 4-6, and one longitudinal voltage V_{xx} between probes 2

and 4 were measured. Difference between Hall voltages on different probes on the same Hall bar was insignificant (Figure 4).

Measurements were done in a He cryostat at base temperature 2K in perpendicular magnetic fields up to 9T. No gate was applied, chip was only covered with PMMA to protect in from the environment.

Hall resistance R_H and longitudinal resistance R_{xx} were calculated from Ohm's law, R=V/I; longitudinal resistance was translated into resistivity by $\rho_{xx} = R_{xx}\frac{w}{d}$ where w is width of the Hall bar and d is distance between voltage probes. Carrier density was calculated from linear (low-field) region of $R_H(B)$ curve as $n = \left(e\frac{dR_H}{dB}\right)^{-1}$ where e is electron charge, and mobility was calculated from R_H and ρ_{xx} at low fields as $\mu = \frac{1}{\rho_{xx}}\frac{dR_H}{dB}$. Results for n and μ are summarized in Table 1.

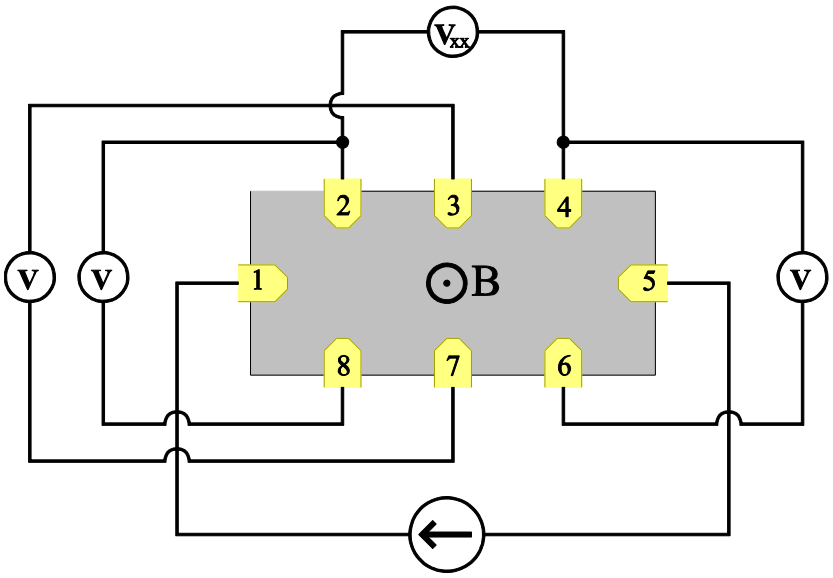

Figure 3: Measurement set-up for characterization

Device #	1	2	3	4
n, 10^{12} cm^{-2}	1.2	1.4	1.4	1.5
μ, $cm^2/V•s$	3700	3800	4200	3100

Table 1: Transport properties of single Hall bars

Figure 4 shows magnetoresistance curves for all 4 single Hall bars. Onset of v=2 plateau is observed at 9T on one structure and is expected around 10-12T on the other three. We expect that photochemical gating would have brought carrier density to a level well bellow 10^{12} cm^{-2}, making it possible to reach the quantum Hall regime at 12T on all structures.

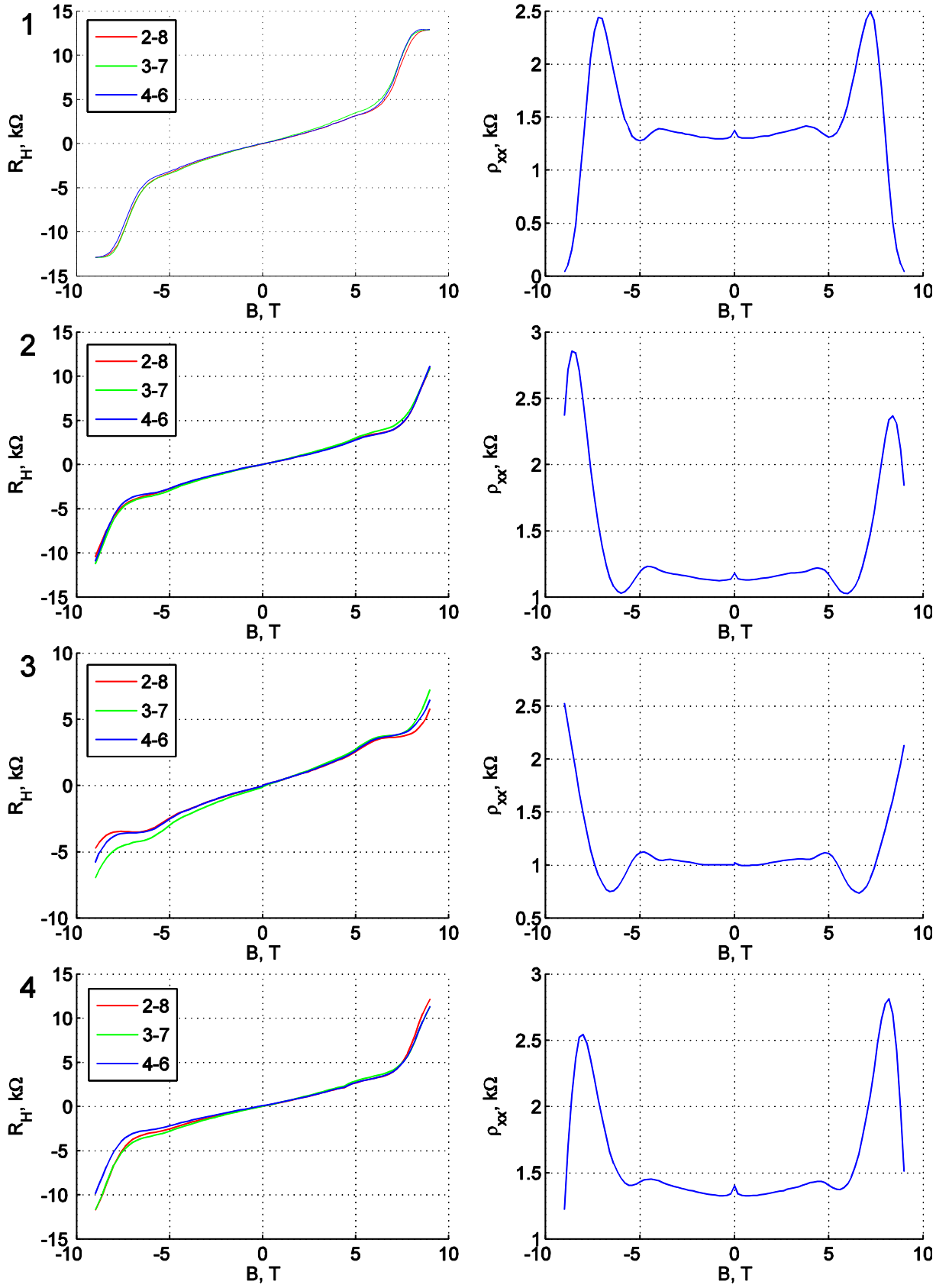

Figure 4: Low temperature (4.2K) magnetoresistance measurements on single Hall bars

3. Electrical characterization of completed devices

After measurements on single Hall bars were done, a few more lithography steps were required to finish the fabrication of arrays.

Because of a lithography error that has caused misalignment in the insulation layer (Figure 5), two extra process steps had to be develop to implement local corrections to already fabricated structures.

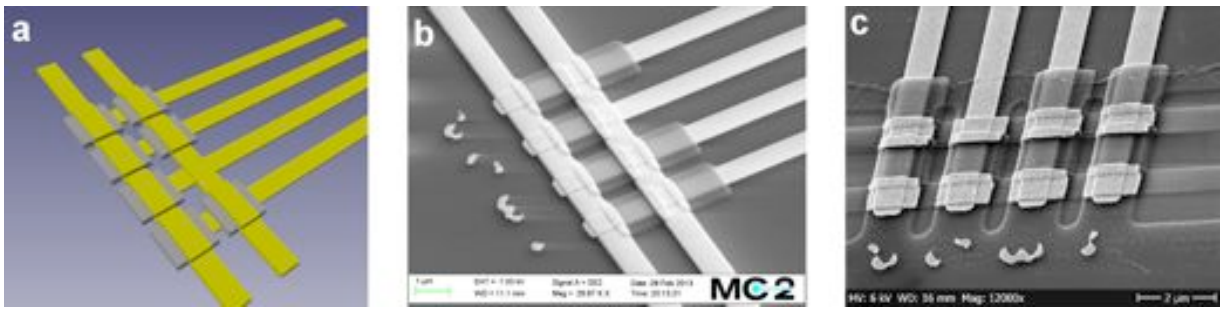

Figure 5: A problem with misalignment: a) designed pattern; b) actually fabricated structure, all the leads are short-circuited because of misalignment in the insulation layer; c) parts of the wires were locally removed by Ar ion milling, new wires were deposited at a later step

After fabrication was finished, longitudinal and Hall resistance was measured at room temperature for single Hall bars as well as arrays. Measurement setup (Figure 6) is similar to the one used for the previous measurements on single Hall bars; one Hall voltage was measured for each structure.

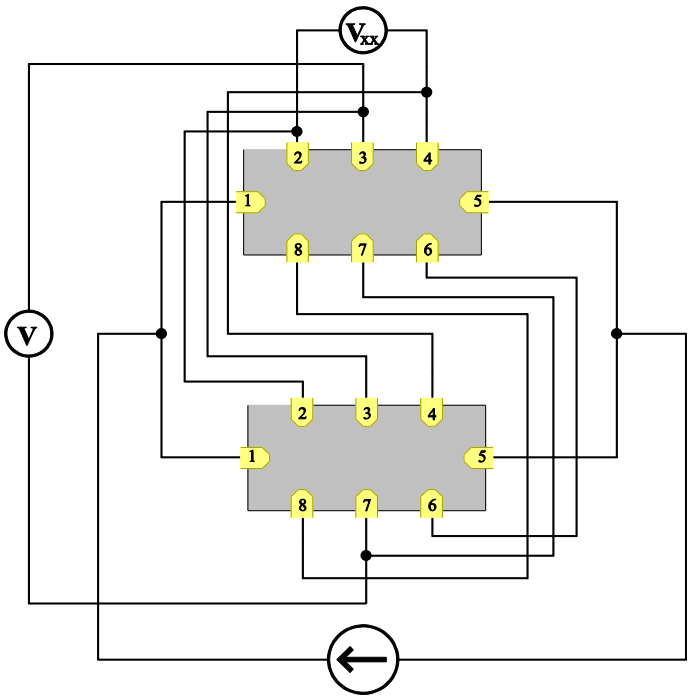

Figure 6: Measurement set up for a parallel Hall bar array (two Hall bars are shown in this example)

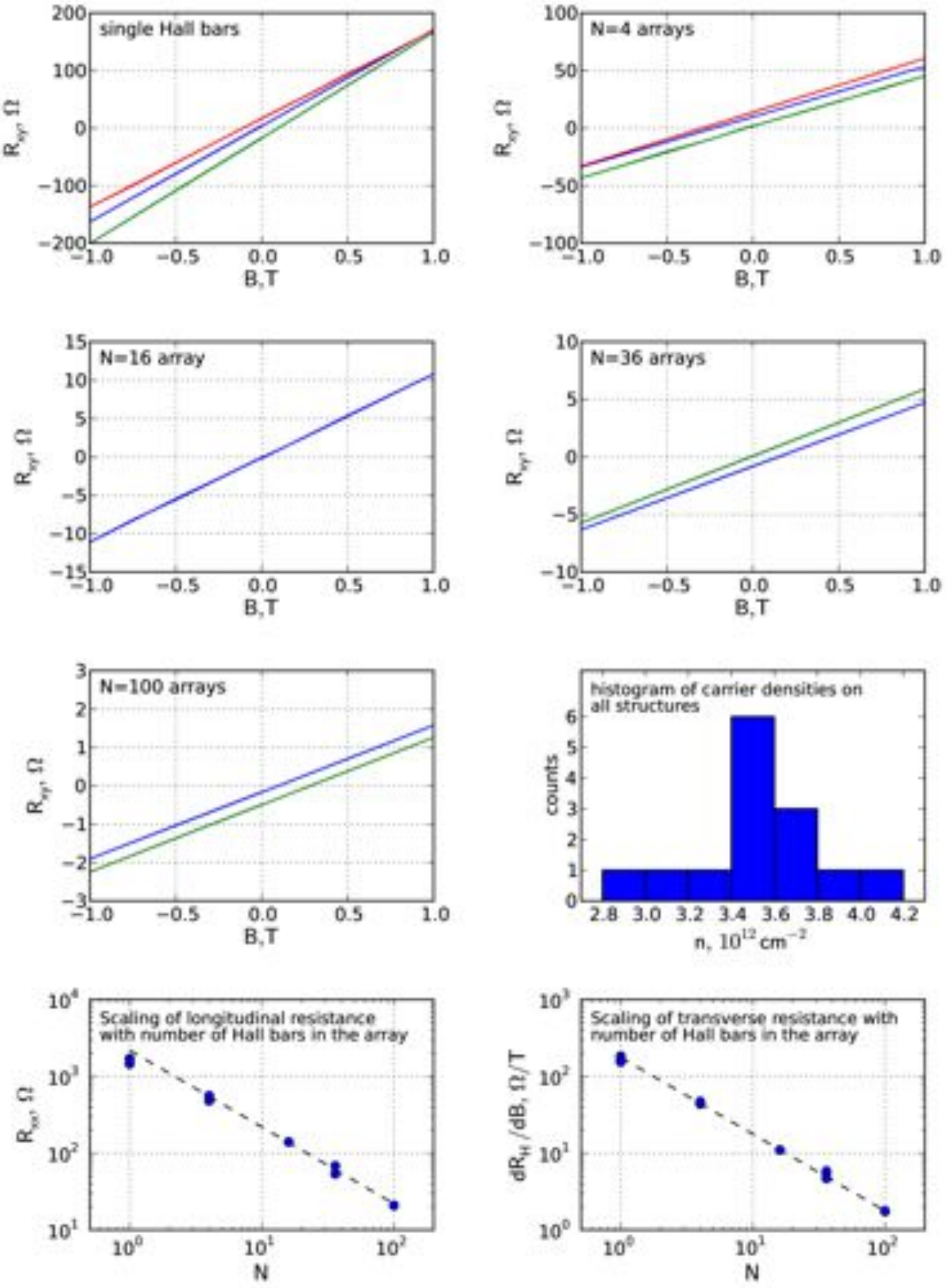

Figure 7: Results of electrical characterization after completing the fabrication

Results of these measurements are summarized on Figure 7. Both longitudinal and transverse resistance scale as inverse number of Hall bars as expected. However, carrier density on all structures, including previously measured single Hall bars, was found to be in the range of $(3\text{-}4)\cdot 10^{12}$ cm^{-2}, which is a clear evidence that the last fabrication steps have caused uncontrolled doping of the substrate. We estimate that even after applying photochemical gate it would require magnetic field of at least 30T to reach quantum Hall regime in these devices. Currently we are trying to implement other gating schemes to bring the carrier density in the structutes within 10^12 cm^-2 limit and to make the device compatible with the merological setup capabilities.