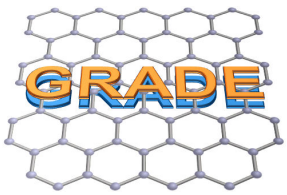

GRADE

Graphene-based Devices and Circuits for RF Applications

Collaborative Project

WP 6

D6.1

DC, S parameter and High Frequency Noise Characterisation of GFET devices

Main Authors:

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I. Introduction

In this deliverable 6.1, we characterise graphene FET devices built at IEMN. First, part I describes the GFET process, then part II summarizes DC/AC electrical characterisation. From S parameter characterisation a small signal model will be deduced within part III. Then, we apply the commonly used NF50 characterisation for high frequency noise characterisation. Results are shown in part IV.

II. Description of the GFET process

In order to process devices on full wafer, we use epitaxial graphene growths by thermal decomposition of Si-face silicon carbide. This sample was characterised by Raman spectroscopy and is estimated to be composed of a full monolayer to few-layers (≤5) of graphene. Based on the technological process described in [5], hundreds of dual-top-gated epitaxial graphene field effect transistor (GFET) on SiC substrate are patterned by successive steps of electron beam lithography and standard lift-off process. Coplanar access for RF devices and source and drain ohmic contacts (shown on the SEM images of the device in Fig.1), with 3 different development widths (W=6, 12, 24µm), are metalized with Ni/Au (50/300nm) according to its low contact resistivity on graphene and its compatibility with the different steps of the technological process. After protecting the full active area with a negative hydrogen silsesquioxane (HSQ) resist, the graphene exposed was then etched by O2 RIE with a speed rate of 2 layers per minutes.

We use 10nm of Al_2O_3 deposit by an Atomic Layer Deposition technique as gate oxide. To achieve a uniform deposition of this oxide on the hydrophobic surface of the carbon crystal, we had to deposit by evaporation thin aluminium as thin seed layer (~2nm) which is oxidized in ambient before ALD. 100nm and 150nm length dual-gate are finally patterned with the same parameters as the ohmic contacts. Fig. 1 shows a SEM image of GFET device with a 150nm gate length.

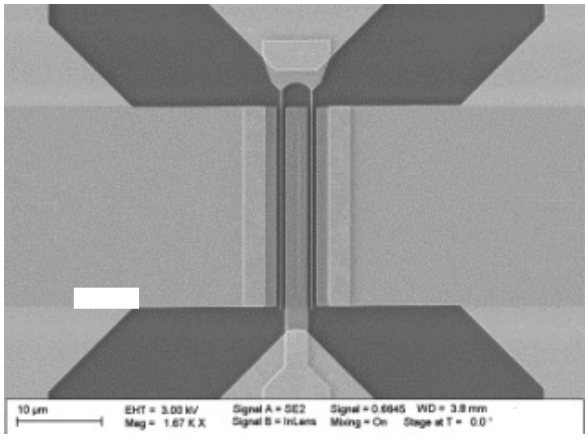

Fig. 1. SEM image of a GFET device.

III. Device Characterisation and small signal modelling

A. DC and S parameter characterisation

The output characteristics of a graphene FET with a 150 nm gate length and W=24µm are shown in Fig. 2. Transfer characteristics and associated DC transconductance of the same device are shown in Fig. 3. An

output current of 2 mA/µm as well as a transconductance of 0.16 mS/mm are achieved. S parameter characterisation has been performed up to 20 GHz on the same device. A pad (open) deembedding has been performed giving extrinsic performances of about f_T=8 GHz and f_{MAX}=7 GHz. A second device with a width equal to 6µm has also been characterised and shows improved performances with maximum g_M=0.25mS/mm and with f_T=12.5 GHz and f_{MAX}=10 GHz. Finally, the best performance is obtained with a gate length of 100nm and W=12µm: at the optimum bias point, g_M=0.275mS/mm, f_T=25GHz and f_{MAX}=19 GHz (This device has not been used for noise characterisation).

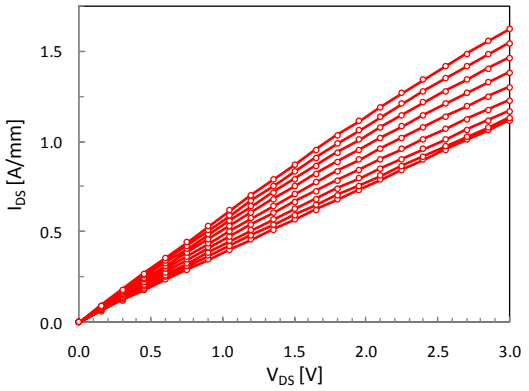

Fig. 2. Drain current I_{DS} versus V_{DS} for different V_{GS} for a GFET transistor with L_G=150nm and W=24µm.

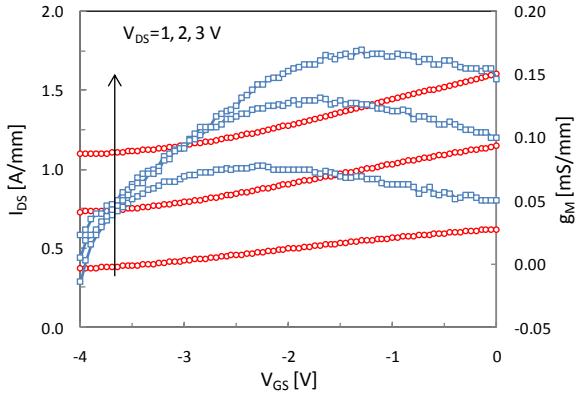

Fig. 3. Drain current I_{DS} (red) and transconductance g_M (blue) versus V_{GS} for different V_{GS} for the same device.

B. Small signal model

A small signal compact model has been developped for the two first devices (W=6 and 24µm) based on the schematic shown on fig. 4. C_{gsp}, C_{gdp} and C_{dsp} have been extracted from PAD-OPEN structure; R_g has been calculated using material and geometrical parameters while R_s and R_d have been deduced using test structure. Bias dependant parameters from the intrinsic structure have been extracted for each measured bias point using conventionnal method [4]. The bias dependant extraction is of interest to extract the minimum noise figure NFmin for each bias point in order to extract the best trade-off of optimal available gain and optimum NFmin.

The table 1 gives the parameters at the otpimum bias point for both devices at V_{DS}=3V and V_{GS}=-2V.

W	C_{GS}	C_{GD}	R_{GD}	R_{GS}	g_M	r_{DS}	$R_s/_d$	R_g	T_{OUT}
6µm	8.2fF	6.7fF	154Ω	104Ω	1.2mS	314	24	1.5	1225K
24µm	32fF	25f	72Ω	26Ω	2.8mS	100	6	6	909K

The fig 5a and b show the magnitude and phase of S parameter measurement and associated simulation for different bias point. The Fig. 6 presents the magnitude of H21 versus frequency for two devices with different widths. Measurement and compact model simulation are compared within fig. 4a, 4b and 5 and shows good agreement for both devices well beyond f_T.

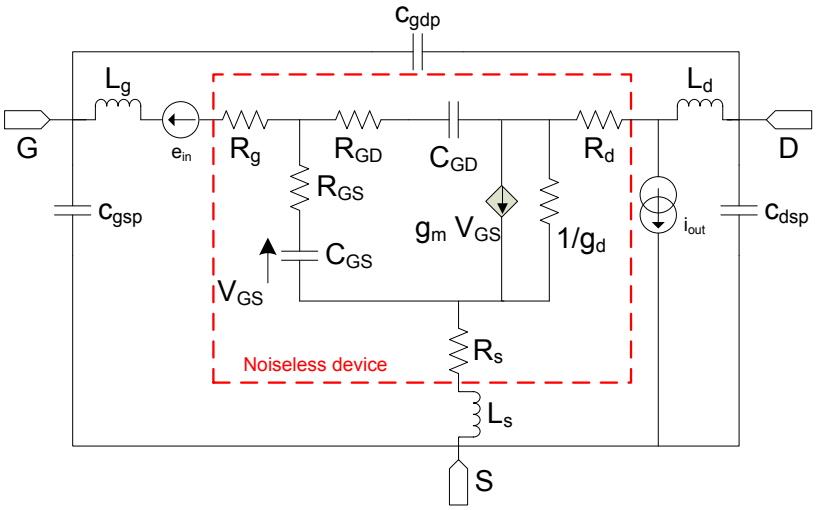

Fig. 4. Schematic of the equivalent circuit of the complete transistor.

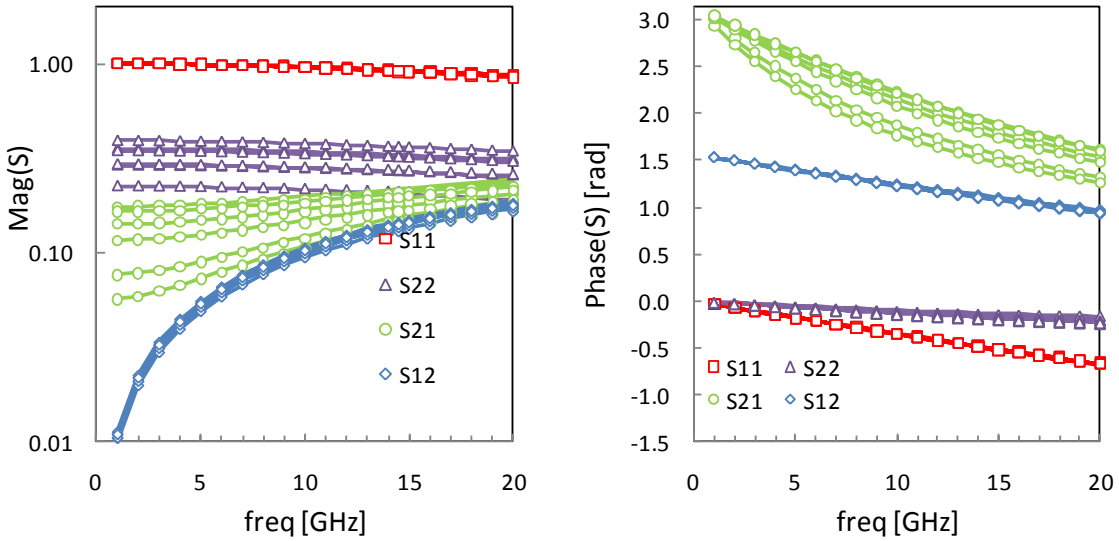

Fig. 5. Magnitude and phase of S parameters versus frequency for different bias conditions. Measurement is in symbol and simulation results of small signal model are in solid line.

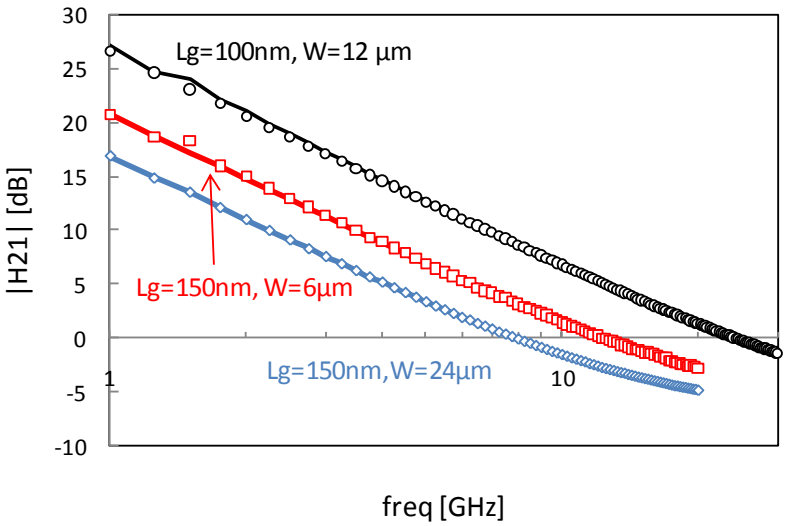

Fig. 6. Magnitude of extrinsic H21 versus frequency for optimum bias point. Measurement is in symbol and simulation results of small signal model are in solid line.

IV. High frequency noise characterisation

Conventionnal NF50 characterisation has been performed using similar method than [4] on different frequency range from 2 to 4GHz and from 4 to 6GHz. Very high noise level is obtained due to the strong mistmacth at the input of the device when the device is characterised on a 50 ohm impedance generator. This is confirmed by the magnitude of S11 which is closed to 1. For the noise performance, the proposed model is validated by comparing the noise figure with a 50Ω generator impedance (NF50) in the measurement process and in calculation model. Noise sources e_{in} and i_{out} are directly correlated to the real part of H11 from the noiseless quadripole times T_{in} and real part of H22 from the noiseless quadripole times T_{out} respectively. Real part of H11 and H22 are directly computed within the SPICE simulation using parameters from the noiseless quadripole. T_{in} is set to ambiant temperature while T_{out} is optimised on NF50 measurement for each bias point. The comparison between NF50 measurement and simulation is shown on fig. 7. A good agreement is observed between model and measurement showing the good trend versus frequency and bias conditions. Extracted T_{out} temperature is ploted versus drain current. From our first results, it seems that T_{out} has two different regime depending if drain current is dominated by electron or hole carrier; i.e. trends of T_{out} changes close to Dirac point when the current is composed of both electrons and holes.

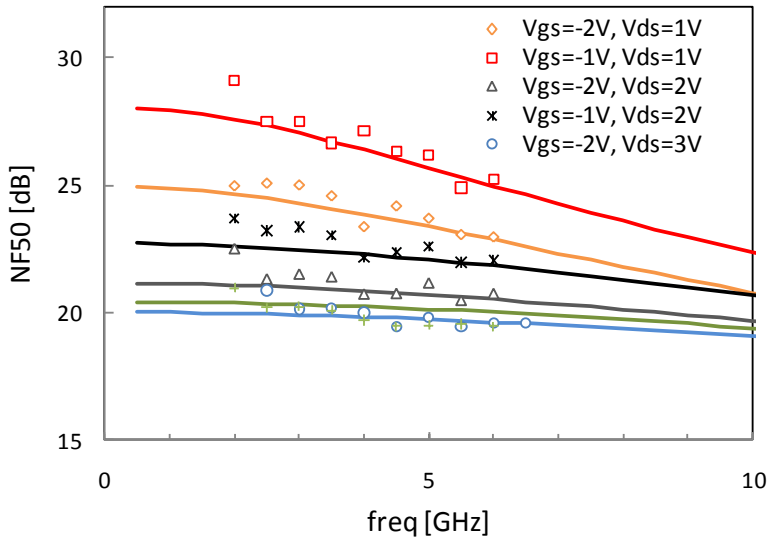

Fig. 7. NF50 characterisation versus frequency and for different bias conditions for the same device (W=24µm) and associated compact model.

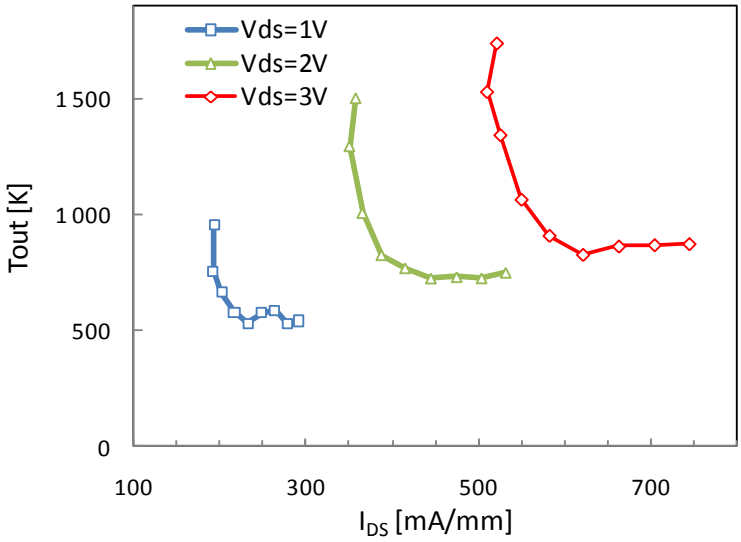

Fig. 8. Extracted T_{out} temperature for the different bias conditons on the same device (W=24µm).

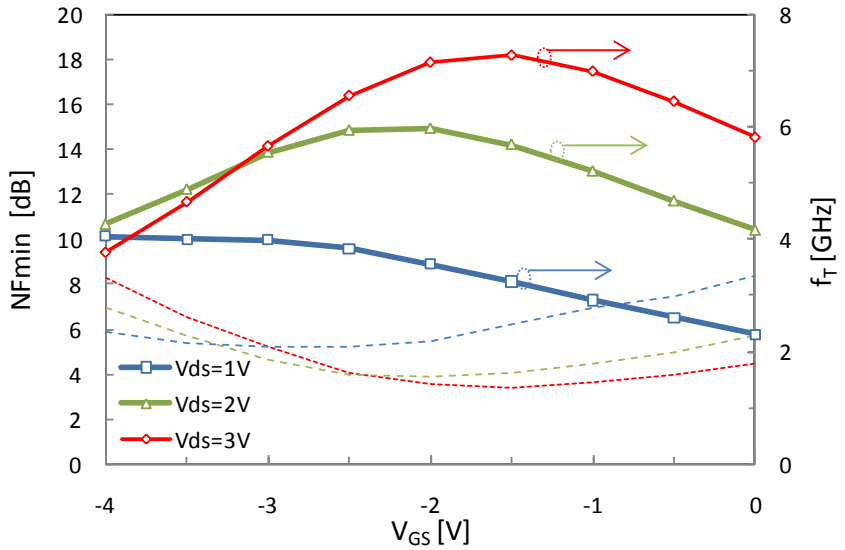

Fig. 9. NFmin and f_T versus V_{GS} and for different V_{DS}; NFmin is extracted at 3GHz. Extrinsic f_T is presented (without PAD).

We apply this approach for both devices and for each measured bias point. The Fig. 9 shows the NFmin extracted at 3GHz and the associated f_T versus bias conditions. It shows that the NFmin optimum is obtained for the optimum f_T bias. The optimum bias point is V_{DS}=3V and V_{GS}=-2V for both devices. For this given bias point, we have plotted NFmin versus frequency for each device (see fig. 10). The smaller device with W=6µm has better RF performances with f_T=12.5GHz and NFmin=2.37dB at 3GHz (device without PAD).

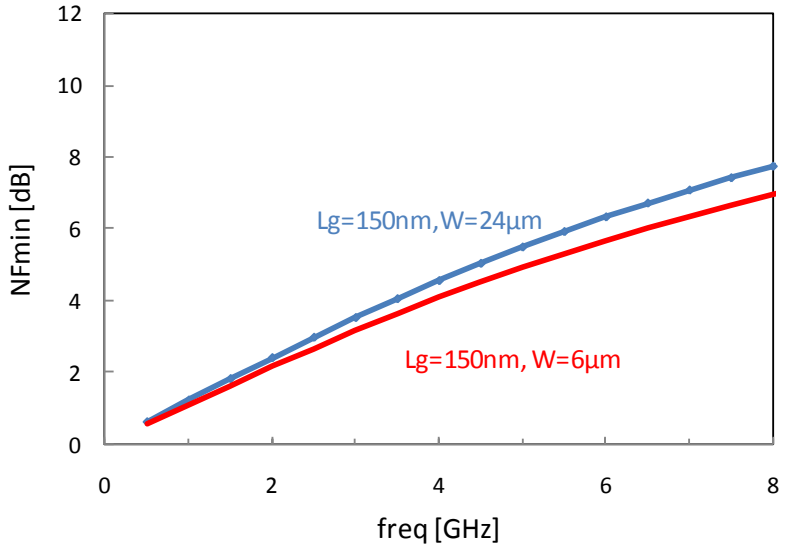

Fig. 10. NFmin versus frequency at optimum bias point for two different transistors W=6µm, and W=24µm (V_{DS}=3V V_{GS}=-2V).

V. Conclusion

Short gate length GFET devices have been processed on SiC wafer using Al2O3 as gate oxide. The channel is composed of a full monolayer to few-layers (≤5) of graphene. These devices have been characterised with DC, S parameter and high frequency noise measurement (NF50). Our best device shows an extrinsic f_T/ f_{MAX} of 23GHz and 19GHz respectively. Using a small signal compact model, the noise parameters have been extracted in order to evaluate the graphene material for RF applications. Complementary measurement using noise-pull measurement system should be performed to match the device at its optimum inpedance and to measure directly the NFmin parameter. This procedure may reduce measurement and noise parameter extraction innacurracy. Finally, this first GFET generation does not compete with very advanced devices but shows promising performances compared to the low maturity of the technology.

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