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2. Introduction

A trend leading to an increase of the switching frequency of DC-DC converters can be observed in many applications, ranging from point-of-load converters to automotive microcontroller's power supplies. One of the main motivations behind this trend is the possibility to reduce the size of bulky external components or even to fully integrate the passives inside the package (Power System-In-Package, PwrSiP) or on-chip (PwrSoC).

Regulating a high-frequency DC-DC converter with a high-bandiwdth digital ripple-based controller presents many challenges and poses tough requirements for the Analog-to-Digital and Digital-to-Analog Converters (ADC and DAC, respectively). In this paper, a mixed-signal implementation of a ripple-based controller, based on the constant-frequency V2 architecture, is presented. The controller has been successfully employed to regulate the output voltage of an integrated high-voltage (up to 16V input voltage, which requires high voltage devices in an integrated solution), high-frequency (up to 10MHz switching frequency) buck converter (HV-DCDC). The output voltage can be regulated in the range from 3.3V to 5V. The controller can be configured to use either the inductor current sense or capacitor current sense, yielding a V2IL or V2IC architecture, to further improve stability in low-ESR applications. The internal Fast Feedback (FFB) loop, optionally including current information, has been implemented in the analog domain, in order to guarantee fast transient response at high switching frequencies, while the outer Slow Feedback (SFB) loop has been realized digitally. Therefore, this approach exploits both the simplicity and performance of the analog domain and the flexibility and programmability of the digital implementation.

A hardware prototype has been developed, where the power stage and driver have been designed in a 130nm Bipolar-CMOS-DMOS (BCD) technology and integrated on the same silicon die. In order to validate the controller concept, the analog FFB loop has been realized with discrete components, while the digital SFB has been implemented by means of an industrial microcontroller. The long-term goal is to integrate all circuitries and components (including the passive filter) together with the power stage and driver to realize a PwrSiP or PwrSoC solution.

3. Controller architecture and implementation

A schematic representation of the overall system is illustrated in Fig.1. The architecture is based on a conventional V2 controller with feed-forward of the inductor or capacitor current. The current sensing has been implemented with a shunt resistor of 15 mOhm in order to avoid excessive penalization of the overall efficiency, but at the same time guarantee an accurate reading. The current information is then processed by an instrumentation amplifier topology. In a future integrated design, the current sense could be implemented with a lossless technique, e.g. by sensing the current through the high-side switch with a SenseFET-based approach. Alternatively, the capacitor current could be estimated by means of a trans-impedance amplifier.

The fast feedback loop (FFB, depicted in blue in Fig.1 has been implemented in the analog domain with discrete components, in order to guarantee fast operation, while the slow feedback loop (SFB, realized by the ADC-PI-DAC path inside the dashed red box in Fig.1 has been realized by means of an industrial microcontroller unit, for maximum programmability and flexibility. The output voltage of the buck converter is passed to the analog subtractor unit, based on a high speed amplifier. The reference signal Vref is set by a DAC of the microcontroller.

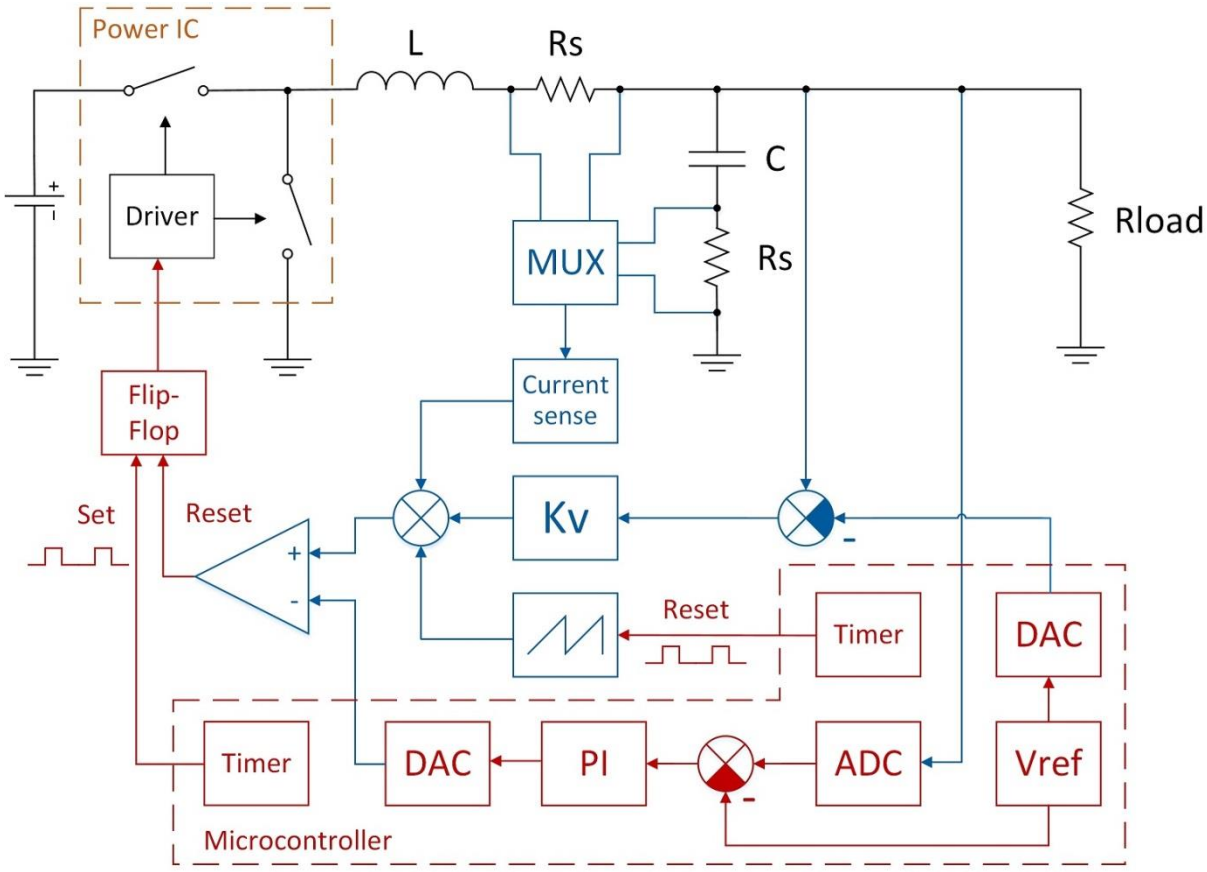

Figure 1. Block diagram of the HV-DCDC converter with the control loop

The reference voltage can be programmed in the range from 3.3V to 5V and can be updated online, thanks to the digital implementation.

In order to avoid subharmonic oscillations, a ramp generator, operating at the switching frequency fsw of the converter, is used for slope compensation. The ramp is realized by charging a capacitor with a constant current and a fast discharge phase, that takes up to 8ns. The timing of the ramp generator is managed by digital signals generated from the microcontroller. A non-inverting summing amplifier adds the current sense, output voltage error and ramp signals together, weighted by appropriately designed coefficients, which are defined by resistors.

The SFB consists of a digital proportional-integral (PI) regulator. The ADC samples the output voltage with a resolution of 12 bits. The DAC has also a resolution of 12 bits. The computations are performed by the Floating Point Unit (FPU) of the microcontroller, which is based on the ARM Cortex-M4 architecture. The output of the SFB is updated with a rate of approximately 250kHz. Furthermore, the microcontroller can control the driver of the buck converter through an SPI interface, in order to implement protection features and to regulate various parameters, such as the dead-time to avoid shoot-through currents. The microcontroller also dictates various timings of the system. The PWM modulator is a conventional constant-frequency peak control modulator, with a nominal switching frequency fsw=10MHz, which is set by the microcontroller.

4. Experimental results

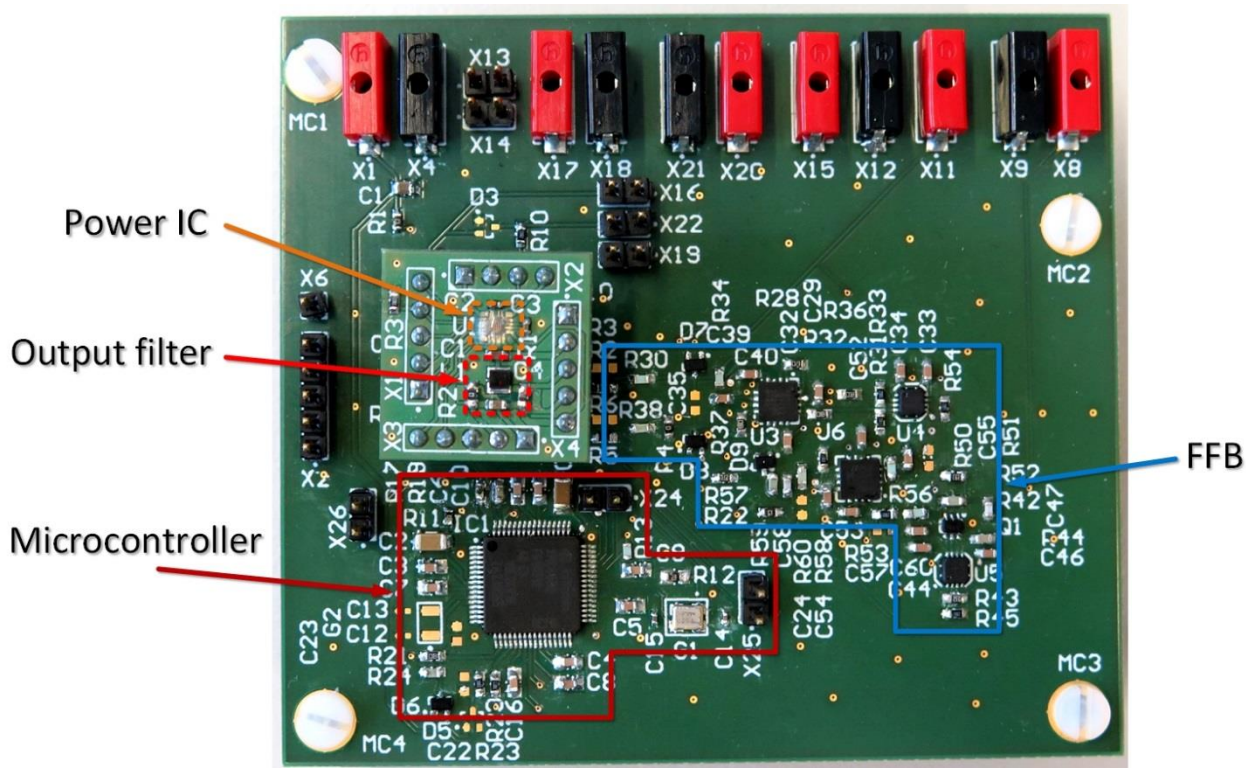

Figure 2. Picture of the PCB board

A picture of the developed hardware prototype is shown in Fig.2. The driver and power stage integrated circuit (IC) is visible in the top left side, together with the external passive components of the output filter. The capacitance of the output filter is C=470nF, while the inductance is L=1uH. The microcontroller can be seen in the bottom left part, while the analog part of the controller (FFB) occupies the remaining area. The size of the board is 85mm x 75mm. The area of the power IC is 1 mm^2, while the output filter occupies approximately 6 mm^2, not including sense resistors.

Load variations have been verified experimentally, through the aforementioned hardware prototype. The measurement is reported in Fig.3, where the top waveform corresponds to the output voltage, the middle one is the switching node and finally the bottom curve represents the load current. The undershoot caused by a 200mA load jump equals approximately 85mV. The overshoot resulting from a load drop from 200mA to 0 (not shown in the figure) equals approximately 60mV.

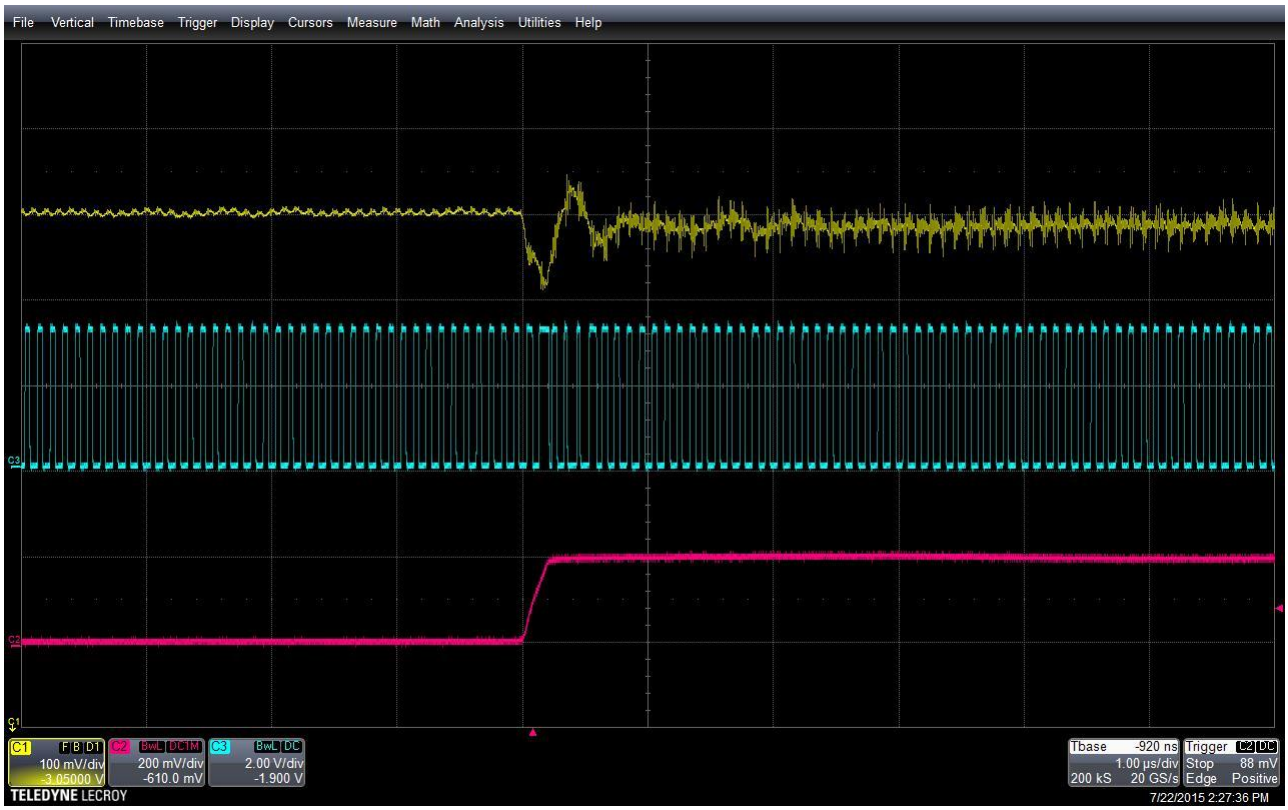

Figure 3. Load transient measurement

5. Conclusions

A mixed-signal implementation of a V2 or V2IC/V2IL controller has been presented. The capacitor (or inductor) current feedback is particularly important in order to improve stability and performance in the case of low-ESR capacitors. The fast part of the feedback loop has been implemented in the analog domain, in order to support high switching frequencies. The digital part, implemented with an industrial microcontroller, gives additional flexibility and programmability.

The performance of the controller has been simulated and validated experimentally by means of a hardware prototype, which includes a 10MHz 16V-input buck converter (HV-DCDC), implemented in a 130nm BCD technology. Excellent dynamic performance during load transients has been proven.