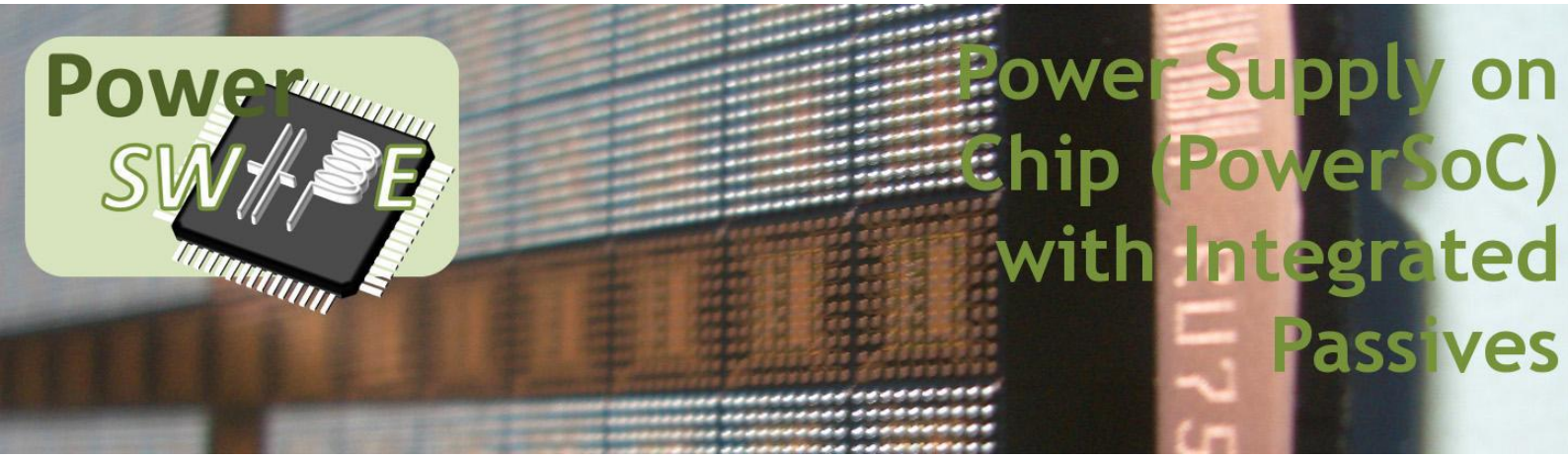


**PowerSWIPE (Project no. 318529)**

**"POWER SoC With Integrated PassivEs"**

# D2.4: Status Report

# "Architecture optimization of 1st prototype chips"

**Dissemination level:**

**Responsible Beneficiary**

**Centro de Electrónica Industrial, Universidad Politécnica de Madrid**

FP7-ICT-2011-8 – Collaborative Project (STREP)

PowerSWIPE (Grant agreement 318529)

Objective ICT-2011.3.1 – Very advanced nanoelectronic components: design, engineering, technology and manufacturability

| Summary | | | | | |
|---|---|---|---|---|---|
| Name | Architecture optimization of 1st prototype chips | | | | |
| Status | | Due | Month 10 | Date | 01-October-2013 |
| Author(s) | Vladimir Šviković, Jorge Cortes, Pedro Alou, Jesús Ángel Oliver | | | | |
| Editor(s) | José A. Cobos, Jesús Ángel Oliver | | | | |
| DoW | Architecture optimization of 1st prototype chips: Report on Architecture optimization with improved models based on characterization of first prototype chips [month 24] | | | | |
| Dissemination Level | PU | | | | |
| Nature | Report | | | | |

| Document history | | | |
|---|---|---|---|
| V | Date | Author | Description |
| V0 | 28-October-2014 | Vladimir Šviković, Jorge Cortés | UPM contribution |
| Final | 26-November-2014 | Jesús A. Oliver | Final Deliverable |

Content

# 1. Introduction

The main objective of this deliverable is to update optimize the power distribution architecture based on improved models developed along this year. Special attention has been paid to the improvements of the passives components, especially the optimization of the magnetic components due to its large impact on the size/efficiency trade-off and on the improvements of the power management IC loss model, that have been extensively validated.

# 2. Selected Architecture of System

In D2.1 and D2.3, preliminary architectures of system were shown. In this section, the final complete selected architecture is explained. Furthermore, an efficiency analysis is performed to evaluate the chosen architecture.

Fig. 1 shows the first considered PowerSwipe System Level Architecture composed by a High Voltage DC-DC converter (HVDC-DC) and two Low Voltage DC-DC converters (LVDC-DC). The HVDC-DC converts the battery voltage to 5V or 3.3V. Then, the LVDC-DC lowers the voltage to 1.2V to supply the microprocessor. Although the maximum input voltage of the system is 16V in normal operation, the HVDC-DC needs to withstand input voltage surges of 48V and even negative input voltage, caused by certain operations of the vehicle (cold start, steering, etc). These surges are listed in the "PowerSwipe Requirements" Excel document and in the Deliverable 2.2.

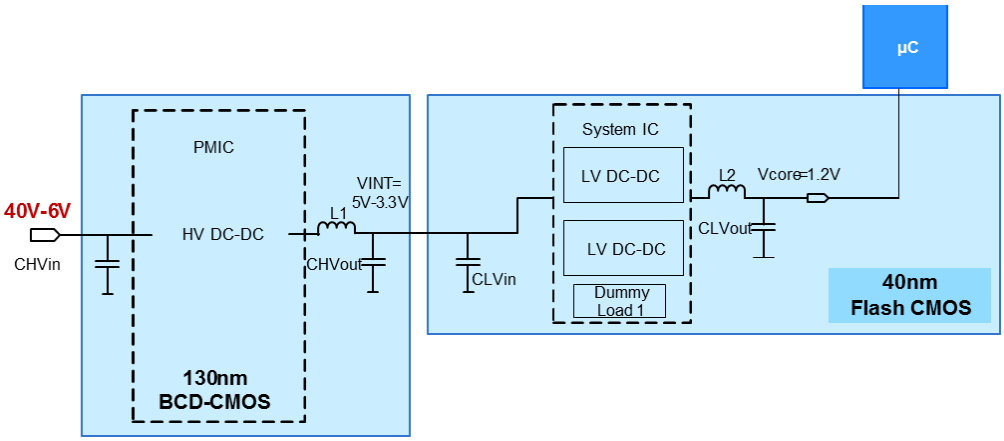


Fig. 1 First considered PowerSwipe System Level Architecture (D2.1)

Fig. 2 shows the second considered PowerSwipe System Level Architecture (D2.3). The HVDC-DC remains the same but different converters are added in the second stage.

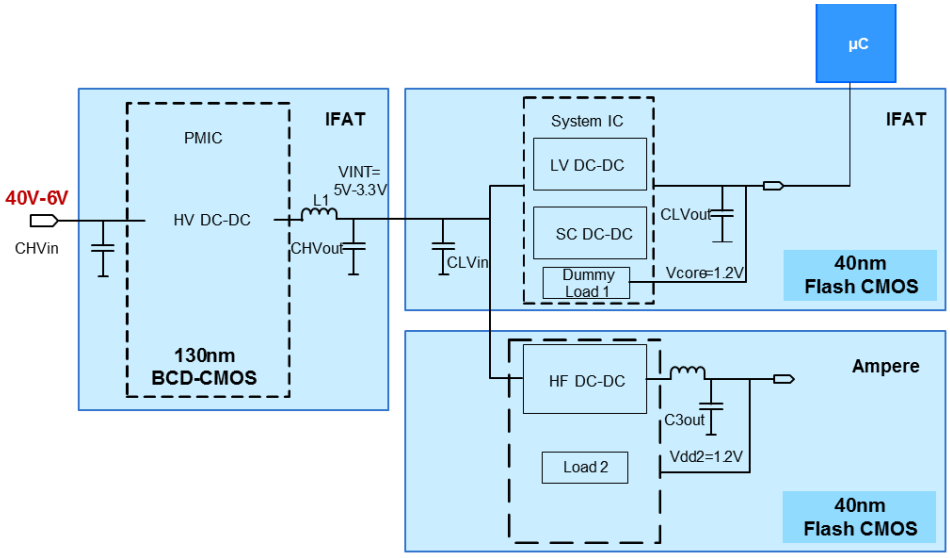


Fig. 2 Second considered PowerSwipe System Level Architecture (D2.3)

The second stage of this architecture is composed by:

- The LV DC-DC converter that is inductor-based and will supply the µController Core (1.2V) from the intermediate voltage generated by the HV DC-DC.
- The SC DC-DC converter will generate a controllable output voltage of 1.2V from the intermediate input voltage (5V or 3.3V).
- The HF DC-DC converter that is inductor-based and will scale down an intermediate voltage of 3.3V to 1.2V using high switching frequency techniques (100MHz-200MHz). This is an inductor-based converter.

Again in this architecture the HVDC-DC normal operation is from 6V-16V but it needs to withstand electrical surges up to 48V and even negative input voltage. As a result of these electrical surges, MOSFETs needed to be rated for 60V instead of 16V, worsening the expected efficiency.

As these electrical surges are a result of the operation of the vehicle and their consideration is not needed to validate the concept of full integration on chip, the partners agreed to include an external protection against these transients.

Fig. 3 shows the final PowerSwipe System Level Architecture (D2.3). The second stage remains the same as in Fig. 2 but, an external protection is added between the battery and the input of the HVDC-DC. This way the HVDC-DC is rated for a maximum input voltage of 16V.

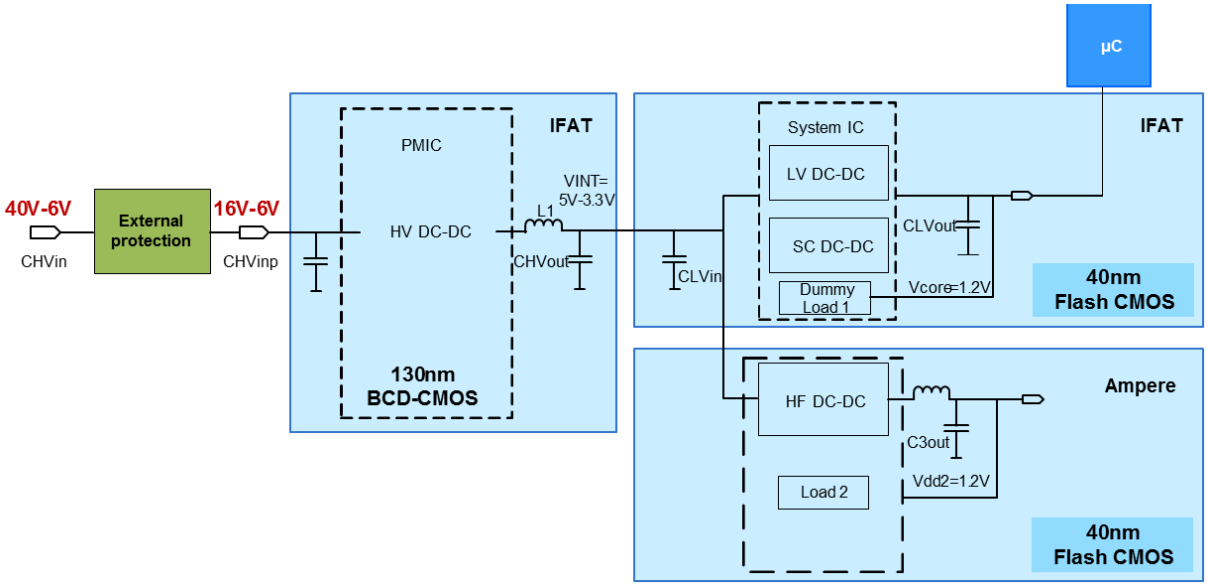


Fig. 3 Final PowerSwipe System Level Architecture

## 3. Analysis of selected PowerSwipe System Level Architecture

The Deliverable 2.3 showed the calculated efficiency for the different blocks of the System Level Architecture. In this section, the results are put together to have an understanding of the expected efficiency of the whole system under specific conditions (different intermediate voltages, different output powers). Two different setups are studied: setup A which includes the inductor-based converter (LVDC-DC) as the second stage and the setup B which includes the switched-capacitor converter (SC DC-DC) as the second stage. The very high frequency converter (HF DC-DC) is not included because the losses calculations are not yet sufficiently accurate.

- Setup A: Fig. 4 shows the first setup composed by the external protection, an inductor-based HVDC converter and an inductor-based LVDC converter.

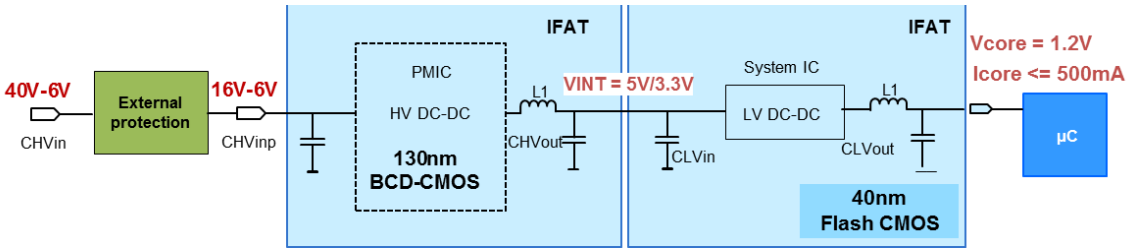


Fig. 4 Setup A: External Protection + Inductor-based HVDC + Inductor-based LVDC

The output voltage of the system is Vcore = 1.2V and the maximum output current is 500mA. The intermediate voltage can be either 5V or 3.3V. Interpolating the efficiency curves of the HVDC-DC converter on the deliverable 2.3 and using the optimization GUI platform of deliverable 2.2, the expected efficiency of the system is calculated from an output current of 50mA to 500mA. Fig. 5 and Fig. 6 and shows the efficiency curves of the HVDC converter, the LVDC converter and the whole system for the case of an intermediate voltage Vint = 5V and Vint = 3.3V, respectively.

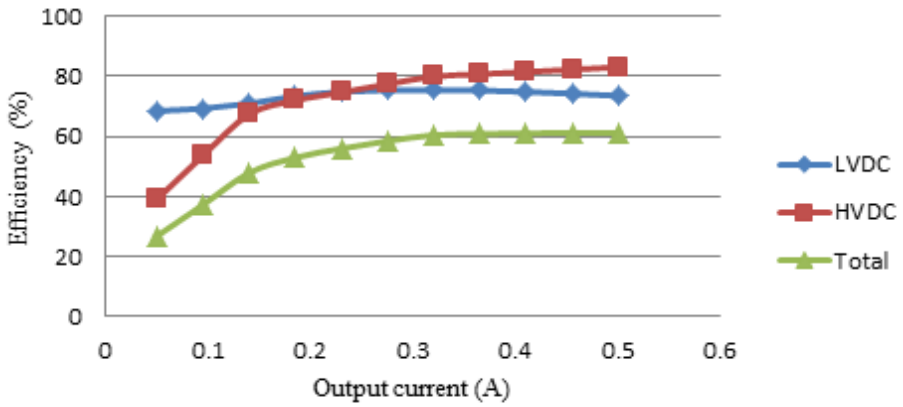


Fig. 5 Setup A: External Protection + Inductor-based HVDC + + Inductor-based LVDC. Vint = 5V

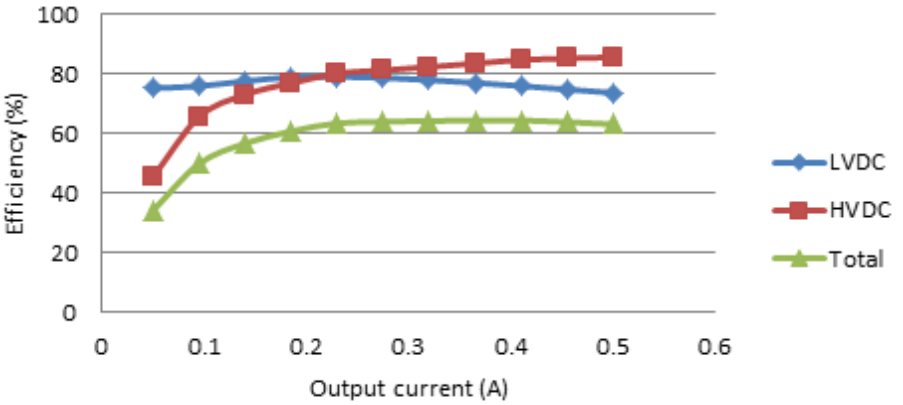


Fig. 6 Setup A: External Protection + Inductor-based HVDC + Inductor-based LVDC. Vint = 3.3V

- Setup B: Fig. 7.shows the second setup composed by the external protection, an inductor-based HVDC converter and a switched capacitor converter (SC DC-DC).

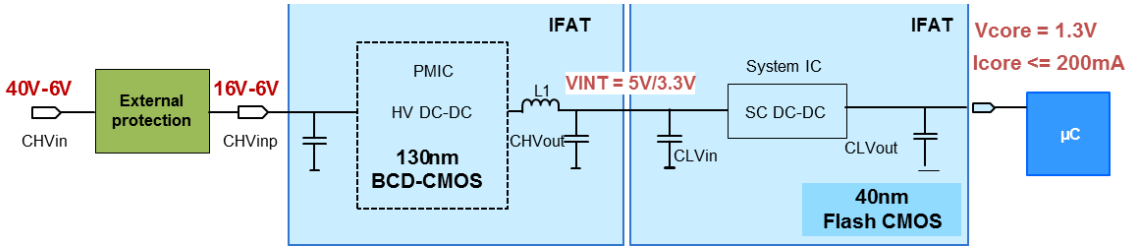


Fig. 7 Setup B: External Protection + Inductor-based HVDC + Switched capacitor LVDC

The output voltage of the system is Vcore = 1.3V and the maximum output current is 200mA. The intermediate voltage can be either 5V or 3.3V. Interpolating the efficiency curves of the HVDC-DC converter and the SC DC-DC converter on the deliverable 2.3, the expected efficiency of the system is calculated from an output current of 50mA to 250mA. Fig. 8 and Fig. 9 and shows the efficiency curves of the HVDC converter, the LVDC converter and the whole system for the case of an intermediate voltage Vint = 5V and Vint = 3.3V, respectively.

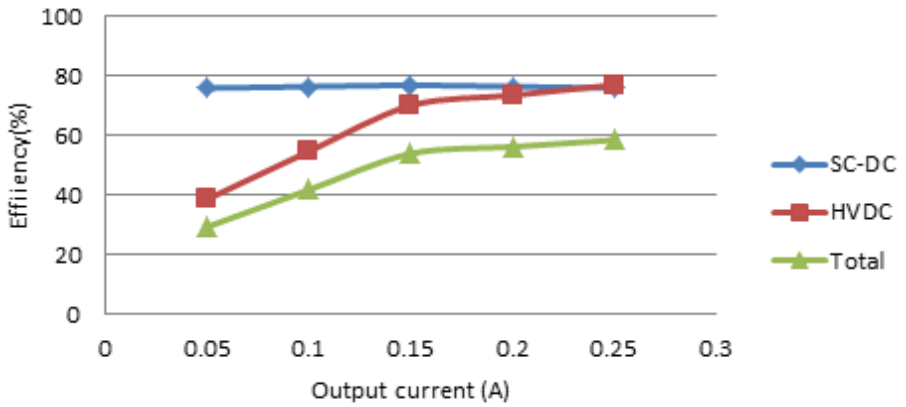


Fig. 8 Setup B: External Protection + Inductor-based HVDC + Switched capacitor LVDC. Vint = 5V.

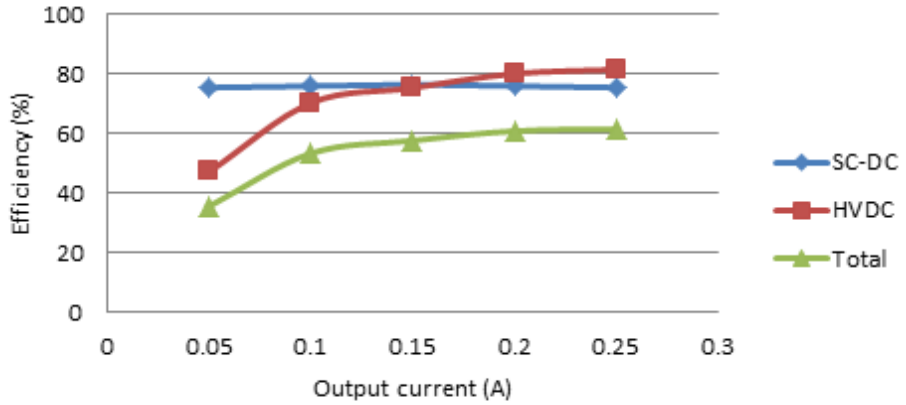


Fig. 9 Setup B: External Protection + Inductor-based HVDC + Switched capacitor LVDC. Vint = 3.3V.

In order to compare all the possibilities, the total efficiency of each setup is shown in Fig. 10 .

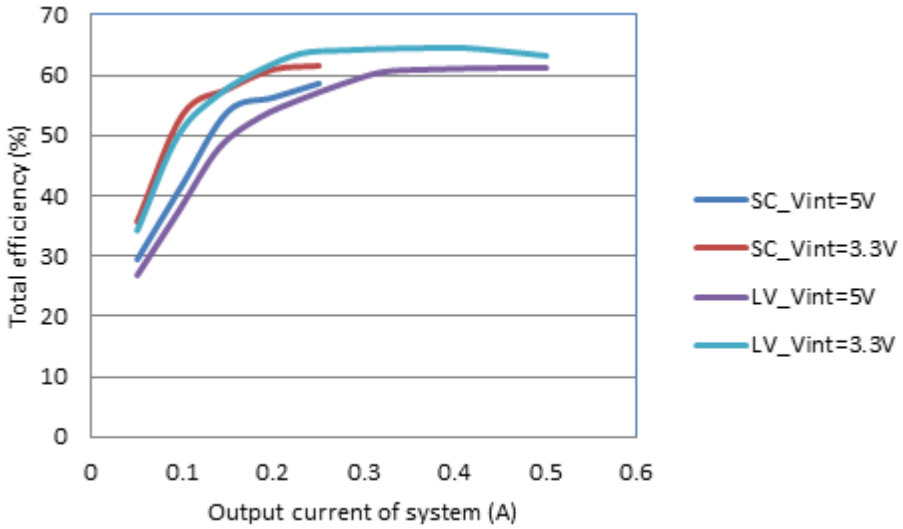


Fig. 10 Comparison of setup A (using inductor-based converter) and setup B (using switched capacitor converter)

From the expected efficiency curves, the setup B using a switched capacitors converter and an intermediate voltage of Vint=3.3V has better efficiency at light loads. However, the switched capacitor converter cannot deliver more than 250mA and the setup A using a low-voltage inductor-based converter is required, reaching more than 60% efficiency. It is also seen that better efficiency is achieved with an intermediate bus voltage of Vint = 3.3V.

## 4. Conclusions

This deliverable shows the detail analysis and optimization results at system level of the architecture selected within this project. These are the results of a tight cooperation between all the partners that have provided all their knowledge about their technologies. This knowledge has been combined into an optimization tool that is able to perform extensive analysis to achieve the optimum design that complies all the requirements.

Two different alternatives have studied: setup A which includes the inductor-based converter (LVDC-DC) as the second stage and the setup B which includes the switched-capacitor converter (SC DC-DC) as the second stage.

In the setup A, the output voltage of the system is Vcore = 1.2V and the maximum output current is 500mA. The intermediate voltage can be either 5V or 3.3V. It is shown that for an intermediate voltage of 5V the efficiency of the HV DC-DC Converter at full load will be around 83% and the LV DC-DC converter will have an efficiency around 75%. If the intermediate voltage is 3.3V the HV DC-DC Converter will go to 85% and the LV DC-DC converter will stay aournd 75%. In both cases individual optimizations with the same restrictions have been performed.

In the setup B, the inductor based LV DC-DC converter has been substituted by a SC DC-DC conveter with the output voltage beeing Vcore = 1.3V and the maximum output current is set to 200mA. The intermediate voltage can be either 5V or 3.3V. In both cases, the HV-DCDC converter has been optimized for these specification. In this case, the efficiency is less sensitive to load variations and the expected values of efficiency for the SC- DC-DC converter are around 78%.

Both for the case A and B, the efficiency of the converters is much higher than the efficiency of an ideal linear regulator (LR) converter. For an ideal LR converter the efficiency to go from 5V to 1.2V is 24%. The results are more striking if instead of efficiency we compare the losses. Losses in the LR will be almost 10 times bigger than in the case of the LV DC-DC converter or the SC DC-DC converter.