

Power Supply on Chip (PowerSoC) with Integrated Passives

PowerSWIPE (Project no. 318529)

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“Report of Interposers Test”

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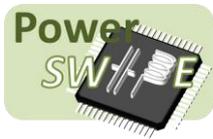


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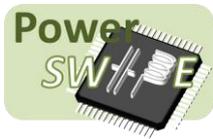
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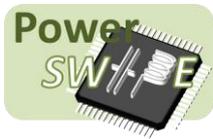


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1. Table of Contents

1.	Table of Contents.....	3
2.	Publishable Summary.....	4
3.	Introduction.....	4
4.	Work description	4
4.1	Parametric analysis of capacitor elements.....	5
4.1.1	Forewords	5
4.2	Test structures and theoretical RLC extraction	6
4.1	Experimental RLC extraction.....	8
4.1.1	Forewords	8
4.1.2	Characterization results for power swiipe capacitive components	9
4.2	Wafer sorting	9
4.2.1	Wafer test infrastructure setup	9
4.2.2	Wafer sorting results on proto and backup lots	10
5.	Conclusion	Error! Bookmark not defined.



2. Publishable Summary

This deliverable corresponds to the work done along Power Swipe project for the implementation of characterization and testing techniques. Those techniques have been deployed on capacitive interposer silicon produced by IPDiA to:

- A. Demonstrate good matching between the silicon interposers parametric behaviors and the initial specifications (capacitor RLC extraction across frequency range and interconnections parasitic extraction). Those measurements have been performed on a subset of samples as long as the repeatability of the electrical behavior is guaranteed by the PICS process.
- B. Wafer sort the demonstration silicon and identify functional dies. Considering the limited number of dies available (active and passive) it was essential for the electrical demo to assemble only the functional occurrences.

3. Introduction

This deliverable corresponds to the work done along Power Swipe project for the implementation of characterization and testing techniques.

Although, the concept of capacitive interposer is relatively simple from a conceptual point of view (passive functions only), the control of the parasitic is essential for the final performance. In that perspective, special design techniques have been used for capacitor design (reported in deliverable 3.4) to:

- Reduce capacitors serial resistance (ESR) to limit losses in the input/output filters and limit voltage swing on the converter output,
- Increase capacitors Self Resonance Frequency beyond the converter working point to guarantee capacitive behavior/sufficient quality factor (or low dissipation factor).

To assess the performance of the capacitors at high frequency (up to 200MHz for ITV), RF measurements techniques based on power scattering have been used instead of conventional RLC-meter measurements. The benefits of this approach correspond to:

- Extraction of a frequency dependent model across wider frequency span (30kHz-5GHz in our case) where RLC meters are limited to few MHz,
- Network analysis enabling a physical model, whereas RLC-meters are usually limited to simplistic serial/parallel models topology.

Beyond the parametric characterization, wafer sorting of the produced silicon is also an essential step to identify the functional dies. Indeed, as samples quantities are limited ($\sim < 100$ dies for each type for passives and actives), it is essential to prove that the silicon is functional prior assembly. For that purpose, test resources (specific probe cards and test programs) have been developed and implemented in the IPDIA test floor. They have been used to screen the initial interposer production and to initiate the yield improvements activity.

4. Work description

4.1 Parametric analysis of capacitor elements

4.1.1 Forewords

Real capacitors can be substituted by their equivalent circuit model shown in Fig.1a. However in practice when designing electronic circuits with capacitors, simpler capacitor equivalent circuit model is usually sufficient as shown in Fig.1b. In this model ESR accounts for both R_p and R_s . Indeed, in application like T filter for DC converter input/output, global ESR represents the dissipative term which is much more important than R_p and R_s separately. Furthermore the nature of dielectric used in PICS (oxy-nitride) is yielding very low leakage and losses in the frequency range of interest giving negligible contribution of R_p term.

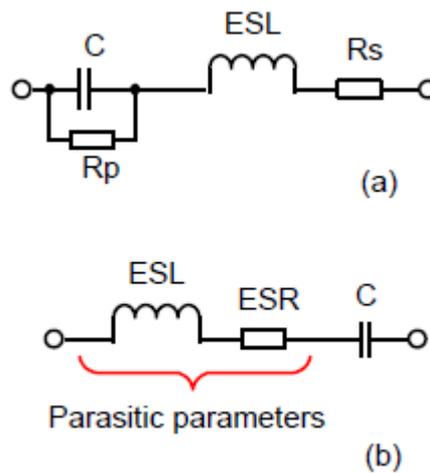


Fig. 1: Real capacitor equivalent circuit model (a) and its simplified version (b).

At a self-resonance frequency SRF a capacitor has its minimum $|Z_c|$, which is equal to ESR (at f_{res}). For $f < f_{res}$, $|Z_c|$ is decreasing function of f , but for $f > f_{res}$, $|Z_c|$ increases as f increases, Fig.2.

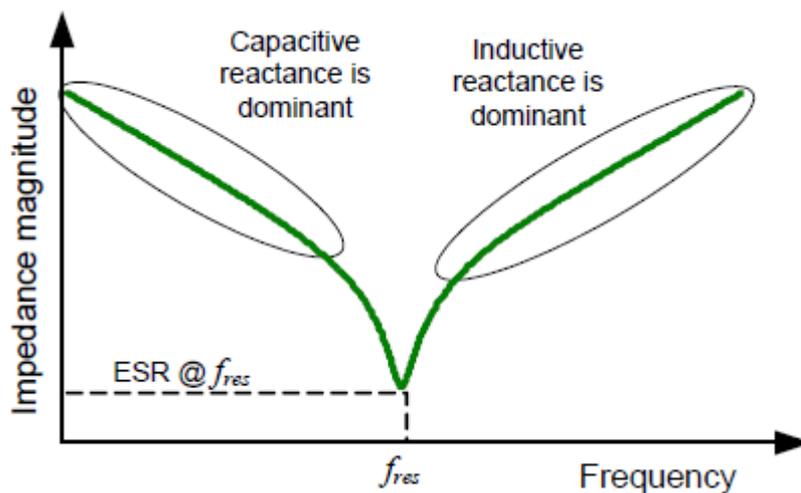


Fig. 2. Real capacitor impedance magnitude versus frequency.

4.2 Test structures and theoretical RLC extraction

For two-terminal passive electronic components measurements using a VNA (Vectorial Network Analyzer), three measurement techniques can be used: reflection (based on reflection coefficient S_{11} measurement), shunt-through (based on transmission coefficient S_{21} measurements) and series-through techniques (based on S_{21} measurements) as shown in Fig.3. Shunt-through technique is usually used for low-impedance passive which are of concern at the DCDC converter working frequency.

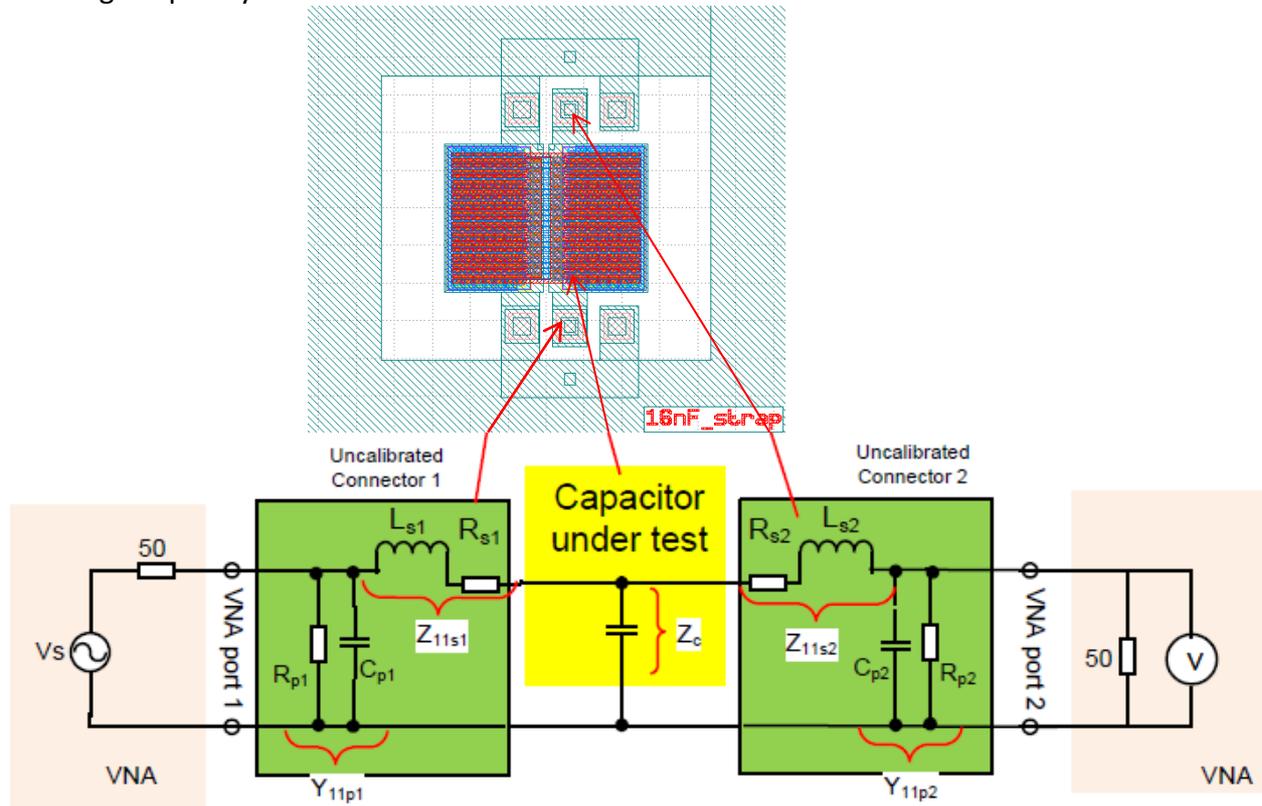


Fig. 3. Experimental setup to perform the shunt-through technique and its equivalent circuit model.

Since it is impossible to perform full SOLT calibration on silicon devices (load cannot be processed), the access parasitic (corresponding to equivalent series impedance Z_{11s} and equivalent conductance Y_{11p}) should be extracted and subtracted from the capacitors measurement results using de-embedding technics.

In view of the technology stack, it is assumed that the terms Y_{11P1} and Y_{11P2} are corresponding to very low conductance in the frequency span of interest. Indeed the C_{p1} capacitor is estimated in the range of \sim fF whereas the R_{p1} equivalent resistor is estimated $>1G\Omega$. The impact of the corresponding impedance inserted in parallel with the DUT is therefore negligible. Same reasoning applied for the terms C_{p2} and R_{p2} corresponding to the second port.

Contrary, the serial terms Z_{11s1} and Z_{11s2} need to be carefully considered for the extraction of the DUT ESR/ESL. Indeed considering the technological stack and the physical sizing of the access, it is expected that the terms L_{s1}/L_{s2} are in the order of \sim 100 pH which is higher than the DUT ESL, and that the ESR is $>50m\Omega$ potentially significantly impacting the ESR and SRF determination. To separate the DUT true impedance from the serial accesses we use S parameter 2 ports measurements. Standard GSG ZProbes are used to contact the silicon. The parasitic induced by the



measurement chain from the VNA down to the tip of the GSG probes are de-embedded using standard SOLT calibration kit.

From a calculation point of view, the experimental [S] parameters box is transformed to [Z] parameters and DUT RLC is extracted from the terms Z12 according usual relations (T network equations):

$$C = \frac{\text{imag}(Z[1,2])}{\omega}$$

$$ESR = \text{real}(Z[1,2])$$

$$SRF = \frac{1}{(2 \pi \sqrt{ESL \cdot C})}$$

In the shunt-through configuration the accesses parasitic are embedded in the Z11 and Z22 terms that are not used for DUT parameter calculation (T network equation).

4.1 Experimental RLC extraction

4.1.1 Forewords

A simplistic RLC equivalent circuit for a capacitor does not reflect properly real capacitor behaviour across the frequency span. Indeed, additional parasitic paths/physical contributions are generating conjugate impedance that combine with the theoretical network. This results in apparent capacitance, resistance and inductances changing with respect to frequency.

A common practice for specification/components comparison is to communicate the magnitude of the capacitance at low frequency (i.e. stable and far away from the SRF), the ESR that is defined at the SRF (i.e. the complex impedance is zeroed at this point) and the SRF which defines the maximum frequency where the component still operate as a capacitor (beyond this frequency the capacitor becomes inductive) – an illustration of those parameters is presented on the figure 4.

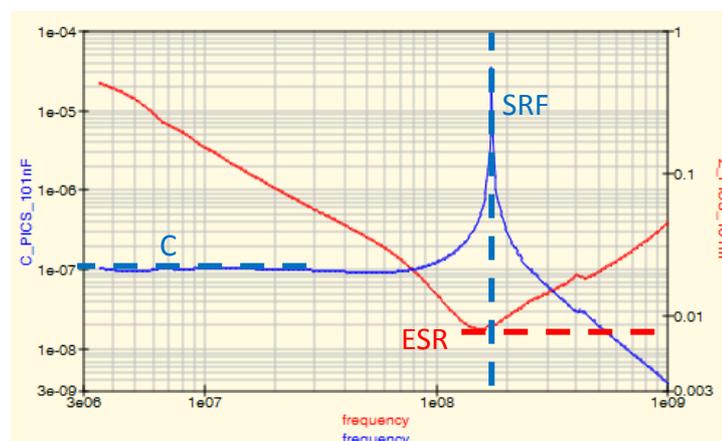


Fig.4: Representation of the impedance modulus (red) and capacitance extraction for a 100nF PICS capacitor.

4.1.2 Characterization results for power swipe capacitive components

A multi project reticle has been developed, embedding the GSG test structures as described in section 4.1 combined with D1 and ITV passive interposer. All the capacitive flavours needed for D1 and ITV have been characterized as standalone components. Corresponding key electrical characteristics and comparison with spec is presented in table 1.

Demo chip	Name	C(nF) Typ. @ 20kHz	C spec. (+/-15%) (nF)	ESR (mOhm) Typ. @ SRF	ESR spec. max(mOhm)	SRF Typ. (MHz)	SRF spec. min (MHz)
D1-LV	Cf	31	30	104	100	380	>11
D1-LV	Cin_LV	571	665	37	50	100	>11
D1-LV	Cout_LV	352	400	45	50	150	>11
D1-LV	Cout_SC	245	260	30	90	130	>11
D1-LV	Cin_evr	105	100	30	50	200	>11
D1-HV	CHV_IN	211	200	48	100	190	>11
D1-HV	CHV_Out	470	500	17	50	100	>11
D1-HV	CHV_hs	29,2	20	67	200	250	>11
D1-HV	CHV_ls	54.5	40	115	100	200	>11
ITV2/D2	Cdec	11.3	10	147	200	700	>200
ITV2/D2	COut	16.4	16	108	140		>200
ITV2/D2	CIn	32.7	33	59	80	350	>200

Table1: List of capacitive components intended for D1 and ITV demonstrators. Greyed columns are corresponding to specification.

4.2 Wafer sorting

4.2.1 Wafer test infrastructure setup

The method described in the section 4.1 for capacitor parametric extraction cannot be used for wafer sorting. Indeed, as explained specific GSG pinning is required that is unsuitable for real chip design (space consuming and parasitic impact). Furthermore, VNAs need frequent calibration and are extremely slow in term of acquisition time: i.e. a few seconds are required per component.

For those reasons, a specific test setup has been built for each of the D1 and ITV design. This setup is implementing a specific probe card that corresponds to the real circuit pinning (see fig. 5) The probe card is embedded onto an SPEA production tester, that implements voltage/current source/meter as well as a precise time base.

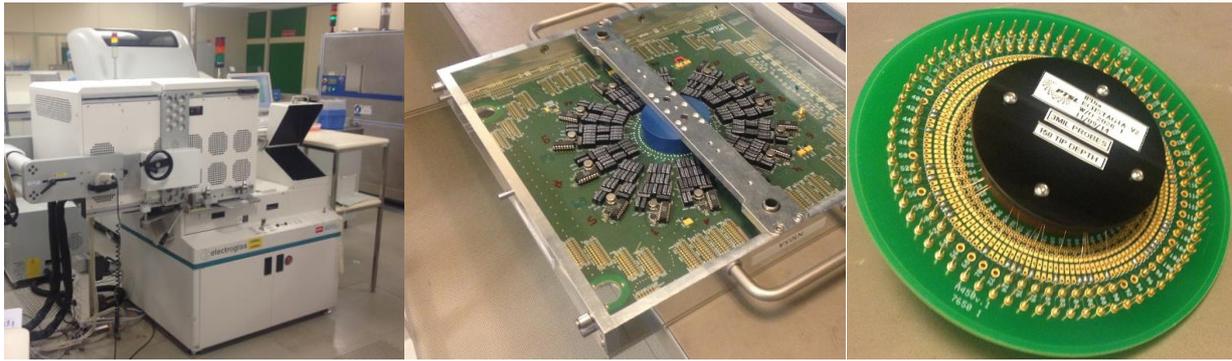


Fig5: SPEA tester, test board, and probe card for the D1A-LV design

A specific test program has been developed which is logging the following:

- Electrical continuity of the chains that are in closed loop on the capacitor interposer
- Isolation between adjacent chains
- Capacitance of isolated capacitors (when possible) or equivalent capacitance of a group of capacitance. The C measurement is performed in the time domain.
- Leakage of isolated capacitors (when possible) or equivalent capacitance of a group of capacitance.

4.2.2 Wafer sorting results on proto and backup lots

Test limits have been setup according normal process distribution within the range specified for each design (see table2).

Demo chip	Name	C(nF) LSL	C(nF) USL	CLeak (nA) LSL	CLeak(nA) USL
D1-LV	Cf	27	33	0	100
D1-LV	Cin_LV	NA	NA	NA	NA
D1-LV	Cout_LV	NA	NA	NA	NA
D1-LV	Cout_SC	234	301	0	100
D1-LV	Cin_evr	104	114	0	100
D1-HV	CHV_IN	160 (group)	200 (group)	0	50
D1-HV	CHV_Out				
D1-HV	CHV_hs	22	32	0	50
D1-HV	CHV_Is	NA	NA	NA	NA

Table 2: Test limits used for D1 silicon passive testing



No specific issues were observed on the chain continuity/isolation and capacitance values for any of the D1A or ITV designs. For those parameters, yield losses are mostly observed on the wafer edge close to the exclusion area.

On the low voltage capacitors (D1-LV), a large spread is observed on capacitor leakage parameter. The natural process spread exceeds the product specification. As a temporary containment, the test limit has been set to 100nA which corresponds to a typical limit observed for other products having similar capacitance in the same technology node – this should allow sufficient margins to safeguard reliability aspects (i.e. wear-out related to current circulation into the dielectric). However, this induces low electrical yield in the range of 35%.

The cause has been narrowed down to selective etching of the electrodes ending on the thin dielectric (problem does not impact HV stage that has a thicker dielectric). A corrective will be developed in case of transfer to production.

5. Conclusions

In the scope of the PowerSwipe project, characterization methods have been developed to evaluate the parametric performance of passive silicon. A characterization campaign has been conducted on prototype silicon and matching with functional requirements has been proven. Beside parametric test, an industrial test setup has been deployed to screen demonstration silicon and reduce risk of no functionality. A design to process sensitivity has been identified on D1-LV leakage and test limit have been adjusted to preserve sufficient electric yield and safeguard product endurance.