PowerSWIPE (Project no. 318529)

"POWER SoC With Integrated PassivEs"

Deliverable 5.2.1

"Mid-term Dissemination Report"

Dissemination level: PU

Responsible Beneficiary
Tyndall National Institute, University College Cork

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FP7-ICT-2011-8 – Collaborative Project (STREP)

PowerSWIPE (Grant agreement 318529)

Objective ICT-2011.3.1 – Very advanced nanoelectronic components: design, engineering, technology and manufacturability

Summary					
No and name	**D5.2.1 – Mid-term Dissemination Report**[1]				
Status	Released	**Due**	Month 18	**Date**	31-Mar-2014
Author(s)	Nicolás Cordero				
Editor	Nicolás Cordero				
DoW	Report on the Dissemination and Communication activities carried out by the PowerSWIPE consortium during the first 18 months of the project				
Dissemination Level	**PU - Public** **PP – Programme Restricted** (Only for other programme participants) **RE – Restricted** (Only for a group specified by the consortium) **CO – Confidential** (Only for members of the consortium)				
Nature	Report				

Document history			
V	**Date**	**Author**	**Description**
Draft	2-Apr-2014	N.C.	Draft
1.0	8-Apr-2014	N.C.	First release
1.1	24-Apr-2014	N.C.	Additional information from project partners
1.2	28-Apr-2014	COM	Minor updates

Related documents: Deliverable D5.1, “Project Website”

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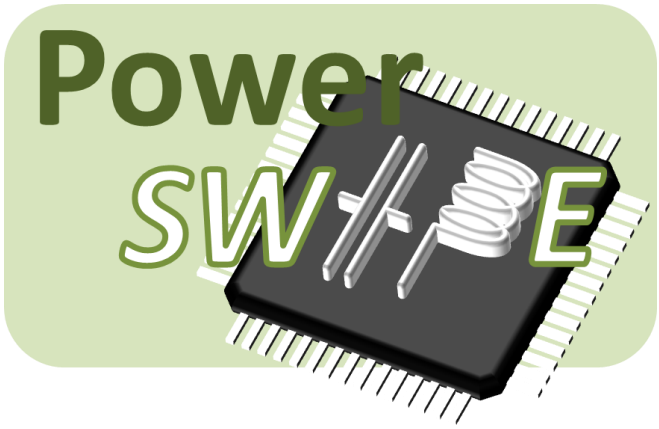
1. Table of Contents

2. Publishable Summary

The PowerSwipe project addresses a key roadblock for PowerSoC by, for the first time, miniaturising and integrating state-of-the-art, high density trench capacitor substrate technology with novel thin film magnetics on silicon to deliver a multi-component LC (inductor-capacitor) interposer which will be combined, in a 3D heterogeneous stack, using eWLB technology, with the µController chip.

The main dissemination objective during the first three months of the project was the development of a project Web site. For more details, please check Deliverable D5.1., or go to http://www.powerswipe.eu

As part of the Web development, a project logo and a project banner were also designed.



To give a uniform and easily recognisable project appearance, standard templates for both reports and presentations were also set up.

A LinkedIn group dealing with PowerSoc was also created, with both members and non-member of the PowerSwipe consortium taking part in rewarding discussions on the topic.

Several papers were submitted/presented at relevant conferences: Compel’13, CIPS’14, APEC’14. The consortium is also actively pursuing the preparation of Professional Seminars in conjunction with some of these conferences.

3. Introduction

Dissemination and communication are essential tools to spread the message, outcomes and impact of the project to both the technical and non-technical audiences.

Dissemination activities within the project are facilitated through WP5 that aims at promoting project results to scientific community, industry and general public. Three different dissemination mechanism are used, namely the project website, the organisation of events and the

dissemination through publicity actions. Depending on the nature of the audience in each action, different aspects and information is conveyed achieving maximum outreach and effectiveness.

From month 3 of the project, PowerSwipe has had a dedicated Web site. The Website is used for dissemination of project objectives and results to the scientific and industrial communities and to the public in general.

The consortium actively disseminates research results in the power electronics academic and industrial community through journal and conference publications. Specifically, partners aim at publishing in high impact factor scientific journals.

The PowerSWIPE consortium also aims at organising workshops/tutorials on Power Supply on Chip (PwrSoC) and uses these workshops as a platform for disseminating project results to the scientific community. We also participate at international conferences in power management IEEE APEC, CIPS, COMPEL, etc.) and system integration and SOC for power.

4. Description

During the first half of the project, the Dissemination activities have focussed on:

- Project branding
- Project website
- LinkedIn PwrSoC group
- Conference presentations
- Workshops and exhibitions
- Training: Tutorials and Professional Development Seminars

4.1 Branding

PowerSWIPE designed a logo and banner to give a single easily recognisable project image. This logo is used in all project deliverables and presentations.

Figure 1. Project logo and banner

4.2 Web site

The address for the Project Website is: **http://www.powerswipe.eu.**

The PowerSwipe project consortium has registered the domain name **www.powerswipe.eu** for exclusive use by the project. The consortium will retain this URL for the duration of the project and for at least two years once the project ends (i.e. to end of 2017).

The Website is hosted at the Tyndall computer server. The Website also links to a private document repository (Consortium embers only access) which is hosted by Infineon Austria.

The following figure shows a screenshot of the Home page.

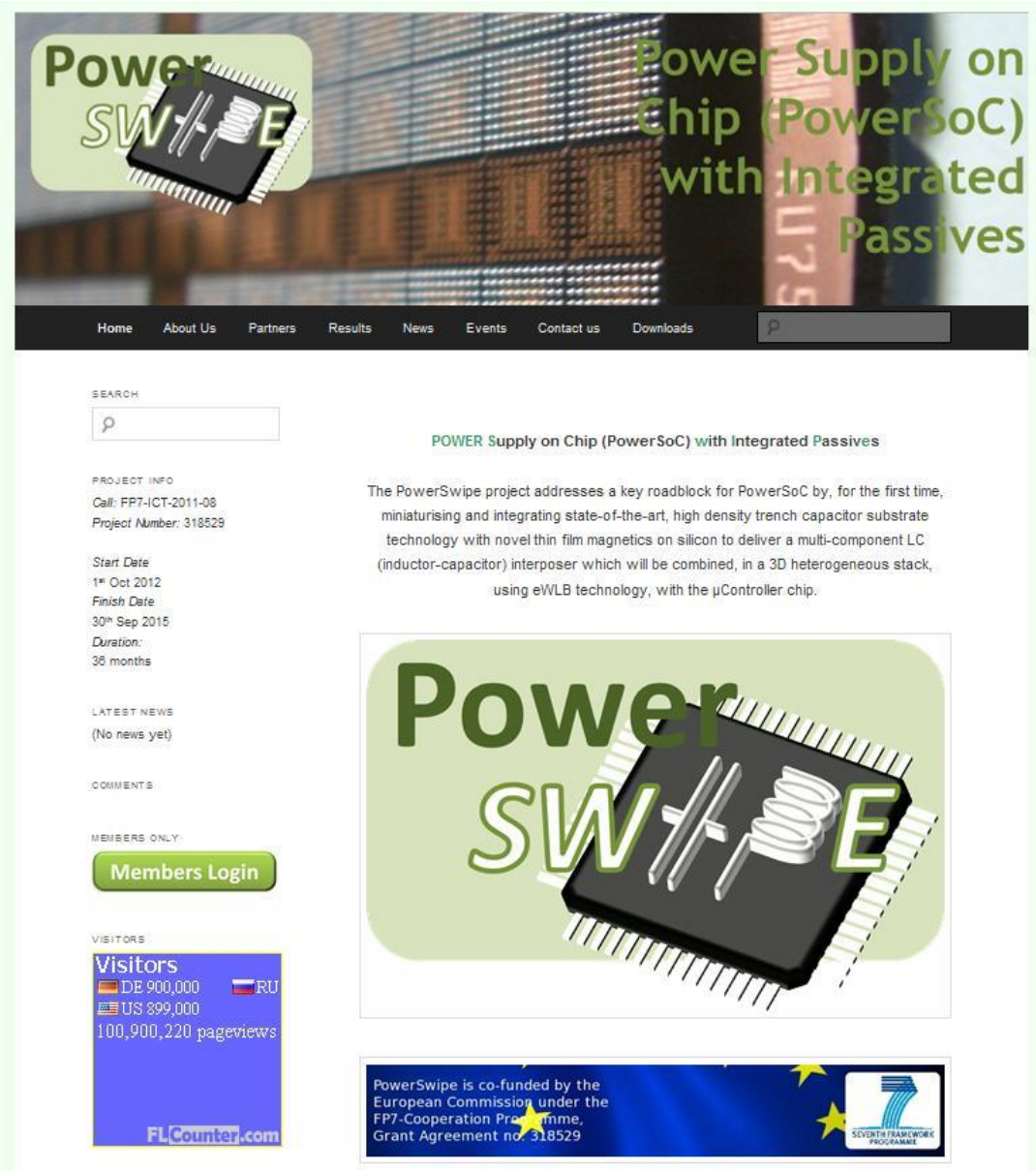


Figure 2. Website Home page

The Website contains the following pages: Home, About Us, Partners, Results, News, Events, Contact Us and Downloads.

4.3 LinkedIn Group

The PowerSWIPE consortium has set up a LinkedIn group on Power Supply on Chip (PwrSoC).

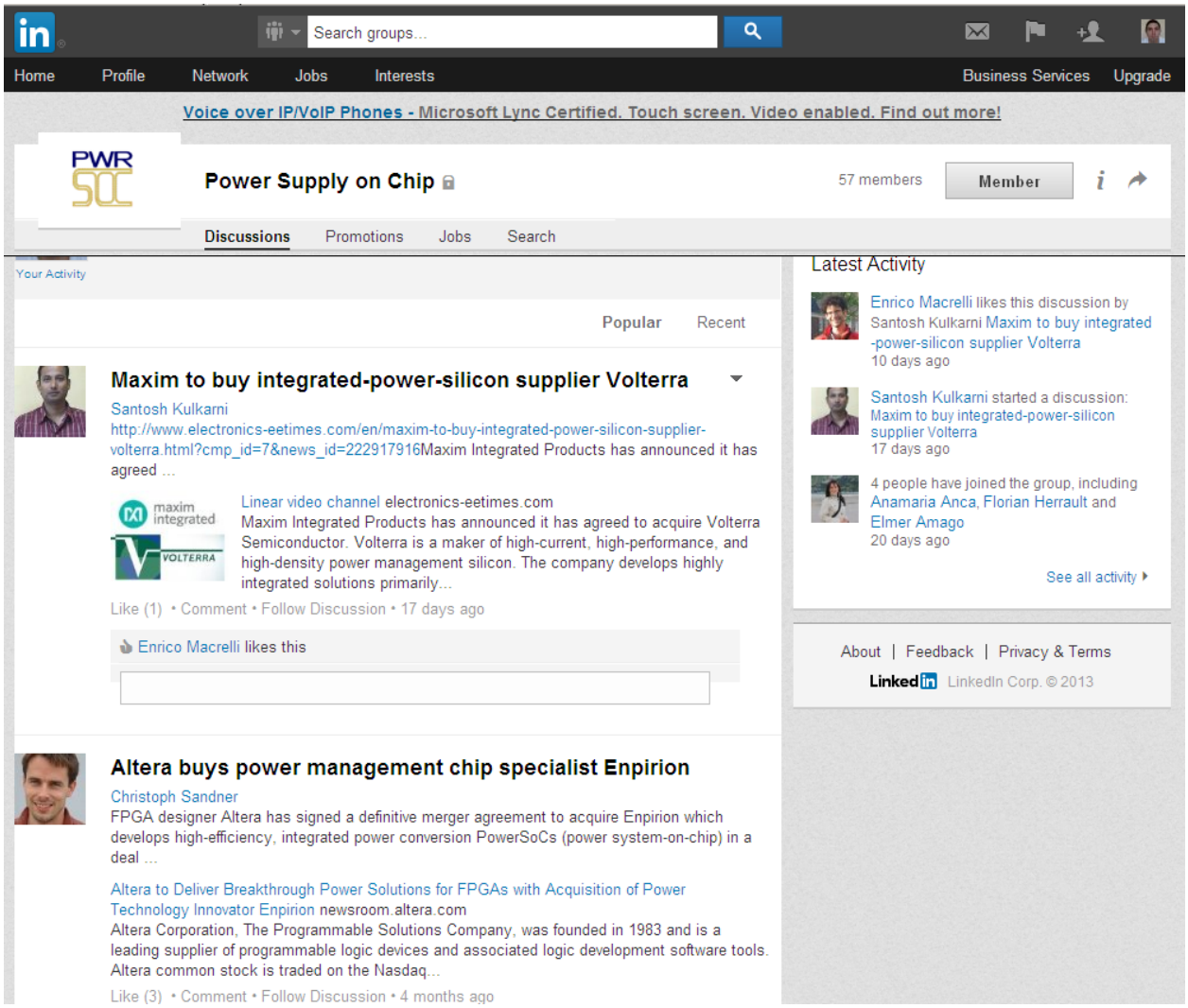


Figure 3. Screenshot of LinkedIn “Power Supply on Chip” group

The membership of the group is open to any professionals working on PwrSoC and related areas (both members of the PowerSWIPE consortium and to non-PowerSWIPE). It currently has 71 members.

The LinkedIn group provides an open forum for discussions on topics related to PwrSoC. Furthermore it gives a quick link to news, updates, and information.

4.4 Journal Editorship

IEEE Trans. Power Electronics, Sept. 2013. Special issue on PowerSoC, Guest editor: C. O'Mathuna

4.5 Conference presentations

COMPEL'13 (14th IEEE Workshop on Control and Modeling for Power Electronics), Salt Lake City, Utah, 23-26 June 2013.

- Cortés, J.; Šviković, V.; Alou, P.; Oliver, J.A.; Cobos, J.A., **"Design and analysis of ripple-based controllers for buck converters based on discrete modeling and Floquet theory"**, IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL), 2013, pp. 1-9.
  DOE: 10.1109/COMPEL.2013.6626474

CIPS'14 (8th International Conference on Integrated Power Electronics Systems), Nuremberg, Germany, 25-27 February 2014. http://conference.vde.com/cips/2014/

- Ó Mathúna, C.; Wang, N.; Kulkarni, S.; Anthony, R.; Cordero, N.; Oliver, J.; Alou, P.; Šviković, V.; Cobos, J.A.; Cortés, J.; Neveu, F.; Martin, C.; Allard, B.; Voiron, F.; Knott, B.; Sandner, C.; Maderbacher, G.; Pichler, J.; Agostinelli, M.; Anca, A.; Breig, M., **"Power Supply With Integrated PassivEs – The EU FP7 Power Swipe Project"** (Invited Paper), Proc. CIPS 2014, Nuremberg, 25-27 Feb 2014, pp. 1-7
  ISBN 978-3-8007-3578-5
- Neveu, F.; Martin, C.; Allard, B., **"Review of high frequency, highly integrated inductive DC-DC converters"**, Proc. CIPS 2014, Nuremberg, 25-27 Feb 2014, pp. 285-91.
  ISBN 978-3-8007-3578-5
- Cortés, J.; Šviković, V.; Alou, P.; Oliver, J.A.; Cobos, J.A., **"Impact of the control on the size of the output capacitor in the integration of Buck converters"**, Proc. CIPS 2014, Nuremberg, 25-27 Feb 2014, pp.1-6
  ISBN 978-3-8007-3578-5

APEC'14 (IEEE Applied Power Electronics Conference and Exposition), Forth Worth, TX (USA), 16-20 March 2014. http://www.apec-conf.org/

- Jorge Cortés, Vladimir Svikovic, Pedro Alou, Jesús A. Oliver and Jose A. Cobos **"Comparison of the Behavior of Voltage Mode, V2 and V2Ic Control of a Buck Converter for a Very Fast and Robust Dynamic Response"**

Cortés, J.; Šviković, V.; Alou, P.; Oliver, J.A.; Cobos, J.A.,: ***Best Poster Award at CIPS'14 and Best Poster Award at APEC'14***

4.6 Workshops and exhibitions

- Poster at Infineon AMPS Symposium Graz, 13th - 14th May 2014
- CNRS Workshop on “Integration in Power Electronics” (24th June 2013) **“Power Supply on Chip – The Next Generation of Integrated Power Management”**.
- Poster @ Univ of Lyon Science & Technology Energy exhibition (http://jsf2013.univ-lyon1.fr/) (in French)
- IFAT Poster/Talk @ PowerSoC Conference Boston, October 2014

4.7 Training: Tutorials, Professional Development

Over 110 attendees took part in the Professional Development Seminar on Power Supply on Chip organised by the PowerSwipe Consortium during APEC’2014.

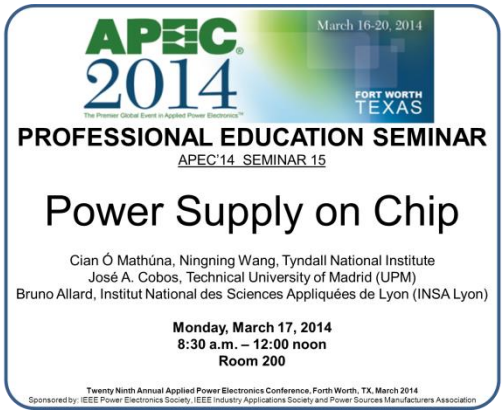


Figure 4. Announcement and lecture by Prof. Cobos during APEC’14

5. Conclusions

The PowerSWIPE consortium has been very active on Communication and Dissemination activities, including the project Website, the setting up of the LinkedIn group, technical publications and seminars.

The Website is up and running and attracts a large number of visitors (visitor counter by nationality is built in the Home page). The Website includes a Feedback section, however this had been disappointing as no query has been received yet.

The Power Supply on Chip LinkedIn group has attracted a large number of members and is becoming a very useful tool for news, updates and to share information about the project in particular and the PwrSoC area in general.

The consortium has already presented 5 papers at conferences, which led to publications in the corresponding Proceedings. Furthermore, the consortium currently has two papers which have been accepted for publication in refereed journals, plus more submissions to upcoming conferences.

Finally, the Professional Development seminar at APEC’14 was a large success, and the material developed for this training course can now be used again at other events. In particular, the consortium is considering running it as a stand-alone training course in Europe.