
**PowerSWIPE (Project no. 318529)**

**"POWER SoC With Integrated PassivEs"**

# Deliverable 6.1.2

# "Second Annual Management Report"

**Dissemination level: PU**

**Responsible Beneficiary**
**Tyndall**

**Due Date**
**30th September 2014**

**Submission Date**
**28th November 2014**

| Summary | | | | | |
|---|---|---|---|---|---|
| **No and name** | **D6.1.2 – Second Annual Management Report**[1] | | | | |
| **Status** | Released | **Due** | Month 24 | **Date** | 30-September-2014 |
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| **Editor** | Cian Ó Mathúna | | | | |
| **DoW** | Report on Project Management from Oct 2013 to September 2014 | | | | |
| **Dissemination Level** | **PU - Public** | | | | |
| **Nature** | Report | | | | |

| Document history | | | |
|---|---|---|---|
| **V** | **Date** | **Author** | **Description** |
| Draft | 18-Oct-2014 | N.C. | Draft |
| 1.0 | 15-Nov-2014 | N.C. et al. | Inputs from all partners for WP reports |
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# 1. Table of Contents

## 2. PROJECT PERIODIC REPORT

**Grant Agreement number:** 318529

**Project acronym:** POWERSWIPE

**Project title:** Power System-on-Chip (SoC) with Integrated Passives

**Funding Scheme:** FP7-ICT-2011-8

**Date of latest version of Annex I against which the assessment will be made:** 4th September 2012

**Periodic report:** **1st** ☐ **2nd** ■ **3rd** ☐

**Period covered:** **from** 1st October 2013 **to** 30th September 2014

**Name, title and organisation of the scientific representative of the project's coordinator[2]:** Prof. Cian O'Mathuna, Senior Research Scientist, Tyndall National Institute, University College Cork

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**Project website[3] address:** www.powerswipe.eu

[2] Usually the contact person of the coordinator as specified in Art. 8.1. of the Grant Agreement.

[3] The home page of the website should contain the generic European flag and the FP7 logo which are available in electronic format at the Europa website (logo of the European flag: http://europa.eu/abc/symbols/emblem/index_en.htm logo of the 7th FP: http://ec.europa.eu/research/fp7/index_en.cfm?pg=logos). The area of activity of the project should also be mentioned.

## 3. Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project (tick as appropriate) [4]:
  - ■ has fully achieved its objectives and technical goals for the period;
  - □ has achieved most of its objectives and technical goals for the period with relatively minor deviations.
  - □ has failed to achieve critical objectives and/or is not at all on schedule.
- The public website, if applicable
  - ■ is up to date
  - □ is not up to date
- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project (section 3.4) and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 3.2.3 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of scientific representative of the Coordinator: .....

Date: ...../ ...../ .....

For most of the projects, the signature of this declaration could be done directly via the IT reporting tool through an adapted IT mechanism and in that case, no signed paper form needs to be sent

[4] If either of these boxes below is ticked, the report should reflect these and any remedial actions taken.

## 3.1 Publishable summary

### 3.1.1 Description of project context and objectives

Combing high efficiency with cost-effective but high level of integration is the major driver in power electronics today. PowerSwipe responds to the call for “advanced More-than-Moore elements” and “their integration and interfacing with existing technology” by aiming to develop innovative Power Supply in Package (PwrSiP) and Power Supply on Chip(PwrSoC) technology platforms through highly integrated passives and advanced CMOS. The PowerSwipe concept addresses the key challenges of "systemability", "integratability" and "manufacturability" for System on Chip (SoC) power management platforms.

An advanced design optimization tool will be developed with both component and system perspective. PowerSwipe will leverage the existing expertise of the consortium in the area of integrated passive and power management design to achieve a first integrated system-level design tool for SoC applications. Additionally, High-volume MEMS manufacturing processes for the monolithic power passives will be developed to enable deployment of the technologies in commercial applications. A custom PwrSiP/PwrSoC will be developed to maximise the system performance in high volume silicon technology. On-chip intelligence will enable system performance to be optimised for different applications. A top-down system design approach will take full advantage of the benefits of the integrated magnetic and capacitive components while resolving issues due to smaller absolute component values, higher switching losses and increased on-chip interference and coupling.

Two intermediate test Vehicles and two demonstrators will address a target applications (e.g. automotive) and system requirements (efficiency, performance, reliability/lifetime, cost, size). The project aims to establish Europe as the leading global player over the coming decade in this emerging space by creating a competitive, European supply chain in Power Supply platform for System on Chip applications with no major missing links.

### 3.1.2 Description of work performed since the beginning of the project and main results achieved so far

Tasks performed since the beginning of the project

**Year 2:**

- Finalise all the IC designs: LV, HV and HF DCDC
- Tapeout and fabrication of ICs
- Analysis and optimisation of chosen architectures and selected blocks
- Improvement of models
- Passives (inductor, capacitor and interposer) fabrication
- Inductor technology transfer
- Maintenance of project Web site. Dissemination activities (seminars, presentations, publications)

**Year 1:**

- Definition of target application requirements
- System architecture, block-level optimisation and integrated circuit design
- System level analysis and optimisation
- Analysis and optimisation of integrated passives
- Passives (inductor, capacitor and interposer) process development
- Inductor technology transfer
- Development of project Web site

Achieved milestones

**Year2:**

- Ms2.3 – Detailed analysis and optimisation of individual blocks for the selected architectures (Month 18)
- Ms1.3 – Tape-out first prototype chips. Error-free GDSII layout in time (Month 21)
- Ms3.1 – Passive components ready (Month 23)

**Year1:**

- Ms1.1 – Application requirements defined (Month 3)
- Ms1.2 – First system architecture (Month 9)
- Ms2.1 – Architecture analysis and evaluation (Month 12)
- Ms2.2 – Analysis and optimisation of integrated passives (Month 12)

Completed and submitted deliverables

**Year 2:**

- D2.3 – Analysis and optimisation of selected architecture (Month 18)
- D5.2.1 – Mid-term dissemination report (Month 18)
- D1.3 – Design report of first prototype chips (Month 21)
- D3.2 – Passive components fabricated (Month 23)
- D2.4 – Architecture optimisation of 1st prototype chips (Month 24)
- D2.5 – Analysis and optimisation with improved models (Month 24)

**Year 1:**

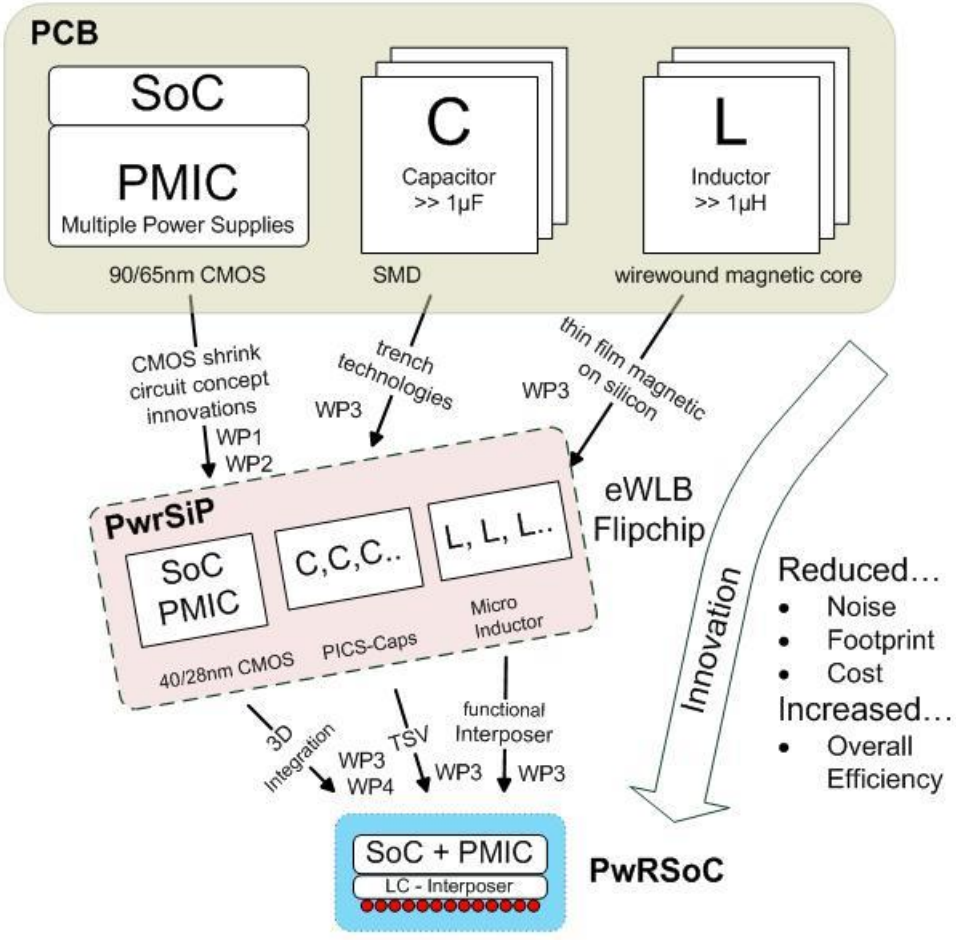
- D5.1 – Project Web site (Month 3)
- D3.1 – Inductor process documentation ready for transfer (Month 6)
- D1.1 – First system architecture description (Month 12)
- D1.2 – Target block-level specification (Month 12)
- D2.1 – Analysis and evaluation of first system architecture (Month 12)
- D2.2 – Analysis and optimisation of integrated passives (Month 12)

### 3.1.3 Expected final results and their potential impact and use (including the socio-economic impact and the wider societal implications of the project so far)

PowerSwipe will develop ...

- ... a demonstrator, consisting of multi-component LC (inductor-capacitor) interposer, which can be combined in a 3D heterogeneous stack together with the SoC/PMIC chip

- ... integrated passive components fulfilling the stringent temperature (125deg) and quality requirements required by the automotive market and thus closing today’s gap in availability of components
- ... inductor and capacitor based very high-frequency DC-DC converters in 40nm CMOS operating at 5V supply, ready for 3D integration with power passives
- ... integrated very high-frequency DC-DC converters allowing PCB footprint reduction by ~100mm² per module, without compromising converter efficiency at 90%
- ... missing system and component level optimization tools to achieve optimum system configuration and efficiency for different operating modes
- ... a demonstrator system targeted for Automotive Microcontroller, with optimized complete chain from car battery (5...48V) down to the core voltage domain (1V)




*System level schematic of the PowerSwipe project innovations*

### 3.1.4 Project website, logos and partners

Project Website:

**www.powerswipe.eu**

Project logo:

Project banner:


Project partners:

| Participant no. * | Participant organisation name | Part. short name | Country |
|---|---|---|---|
| 1 (Coordinator) | University College Cork, National University of Ireland, Cork | Tyndall-UCC | IE |
| 2 | Infineon Technologies AG | IFX | DE |
| 3 | Infineon Technologies Austria AG - Villach | IFAT | AT |
| 4 | IPDiA | IPDiA | FR |
| 5 | Universidad Politécnica de Madrid | UPM | ES |
| 6 | Robert Bosch GmbH | Bosch | DE |
| 7 | Université de Lyon, Claude Bernard | UCBL | FR |

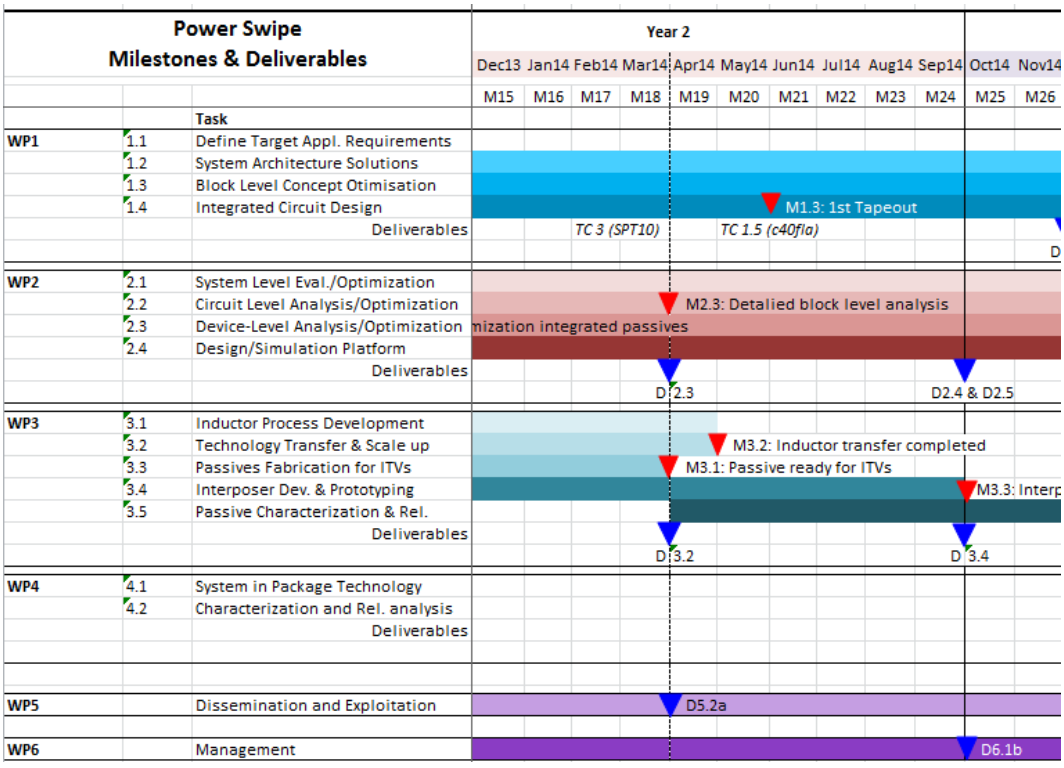
## 3.2 Core of the report for the period: Project objectives, work progress and achievements, project management

### 3.2.1 Project objectives for the period

The main objectives of the PowerSwipe project for Year 2 for were:

- Integrated circuit design and fabrication
- System level analysis and optimisation
- Analysis and optimisation of integrated passives
- Fabrication of passives (inductor, capacitor and interposer)
- Inductor technology transfer
- Maintenance of project Web site. Dissemination activities (seminars, presentations, publications)

The following figure shows the Gantt chart with the tasks, deliverables and milestones for the period (Original workplan. See Project Management section for updated plan).



### 3.2.2 Work progress and achievements during the period

Concise overview of the progress of the work in line with the structure of Annex I to the Grant Agreement.

## WP1 – System Specifications and Design

### WP Objectives for Year 1

- Finish the LV DCDC, HV DCDC, HF DCDC design
- Tapeout LV DCDC, HV DCDC and HF DCDC

### Work Progress

***Tasks finished***

- **Deliverable 1.3 “Design report of first prototype chips”**

### Achievements

## Demo1a – Full power management chip

**Summary**

The implemented Demo1a test chip is a complete, fully integrated power management chip for supplying automotive microcontrollers. The chip contains an integrated inductor based DC-DC buck converter and an integrated switched capacitor DC-DC converter. Beside the converters additional auxiliary circuits are placed: linear voltage regulators, different oscillators, bandgap references, current references, ADCs, temperature sensors, startup circuits.

Furthermore, an artificial load is placed on the chip in order to emulate steep current jumps from a microcontroller load. The current ramps of the load are programmable and can be controlled by external control signals.

**Block Diagram Demo1a**

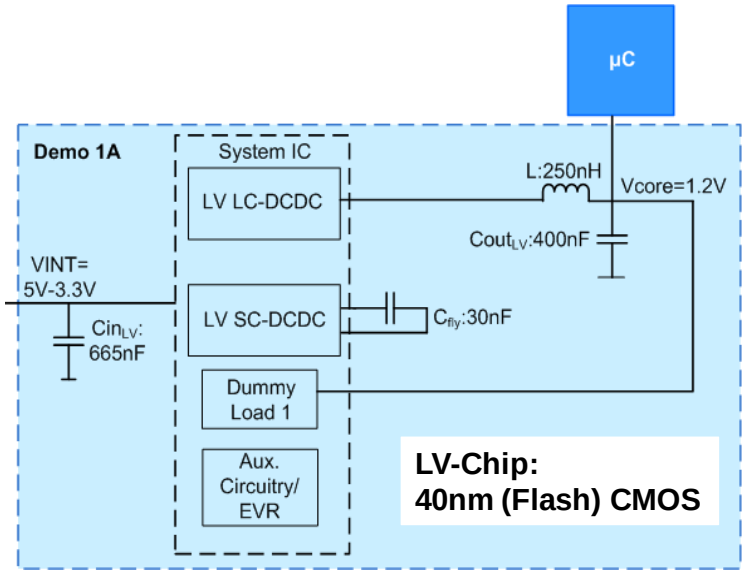



*Figure 1.1: Block diagram of the fully integrated power management chip Demo1a*

**Layout of Demo1a**

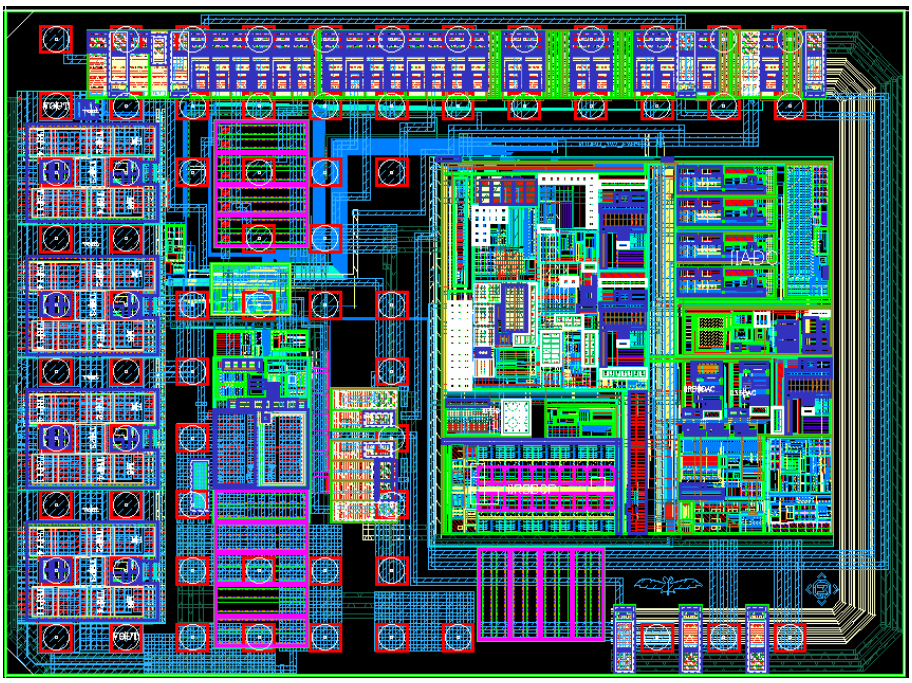


*Figure 1.2. Demo1A layout*

**External components**

The external capacitors and inductors used for the circuits are implemented on the interposer that is within the chip package. $C_{IN}$ = 665nF, $C_{OUT\_LV}$ = 400nF, $C_{OUT\_SC}$ = 260nF, $C_{fly}$ = 30nF, $L_{LV}$ = 250nH.

**Implemented Switched Mode Power Supplies**

Two different types of power converter were developed during this project. The first one is a Switched Capacitor DC-DC converter (SC DC-DC) and the second one is an inductor based DC-DC converter (LC DC-DC).

**a. SC DC-DC Converter**

The designed switched capacitor DC- DC converter is implemented as a four phase interleaved converter. It converts a 5V or 3.3V input voltage down to 1.3V or 1.2V with a typical efficacy of 75%. The converter can handle load currents up to maximum 200mA with dynamic load jump of 50mA/20ns.

Figure 1.3 shows the top level block diagram of the designed switched capacitor DC-DC converter. It consists mainly of four switched capacitor unit stages, a voltage comparator, a start-up current source and the Pulse Frequency Modulation (PFM) controller. The power flow from the converter input to the output is highlighted in red and buffered by the input capacitor Cin and the output capacitor Cout.

The four times placed unit stage includes a switch network, a chain of buffers and a level-shifter block. The switch network illustrated in Figure 1.4 is the core of the converter and consists of nine power switches and two flying capacitors. Out of that, two different gain modes (1/2 and 1/3) are realized to convert the input voltage down to the output voltage. Each of the nine power switches is driven by its own buffer circuit, which get its input signal from the level-shifter block. Inside the level shifter block, a switching signal coming from the controller is decoded depending on the gain mode into nine individual switching signals.

To regulate the output voltage, a voltage comparator is implemented which monitors the output voltage and compares it with an internal generated reference voltage. The output signal of the comparator is used inside the controller to generate the Pulse Frequency Modulated (PFM) switching pulses. These switching pulses are further on converted into four time interleaved signals, which controls the four unit stages. In Addition, a digital Finite State Machine (FSM) is implemented which controls the start-up and puts the converter into normal operation or into different debugging modes.

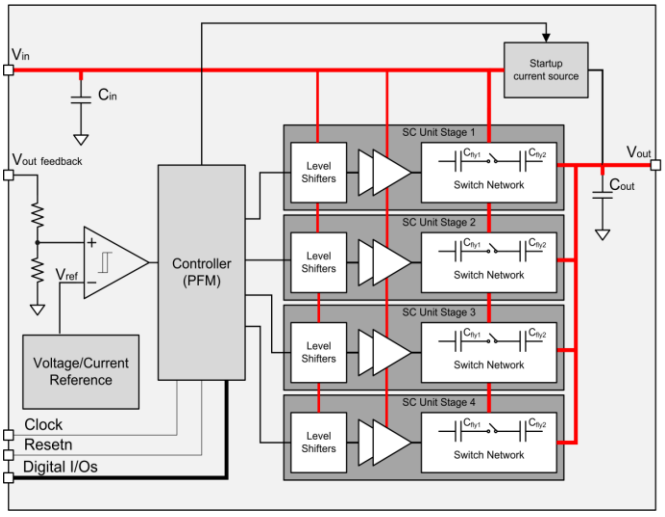



*Figure 1.3: Block diagram switched capacitor DC-DC converter*

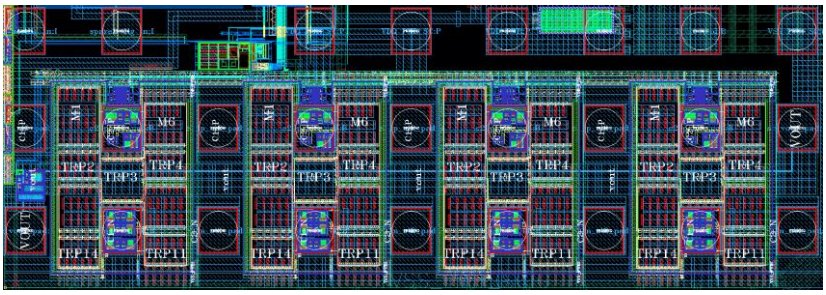


*Figure 1.4: Switched Capacitor DC-DC converter chip layout*

**b. LV DC-DC Converter**

The high frequency inductor based DC-DC converter provides load currents up to 500mA at an output voltage of typical 1.2V. The converter supports Pulse Width Modulation – Continuous Conduction Mode, Pulse Width Modulation – Discontinuous Conduction Mode and Pulse Frequency Modulation in order to guarantee high power conversion efficiencies over the whole specified load range.

The output filter of the converter consists of a 250nH power inductor and a 400nF capacitor – both passives are integrated in the chip package. At the typical load the target efficiency of the converter is 85% at a switching frequency of 10MHz.

The Inductor Based DC-DC buck converter (LV DC-DC) steps down a 5V or 3.3V input voltage to a stable 1.2V or 1.3V output voltage in a very efficient way. A simplified block diagram of the converter is shown in Figure 1.5. Large 5V capable PMOS power devices and NMOS power devices are connected in half bridge configuration. The switching node (sw) of the half bridge is connected to a second order low pass filter. The filter is composed of a 250nH power inductor (L) and a 400nF output capacitor (Cout). Both passives are integrated into the package.

The power devices are driven by strong and fast tapered buffers which are controlled by a finite state machine in the power stage (Power Stage Control). In order to save power the state machine is implemented with low voltage transistors in the 1.2V core power domain. Therefore, level shifters are required as interface between the signals from the state machine and the 5V power stage. The level shifters are very fast over PVT, this allows to control the power devices in a very accurate way. Furthermore, the shifters are implemented very robust and without any static current consumption.

An analogue peak current controller is used for controlling in PWM mode. The controller is realized as a transconductance amplifier with an integral part. The actuating variable of the controller set the peak current through the power inductor. The measuring of the peak current is done by means of a current sense block beside the PMOS power device. The current sensing is done lossless with a sense-FET topology (no sense resistor). The output of the converter can be programmed: Typical output voltages are 1.2V or 1.3V.

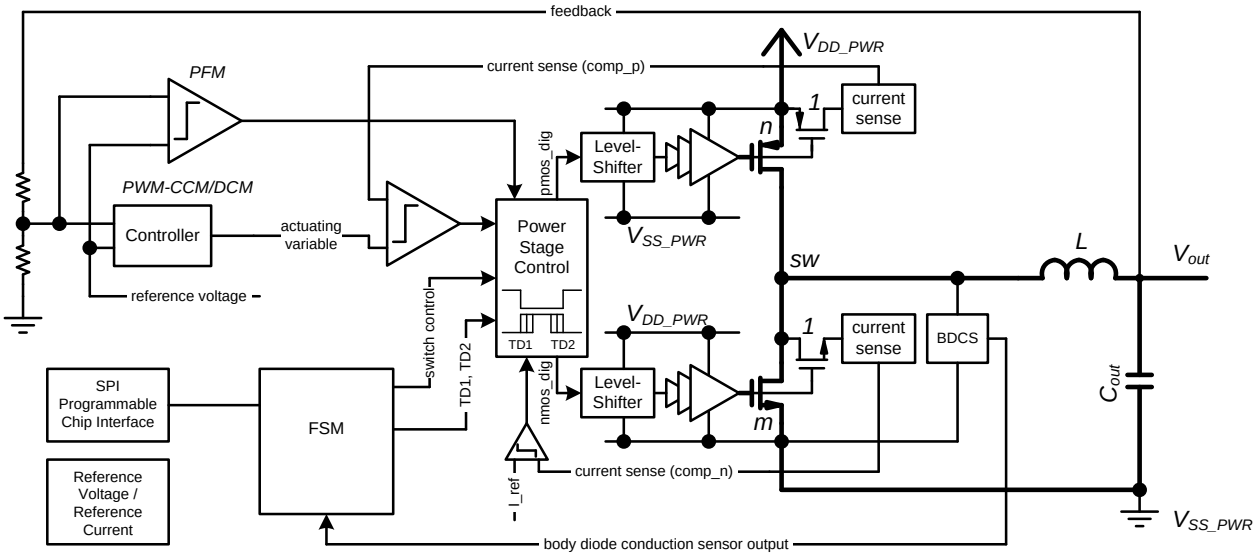



*Figure 1.5: Block diagram of the inductor based DC-DC converter*

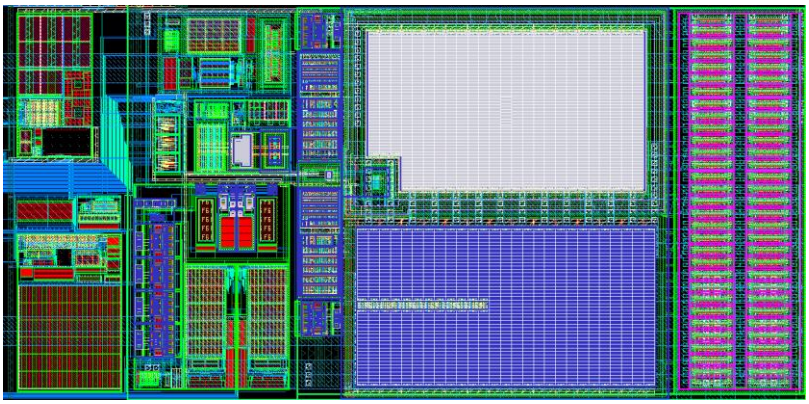


*Figure 1.6: Switched Capacitor DC-DC converter chip layout*

## High-voltage DC-DC Converter (power stage only)

### Summary

The HV DC-DC converter is an inductor-based step-down regulator that operates at a frequency of 10MHz. At the moment only the power stage has been implemented on silicon. The controller will be implemented externally in the future.

The acceptable input voltage range goes from 6V to 16V while the output voltages for which the design has been optimized are 3.3V and 5V. The maximum output current is 500mA.

### Block Diagram

Figure 1.7 shows the block diagram of the implemented design.

The power stage itself consists of a low-side switch and a high-side switch which are both 20V NMOS devices.

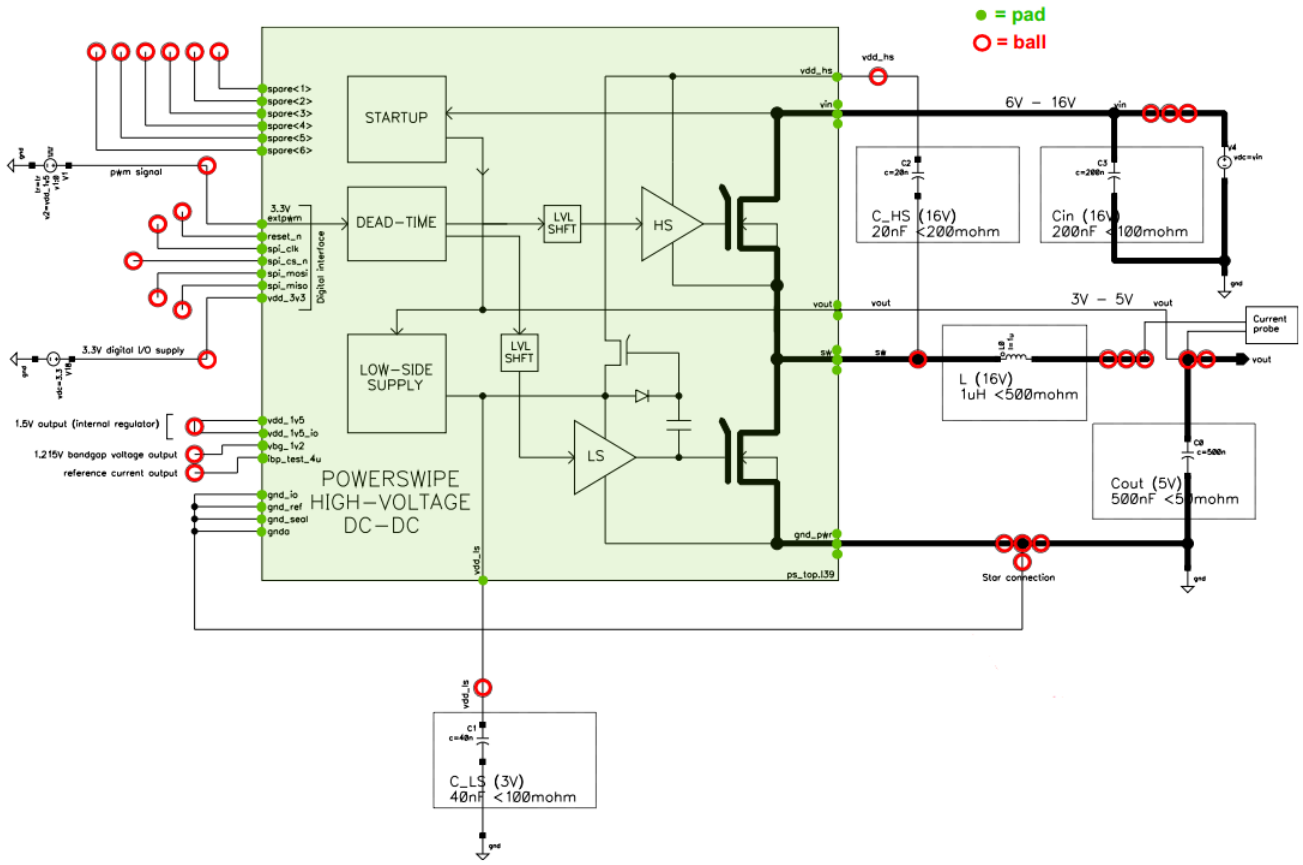



*Figure 1.7. Block diagram of implemented design*

**Description of operation**

The PWM signal driving the power stage can be either provided from outside (from an external controller) or generated internally (for open loop testing). In the latter case the duty cycle can be programmed through SPI.

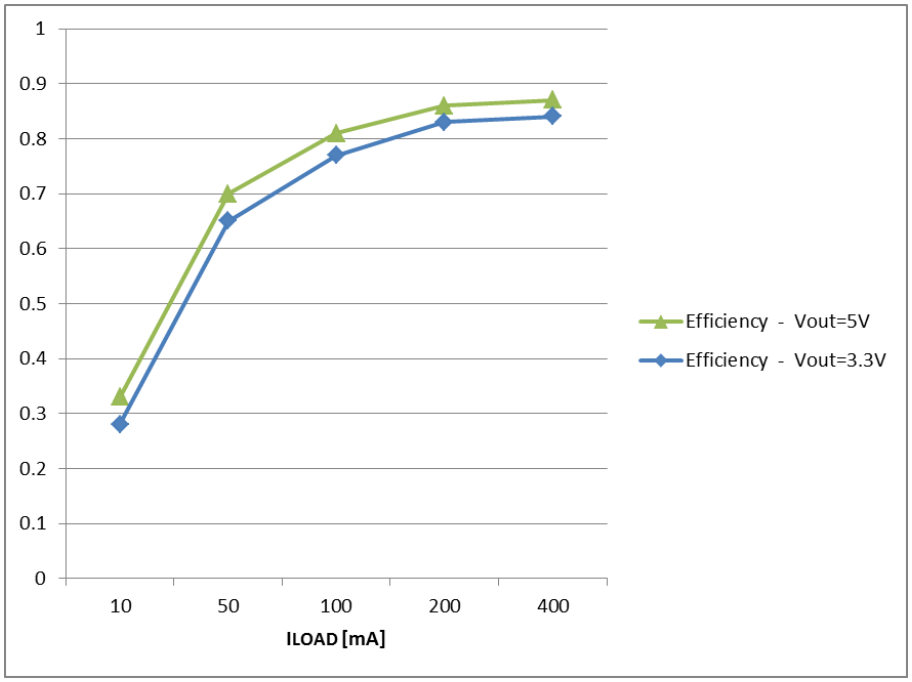
The supply for the low-side switch driver is generated by an LDO (the “low-side LDO”) which in turn is supplied by the regulator output voltage (for higher efficiency). Because the output voltage is initially low at startup another LDO (“the Startup LDO”) will pre-charge the output capacitor to 3V before the switching begins.

An external bootstrap capacitor generates a voltage (higher than $V_{IN}$) from which the high-side driver is powered.

**External components**

The external capacitors are integrated on a separate die that will be enclosed in the same package as the regulator IC: $C_{IN}$ = 200nF, $C_{OUT}$ = 1µF, $C_{LS}$ = 40nF, $C_{HS}$ = 20nF.
The 1uH inductor is a separate component that is also enclosed in the package.

**Simulated efficiency**




Vin=12V, ESRL=500mΩ, ESRCOUT=50mΩ, ESRCHS=100mΩ, ESRCLS=50mΩ
(open loop operation, controller power consumption not included)

*Figure 1.8. Simulated efficiency*

**Layout**

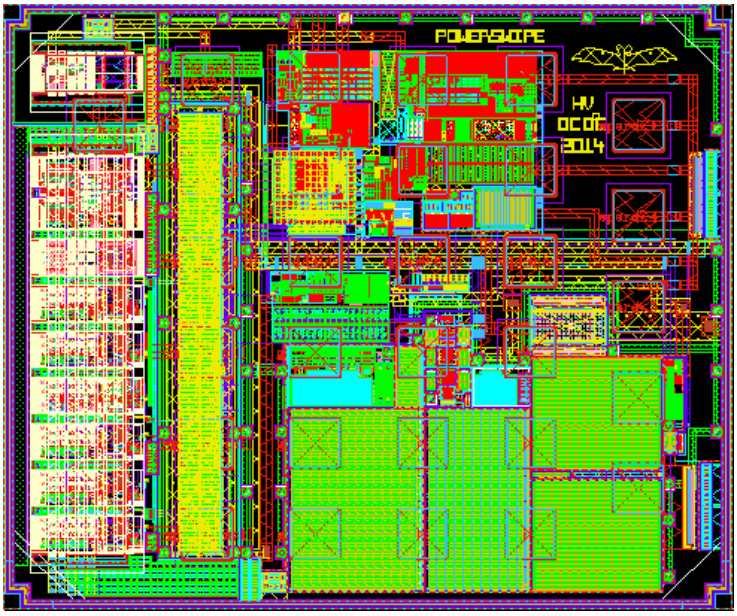



*Figure 1.9. HV DC-DC converter layout*

## High Frequency DCDC

### Summary of progress towards objectives and details for each task

The main objective was to get to the Intermediate Test Vehicles (ITVs). These ITVs are including converters using standard and cascode power stage, and converter with 1 and 2 phases. This means that to get to the ITVs several tasks were required: the optimization of the capacitive interposer, the optimization of an output filter for a 2-phase converter, the design of converters with standard and cascode power stage (1- and 2-phase configurations for both) with all the necessary blocks, and the layout (physical implementation) of these converters.

### Capacitive interposer optimization

Based on considerations from 1st interposer and active components needs for decoupling, the interposer has been redesigned and optimized.

The main changes are:

- Reducing ground net parasitic inductance
- Adding 1 decoupling capacitor for a voltage reference
- Moving 1 active pad for to be more compact on active die

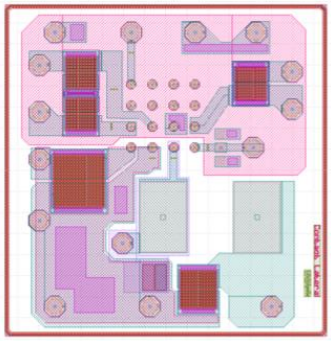
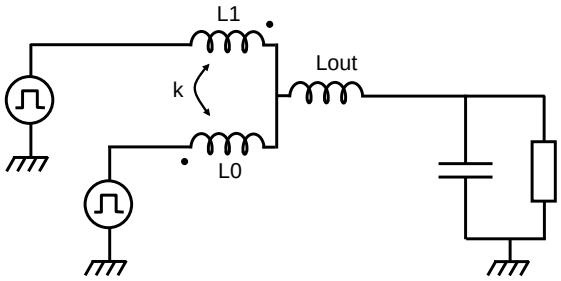


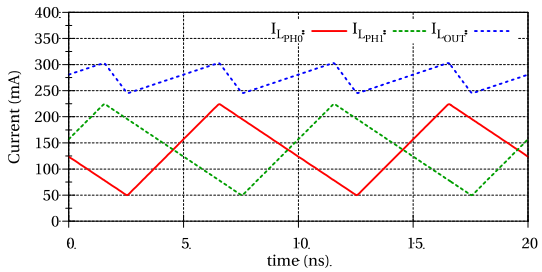
*Figure 1.10: Optimized capacitive interposer*

### Output filter optimization for a 2-phase converter

The output filter has been optimized in order to minimize the phase current ripple given a total inductance value (90 nH)



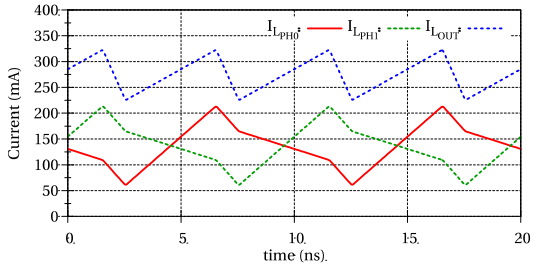

Structure used of output inductors optimization




Case 1: No coupling and no output inductor

Optimization results:

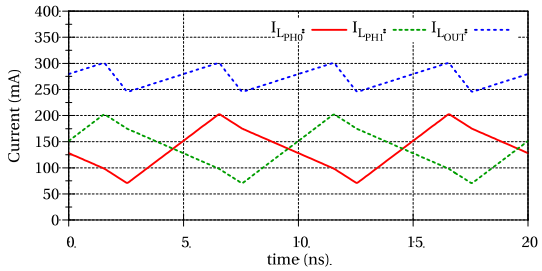
- k=0, $L_{OUT}$=0nH, $L_{PH}$=45nH
- Phase current ripple: 172mA
- Ripple reduction vs. previous case:0%




Case 2: Coupling and no output inductor.

Optimization results:

- k=0.4, $L_{OUT}$=0nH, $L_{PH}$=45nH
- Phase current ripple: 151.4mA
- Ripple reduction vs. uncoupled:12%




Case 3: coupling and output inductor.

Optimization results:

- k=1, $L_{OUT}$=20nH, $L_{PH}$=35nH
- Phase current ripple: 123.8mA
- Ripple reduction vs. uncoupled:28%

**Design and optimization of converters: cascode and standard**

**Standard converters and sub-blocks**

The power stage of the standard converter has been optimized in order to enhance efficiency at the nominal power point. The optimization has been carried out for a 1-phase (336 mW) and a 2-phase (168 mW per phase) configuration, at 100 MHz ant 200 MHz switching frequency.

**Optimized power stage efficiency for 3.3V to 1.2V configurations:**

- 200MHz, 336mW ➔ 80.06%
- 200MHz, 168mW ➔ 80.05%
- 100MHz, 336mW ➔ 85.48%
- 100MHz, 168mW ➔ 85.90%

Sub-blocks required for this power stage to operate properly are the non-overlapping, synchronized tapered drivers and the level shifter with its current source. These blocks have been designed and optimized for high frequency operation.

**Cascoded converters and sub-blocks**

The power stage of the cascode converter has been optimized in order to enhance efficiency at the nominal power point. The optimization has been carried out for a 1-phase (336 mW) and a 2-phase (168 mW per phase) configuration, at 100 MHz ant 200 MHz switching frequency.

**Optimized power stage efficiency for 3.3V to 1.2V configurations:**

- 200MHz, 336mW => 88.10%
- 200MHz, 168mW => 88.25%
- 100MHz, 336mW => 91.70%
- 100MHz, 168mW => 92.05%

Sub-blocks required for this power stage to operate properly are the non-overlapping, synchronized tapered drivers and the level shifter with its current source. These blocks have been designed and optimized for high frequency operation.

**Converters implementation**

The optimized converters have been implemented using 40 nm CMOS technology. This resulted in 2 dice of 0.9 mm x 0.9 mm. The dice have been delivered in July 2014.

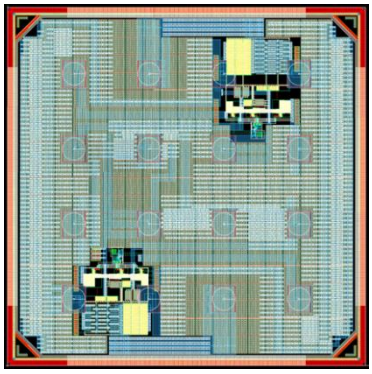


*Figure 1.11: Layout of the chip with cascode converters*

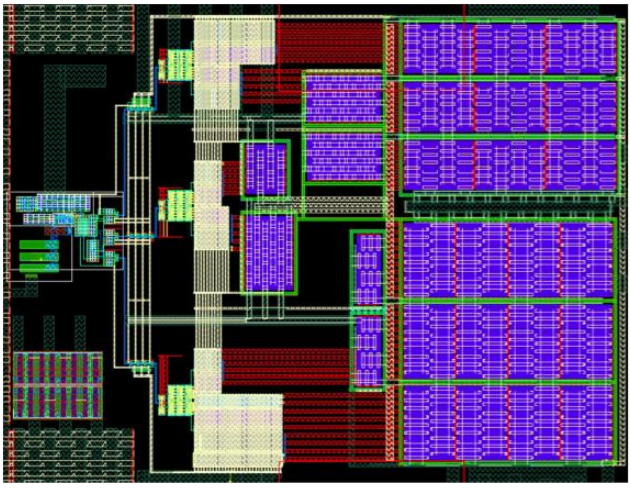


*Figure 1.12: Zoom on 100MHz cascode converter*

## WP2 – Computer-aided Optimisation and Analysis

### Work Package Objectives

The objectives for WP2 for year 2 were:

- To provide detailed optimization results and the analysis of the selected architectures. The optimization and analysis are based on the CAD analysis and optimization tool described in D2.1 developed within this project.
- To provide detailed optimization results of the individual blocks selected in this project:
  - The HV DC-DC converter that reduces the battery input voltage that can vary from 16V to 6V to an output voltage of either 5V or 3.3V. The PMIC will be implemented in BCD-CMOS technology.
  - The LV DC-DC converter will supply the µController Core (1.2V) from the intermediate voltage generated by the HV DC-DC.
  - The SC DC-DC converter will generate a controllable output voltage of 1.3V from the intermediate input voltage (5V or 3.3V).
  - The HF DC-DC converter will scale down an intermediate voltage of 3.3V to 1.2V using high switching frequency techniques (100MHz-200MHz).
- To improve the analytical models of the integrated inductors including high frequency effects (skin and proximity) not accounted the first year.
- To include accurate analytical models of integrated coupled inductors to analyse and optimize two phases buck converters with coupled inductors
- To develop the optimization algorithms for two-phase coupled inductors buck converters including the accurate models of the inductors
- To improve the semiconductors model losses based on accurate simulations on CADENCE
- To adapt the integrated capacitor models for the optimization of the Switched Capacitor Converter SC DC-DC.
- Refinement of the Matlab model of the plant of the SC DC-DC
- Development of the Controller of the SC DC-DC in Matlab
- Design and optimization of the HF DC-DC Power Management IC
- Optimization of the cascoded power stage and standard power stage → refined eff. figures for power stage + 1st driver:
  - Design of clock level shifters and synchronization
    - Constraints: high frequency (200 MHz), high timing accuracy (~100ps), high slew rate (~100ps) and low power
  - Output filter optimization (1phase, 2 phases and 2 coupled phases, assuming ideal inductors) ➔ higher inductances gives better efficiency

### Work Progress

Regarding WP2 all the objectives for the second year has been met.

- The system level optimization tool has been improved with more accurate models of the inductors and the semiconductor losses.
- New fast ripple based controllers have been added to the optimization tool that allows improving the dynamic response and reduce the output capacitance to be integrated.
- MOSFETs models have been improved and extensively validated comparing the results of the optimization tool with accurate CADENCE simulations.
- The device level optimization tool for the optimization of the magnetic components has been improved with more accurate models including:
  - Proximity losses

    - Skin losses
    - Eddy current losses in the magnetic material
    - Hysteresis losses in the magnetic material
- New models for coupled inductors including all the previous effects.
- Validation of the new magnetic models by means of finite element analysis.
- Analysis and optimization of the selected architectures based on the models developed
- Detailed analysis and optimization of each converter based on the developed optimization tool.

## Significant Results

- Improvements on the System level optimization tool based on models of the main components (magnetics, capacitive, parasitic interconnections and power devices). This tool allows optimizing and analysing:
    - Addition of multiphase coupled inductors topology in the optimization
    - Improved models of semiconductors
    - Addition of different operation modes: Continuous Conduction Mode, Discontinuous Conduction Mode and Burst Mode for improving energy efficiency at light load for multiphase coupled inductors
    - Addition of ripple based controllers
- Improved characterization procedure of the power semiconductor devices based on accurate CADENCE simulations to estimate conduction and dynamic losses in the system level optimization. Extensive validation
- Improvement of Power Inductor optimization tool. This tool helps on the detailed optimization of the power inductor selected by the System Level optimization tool:
    - More accurate analytical models including skin and proximity effects
    - More accurate models for core losses
- Integrated Capacitor SPICE model development to account for parasitic effect for Switched Capacitor Converters.
- Improved modelling of the SC DC-DC in MATLAB
- Controller design and optimization of the SC DC-DC in Matlab
- Accurate equivalent circuit of integrated capacitor to account for the losses and ripple in the system level optimization
- Placement of VHF DC-DC converter on state-of-the-art landscapes to highlight novelties and challenges of the design
- Optimization of the cascaded power state and the driver for the HF DC-DC converter
- Improved modelling of the HF DC-DC converter based on cascoded power stage on detailed switching losses and dead-time optimization

- Documentation for the block level optimization of **D2.3 "Analysis and optimisation of selected architectures"**
- Documentation for the optimization of the first prototype chips **D2.4 "Architecture optimisation of 1st prototype chips"**
- Documentation for the optimization with improved models **D2.5 "Analysis and optimization with improved models"**

## WP3 – Technology Development

### Work Package Objectives and Significant Results

WP3 has met all the objectives set at end of Year 1 review. Significant results from WP3 are listed below.

1) Inductor fabrication for Demo1 & ITVs
   - Tyndall has fabricated inductors for Demo 1, ITVs and reliability testing of inductors
   - Tyndall has completed initial characterization of inductors for Demo1, ITVs and die-level reliability testing for Demo1 & ITV2
   - Tyndall has provided 100 dies to Infineon for packaging and reliability testing
2) Technology transfer and scale up (Tyndall to IFX)
   - Tyndall has worked with IFX in setting up a magnetics processing line in Regensburg, Germany based on Tyndall's processing of racetrack structures
   - IFX has developed an optimized process for realising an air-core design on a 200 mm wafer
   - Magnetics processing is being investigated in a backend plating tool
3) Capacitor fabrication & interposer development
   - To meet HV stage requirements
   - Develop and demonstrate high voltage (BV=30V) process for HV stage
   - Execute preliminary reliability study and extrapolate lifetime under BOSH specified usage conditions
   - To implement technologies for demonstrators
   - Generate layout for LV/HV/HF interposers (2 mask sets)
   - Process PICS wafers – actual : TSV finalization ongoing (4 lots)
   - Develop and execute electrical testing Esort (3Dexcluded) and HF characterisation

### Work Progress (Detailed description of all tasks)

#### 1) Task 3.3a - Inductor fabrication for Demo1 & ITVs

Tyndall completed fabrication of Single Layer Metal (SLM) inductor designs for Demo1, ITV2a and for inductor reliability testing programme. The Double Layer Metal (DLM) devices are scheduled to be completed by end of November 2014. Figure 3.1 below, shows image of a full fabricated 4" SLM wafer for Demo1 devices. Further, small signal characterization of the Demo1 devices were completed at Tyndall and around 100 samples were sent to IFX for package level reliability testing of the inductors.

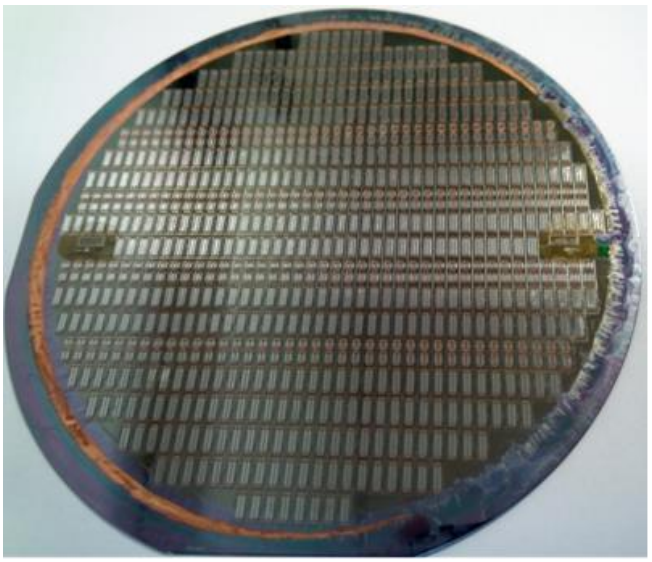


*Figure 3.1. Fully fabricated SLM devices wafer for Demo1*

Additionally, Tyndall has worked on developing a lamination process using sputter deposition of NiFe (permalloy) core. Figure 3.2 below shows the cross-section of a laminated NiFe core. The initial characterization of the laminated core shows that this structure has a higher operational frequency (6 lamination of 100 nm thick-500 MHz) compared to a single lamination core (100 MHz) due to reduced eddy currents.

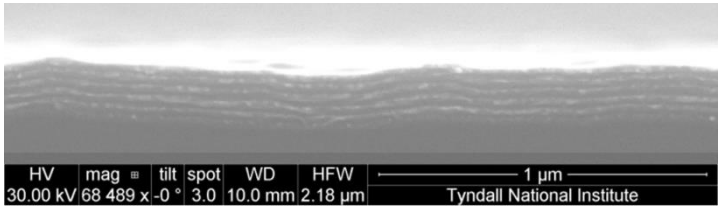



*Figure 3.2. Cross-section of a laminated core structure*

**2) <u>Task 3.2 - Magnetics processing technology transfer from Tyndall-IFX</u>**

IFX and Tyndall work together in establishing a magnetics processing line in Regensburg. In terms of transfer of technology, IFX were successful in replicating all the major process steps in realising a racetrack inductor structure. IFX successfully fabricated an air-core structure based on Demo 1 designs on an 8” wafer with copper winding thickness of around 18 µm (standard-10 µm). Figure 3.3 shows a fully fabricated air-core SLM wafer at IFX, along with a magnified image of a Demo1 device.

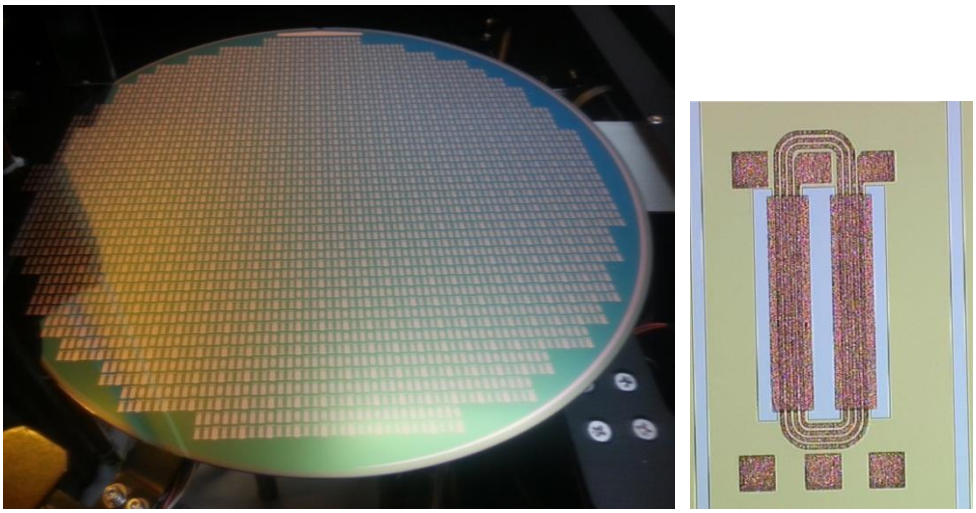


*Figure 3. Fully fabricated air-core inductor with Demo1 device*

IFX investigated different approaches to depositing magnetic thin films including sputtering and electrodeposition. Electrodeposition was the more attractive solution in terms of the processing speed and cost. The initial plan was to implement the magnetics plating in the front end tool, however, on further discussions with the bath vendor, issue of contamination in the front end tool were identified, which would impact the other processing on this tool. Hence, IFX decided to establish the magnetic plating line as a back end tool and are currently in discussions with tool vendors in installing this processing line.

### 3) Task 3.3b - Capacitor fabrication & Interposer development

IPDiA started the fabrication of trench capacitor for Low Voltage (LV) Demo1, ITVs and High Voltage (HV) Demo1 in July 2014. Presently, the wafers are getting the TSVs metallized and will be ready for further packaging by end of Q4 2014 (M27). It is envisaged that the required quantities of ‘System In Package’ prototypes will be achieved by the main process run and would not require a back-up run. The capacitors for this project are based on IPDiA’s Silicon deep trench technology with tripod structure to multiply surface ratio & their electrical performance is in agreement with the design targets. Figure 3.4 shows the layout of LV Demo1 and ITVs being fabricated at IPDiA.

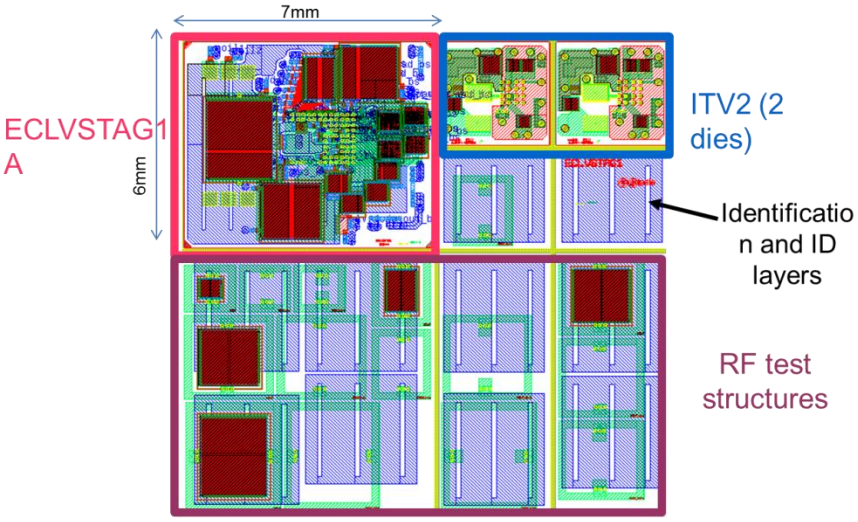



*Figure 3.4. Layout for LV Demo1 & ITV2 devices*

### Objectives for Year 3

1) **Task 3.3a - Inductor development**
   - Tyndall will further optimize the lamination process for improving performance of inductors
   - Tyndall will work with IFX & Bosch in completing the detailed reliability programme for inductors
   - Tyndall will work with IFX, IFAT, IPDiA, Bosch in developing Power Supply in Package, test and analysis of the assembled Demo1 device
   - Tyndall will work with INSA, Lyon & IPDiA in assembly and testing of ITVs
2) **Task 3.2 - Tyndall-IFX technology transfer**
   - IFX will establish a proof of concept back end processing tool for magnetic material deposition
   - IFX will demonstrate a fully fabricated Demo1 device in an 8" wafer with closed magnetic core
3) **Task 3.3b - Capacitor & Interposer development**
   - IPDiA will work with IFX in completing the PwrSiP modules
   - IPDiA will work with IFX, IFAT, Tyndall & Bosch in testing & analysis of Demo1 device
   - IPDiA will work with INSA, Lyon & Tyndall in assembly and evaluation of ITV2 devices

## WP4 – System Integration

### Progress towards objectives

Task 4.1.1 System-in-Package Technology (embedded solution) – Demo1A
Developing a power supply in package (PSiP) solution containing a functional interposer including Through Substrate Vias (TSV), passive devices (Inductor & Capacitor) and the respective logic IC. By adapting eWLB technology in order to scope with the requirements of advanced CMOS technology (e.g. ultra low k, Thermal mismatch, etc.) in terms of stress and strain adjustment an optimum Frontend/Backend interface will be achieved. The SiP technology is aimed to be scalable to sub 28 nm technologies.

Task 4.1.2 System-in-Package Technology (flipped solution) – ITV2
Developing a power supply solution containing LC substrate including passive devices (Inductor & Capacitor) and the respective logic IC based on an intermediate test vehicle). This test vehicle is used to show the principal system feasibility by early functional and reliability characterisation. For the demonstrator the PMIC will be microbumbed onto this functional fan out substrate. With monolithic integrated inductors and capacities.

Task 4.2: Characterisation and reliability analysis of individual components and Demo1A
Board level characterisation according to defined electrical and reliability requirements to evaluate the manufacturability, functionality and reliability is performed on the individual components (inductors, trench capacitors and interposer) and the whole demonstrator system.

Development of an adequate application test board and verify the performance in the test board in real automotive environment. Result will be an assessment whether this will fit into automotive environment.

### Significant results

- Integration process for ITV2 (flip-chip) and Demo1A (eWLB) prepared, validated and ready to start once components are ready (early December 2014).
- Validation Matrix (VM) ready for individual components (Inductors, Trench capacitors, Interposer), integration (eWLB) and full demonstrator.
- Development of an adequate application test board ongoing. As the switching frequency in Demo1A is 10MHz (compared to 1MHz in SotA), conducted and capacitive emissions and immunity test are mandatory for the assessment in automotive environment.

## WP5 - Dissemination

Web site and LinkedIn Group

The Web site (http://www.powerswipe.eu) was kept active during the course of the year. All public deliverables are uploaded to the Downloads page. Furthermore, a list of all publications and presentations is kept in the Results page, including Digital Object Identifier links to allow access to those with subscriptions.

The LinkedIn Power Supply on Chip (PwrSoC) has continued growing and now has almost 80 active members.

Tutorial

On March, as part of the APEC (Applied Power Electronics Conference and Exposition) in Fort Worth, the PowerSwipe consortium presented a Professional Development Seminar on Power Supply on Chip, which was well attended with 110 attendees.


*Figure 5.1. Announcement and lecture by Prof. Cobos during APEC’14*

Papers and presentations

PowerSwipe has been very active disseminating the results of the project during this year. We have published 6 papers in refereed journals, and 14 presentations have appeared in conference proceedings. The following is the list of titles:

Papers

- Trans on IEEE Trans Power Electronics
  - "Accurate analysis of sub-harmonic oscillations of V2 and V2Ic controls applied to Buck converter" – DOI: 10.1109/TPEL.2014.2308015
  - "Improved transient response of controllers by synchronizing the modulator with the load step: Application to V2Ic" – DOI: 10.1109/TPEL.2014.2314242
  - "Multiphase Current Controlled Buck Converter with Energy Recycling Output Impedance Correction Circuit (OICC)" – DOI: 10.1109/TPEL.2014.2362011
  - "v1 concept: designing a voltage mode control as current mode with near time-optimal response for Buck-type converters"
- EPE Journal: "Improved transient response of V2Ic control: clock pulse synchronization based on the current through the output capacitor"
- IEEE Trans on Magnetics: "Advances in Planar Coil Processing for Improved Micro-Inductor Performance"

Conference Proceedings

- PwrSoC 2014 (Boston, 6-8 October)
  - Presentations: IFAT, IPDiA, CEI-UPM, Lab Ampere
  - E-posters: IFAT, Tyndall, Lab Ampere
- ECCE'14 (Pittsburgh, 14-18 September)
  - CEI-UPM: "Optimization and Analysis of PwrSoC Buck Converter with integrated passives for Automotive Application" *(Best Poster Award)*
- EPE'14-ECCE Europe (Lappeenranta, 26-28 August)
  - CEI-UPM: "Analysis on the Effect of Modulation Delays on the Size of the Output Capacitor"
- COMPEL 2014 (Santander, 22-25 June)
  - CEI-UPM/IFAT: "Energy based switches losses model for the optimization of PwrSoC buck converter"
  - CEI-UPM "An optimization algorithm to design fast and robust analog controls for buck converters"
- Infineon AMP-S Design Symposium (Graz, 13-14 May)
  - IFAT: "Power SoC with Integrated Passives: PowerSWIPE"
- InterMAG 2014 (Dresden, 4-8 May)
  - Tyndall: "Copper coil deposition process and effects of winding gaps on micro-inductor performance"
- APEC'14 (Fort Worth, 16-20 March)
  - CEI-UPM *(Best Poster Award)*
- CIPS'14 (Nuremberg, 25-27 February)
  - PowerSwipe overview *(Plenary session)*
  - Lab Ampere
  - CEI-UPM *(Best Poster Award)*

**WP5 - Exploitation**

All partners have started looking at potential exploitation routes for the knowledge and technologies that are being developed through PowerSwipe. The following figure shows the PUDF spreadsheet, with the list of potential project outcomes identified so far.

| Description | Type | Sector | IPR Exploitation | Lead Partner |
|---|---|---|---|---|
| Process for fabrication of racetrack inductor | Commercial | Power Electronics | Own/Licence | Tyndall |
| Multi DC-DC converter PMIC with Passives | Adv. Knowledge Commercial | Power Electronics, Automotive, General | Own/Licence | IFAT |
| Integrated Magnetic Design Tool | Commercial | CAD | Licence | UPM |
| Component embedding Si trench based capacitors | Commercial | Power Electronics | Own/Licence | IPDiA |
| SiP for multi DC-DC Converter PMIC with Passives | Adv. Knowledge Commercial | Power Electronics, Automotive, General | Own/Licence | IFX |
| Microcontroller with embedded voltage controller | Commercial | Power Electronics, Automotive | Own | Bosch |

*Figure 5.2. List of identified project outcomes from PUDF*

Based on this list, the PowerSwipe consortium has produced a Draft Exploitation Plan 9Deliverable D5.3).

### 3.2.3 Project management during the period

Management tasks included the organising of consortium meetings, internal reporting on work progress (monthly) and submission of deliverables.

Project meetings were organised on a regular basis, as well as WP specific meetings and discussions:

- Executive Steering Committee meetings were carried out on the first Tuesday of every month via teleconference with the support of multimedia sharing facilities (WebEx)
- Consortium meetings every six months:
  - 3rd Six-monthly meeting: Lyon, 28-29 April 2014
  - 4th Six-monthly meeting: Villach, 20-21 October 2014
- WP-specific meetings were organised when required:
  - WP4: Reliability meeting at Bosch (Reutlingen/Stuttgart) attended by IPDiA, Tyndall and IFX on July 7-8 July 2014.
  - WP2: Modelling meeting at UPM (Madrid) attended by Lab Ampere on 11 October 2014.

The project consortium keeps a Document Repository where all common documents and internal reports are shared.

All required legal, administrative and financial documents and procedures were taken care of. The Consortium Agreement was negotiated and the final agreed document signed in October 2013.

## Problems which have occurred and how they were solved or envisaged solutions

The inductor technology transfer from Tyndall to IFX (Task 3.2) has resulted more problematic and time consuming that originally planned. IFX were planning to introduce magnetics processing in their front end plating tool. On discussions with magnetics plating line manufacturers, introducing this bath in the tool would have increase contamination risk. This would impact their commercial business; hence the IFX team decided to move the magnetics plating as a backend process and required IFX to purchase new tools.

Therefore IFX were not in a position to fabricate the inductors for the ITVs and Demonstrators on time as planned. This would have meant delays in fabrication of Demo1 and impacted all the major milestones. The consortium agreed to do the fabrication of the inductors at Tyndall and IFX has employed their effort (originally allocated to fabrication) to complete the technology transfer.

Thanks to this solution the inductors have been delivered on time and the technology transfer is nearly finished.

## Changes in consortium

No changes

## Impact of possible deviations from the planned milestones and deliverables

**Tape-out delay and Updated plan**
According to the PowerSwipe DoW, WP1 includes the fabrication of power management ICs (PMIC) for the project Demonstrators and Intermediate Test Vehicles (ITV). These PMIC's are fabricated by Infineon Austria (Partner 3) on a C40fla (CMOS 40nm, flash memory, automotive qualification) shuttle run as part of a multi-project wafer (MPW). A low voltage (LV) PMIC will be used in Demo1 and a high frequency (HF) in ITV2. In the original DoW, the first C40fla tape-out was planned to take place on December 2013 (Month 15). A C40fla run is carried out at Infineon approximately every 12 months. Due to commercial considerations, the run in December 2013 was re-scheduled to June 2014 (Month 21).

**Impact of keeping original workplan (as described in DoW)**
If the consortium continued as planned (doing nothing and waiting for the re-scheduled tape-out), the whole project would have been delayed by 6 months.

**Proposed solution**
During the 1st Annual Review, it was proposed that **Demonstrator 1**, which was planned to be based on a second tape-out PMIC (M27, Dec 2014) would use the low-voltage PMIC from the first tape-out (M21, Jun 2014) instead. To minimise the risks of an unsuccessful first design, the extra 6 months (from M15 to M21) were used to improve and validate the IC design. Furthermore, extra functionality, and modules which would have not been available in M15, are now included. Therefore Demo 1 is been built 6 months ahead of schedule, giving more time for automotive-grade characterisation, reliability and testing during Year 3.

**ITV2**, which uses the high-frequency PMIC, was delayed by 6 months. This extra time has been used to improve the design and to incorporate new technology concepts. As a consequence, **Demonstrator 2** will have a 5 month delay. However, because Demo2 is not reliant on the C40fla technology and does not require automotive certification, it will be fabricated and characterised within Year 3 of the project.

**Impact of revised workplan**
The work on the different workpackages will continue as planned, with only minor adjustments on the due date of deliverables and milestones:

| **Delayed deliverables** | DoW due date | New due date |
|---|---|---|
| D1.3 – First prototype chips | M18 | M26 |
| D4.2 – Demonstrator 2 | M30 | M35 |

| **Delayed milestones** | DoW due date | New due date |
|---|---|---|
| Ms1.3 – Tape-out 1st prototype chips | M15 | M21 |
| Ms1.4 – System architecture analysis | M24 | M30 |
| Ms4.1 – Intermediate test vehicles | M24 | M30 |

The resources allocated to each partner and WP will remain the same (no reduction or increase).

This updated workplan was accepted by both External Experts (R. Groppo and H.J. Thanner) and the Project Officer (A. Galetsas).

**Year 1 Review Recommendations and Actions**

| | |
|---|---|
| Update State of the Art | Done – Continue during the course of the project |
| Harmonise deliverables | New template, including recommended lengths has been agreed upon by the consortium |
| Finalise CA | CA agreed and signed in November 2013 |
| Provide use of resources before 2nd Review | Included in this document which will be submitted in advance of 2nd Review on 4th December 2014 |
| Prepare Draft Exploitation plan before 2nd Review | Draft Exploitation Plan will be presented during 2nd Review |

## Effort per WP

| *Workpackage*[5] | WP1 | | WP2 | | WP3 | | WP4 | | WP5 | | WP6 | | TOTAL per Beneficiary | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Actual PM total | Planned PM total | Actual PM total | Planned PM total | Actual PM total | Planned PM total | Actual PM total | Planned PM total | Actual PM total | Planned PM total | Actual PM total | Planned PM total | Actual Total | Planned total |
| Tyndall-UCC | 0.3 | 0.3 | 13 | 8 | 46.6 | 16.7 | 8 | 8 | 3.5 | 2.7 | 5.3 | 2.3 | **76.7** | 38 |
| IFX | | | | | 11.18 | 11.7 | 5.5 | 11.3 | | 1 | 0.27 | 1 | **16.95** | 25 |
| IFAT | 36.9 | 21.7 | | | | | 2.1 | 2.7 | 0.7 | | 2 | 1 | **41.7** | 25.4 |
| IPDIA | 1.5 | 1 | | | 7.09 | 7 | 4.71 | 4.5 | 0.26 | | 0.32 | 0.1 | **13.88** | 12.6 |
| UPM | 11 | 8 | 13 | 12 | | | | | 0.67 | 0.67 | 0.33 | 0.25 | **25** | 20.92 |
| BOSCH | 0.19 | 1.67 | 0.07 | 1.5 | 0.05 | 0.5 | 1.77 | 8 | | | 0.28 | | **2.36** | 11.67 |
| UCBL | 10.51 | 6.4 | 2.27 | 6 | 1.18 | 4.2 | 0.23 | 10.3 | 1.67 | 0.3 | | | **15.86** | 27.2 |
| **TOTAL** | **60.4** | 39.07 | **28.34** | 27.5 | **66.1** | 40.1 | **22.31** | 44.8 | **6.80** | 4.67 | **8.50** | 4.65 | **192.45** | **160.79** |

[5] Please indicate in the table the number of person months over the whole duration for the planned work, for each workpackage by each beneficiary

## 3.3 Deliverables and milestones tables

**Deliverables**

| TABLE 1. DELIVERABLES | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Del. no.** | **Deliverable name** | **Version** | **WP no.** | **Lead beneficiary** | **Nature** | **Dissem. level[6]** | **Delivery date from Annex I** | **Actual / Forecast delivery date** | **Status No submitted/ Submitted** | **Comments** |
| D1.3 | Design report of 1st prototype chips | 1.3 | 1 | IFAT | R | CO | M18 | M22 | Submitted | |
| D2.3 | Analysis and optimisation of selected architectures | Final | 2 | UPM | R | PU | M18 | M19 | Submitted | |
| D3.2 | Passive components fabricated | Final | 3 | Tyndall | R | PU | M18 | M24 | Submitted | |
| D5.2.1 | Mid-term dissemination report | 1.2 | 5 | Tyndall | R | PU | M18 | M19 | Submitted | |
| D1.4 | Optimised system architecture description | | 1 | IFAT | R | CO | M24 | M32 | No sub. | (New plan) |
| D1.5 | Optimised block-level specification | | 1 | IFAT | R | CO | M24 | M32 | No sub. | (New plan) |
| D2.4 | Architecture optimisation of 1st prototype chips | Final | 2 | UPM | R | PU | M24 | M25 | Submitted | |
| D2.5 | Analysis and optimisation with improved models | Final | 2 | UPM | R | PU | M24 | M25 | Submitted | |
| D3.3 | Report on inductor technology transfer | | 3 | Tyndall | R | PU | M24 | M28 | No sub. | (Delayed) |
| D6.1.2 | 2nd annual management report | | 6 | Tyndall | R | PU | M24 | M25 | Submitted | This doc. |

[6] **PU** = Public. **PP** = Restricted to other programme participants (including the Commission Services). **RE** = Restricted to a group specified by the consortium (including the Commission Services). **CO** = Confidential, only for members of the consortium (including the Commission Services).
**Make sure that you are using the correct following label when your project has classified deliverables.**
**EU restricted** = Classified with the mention of the classification level restricted "EU Restricted". **EU confidential** = Classified with the mention of the classification level confidential " EU Confidential ". **EU secret** = Classified with the mention of the classification level secret "EU Secret "

**Milestones**

| TABLE 2. MILESTONES | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Milestone no.** | **Milestone name** | **Work package no** | **Lead beneficiary** | **Delivery date from Annex I dd/mm/yyyy** | **Achieved Yes/No** | **Actual / Forecast achievement date dd/mm/yyyy** | **Comments** |
| **Ms1.3** | Tape-out 1st prototype chips | **1** | **IFAT** | **31/12/2013** | **YES** | **30/06/2014** | New plan |
| **Ms2.3** | Detailed analysis and optimisation of selected architectures | **2** | **UPM** | **31/03/2014** | **YES** | **31/03/2014** | |
| **Ms3.1** | Passive components ready | **3** | **Tyndall** | **31/03/2014** | **YES** | **31/08/2014** | |
| **Ms1.4** | System architecture analysis completed | **1** | **IFAT** | **30/09/2014** | **NO** | **31/03/2015** | New plan |
| **Ms3.2** | Inductor process transfer completed | **3** | **Tyndall** | **30/09/2014** | **NO** | **31/01/2015** | Delay |
| **Ms4.1** | Intermediate test vehicle | **4** | **IFX** | **30/09/2014** | **NO** | **31/03/2015** | New plan |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |