Deliverable D5.2
‘’DEMO chip processing’’ option 3

Deliverable D5.2 ‘’DEMO chip processing‘’ Option 3 PiezoMAT – 2017-03-22_Delivrable_D5.2	
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Diffusion to:	All consortium

RESTRICTED DISSEMINATION

EXECUTIVE SUMMARY

This document describes the DEMO chip processing concerning the option 3 done at CEA clean-room.
It first reminds the DEMO layout already presented in deliverable D5.1. Then it described preliminary study for process optimization and final process till the DEMO chips delivery to partners.

REVISION HISTORY

Revision	Date	Description	Author
V0	14/03/17	First draft	E.Saoutieff
V1	22/03/17	Final version	E.Saoutieff

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1 Introduction

Deliverable **D5.2** is the second deliverable in **WP5** (*Process developments*).

Technological processes have been globally developed on PoC chips so that only fine tuning of these processes is foreseen at this stage (in relationship with design modification as compared to PoC chips).

In DEMO chips, the emphasis is on the electronic integration and on size of the active region rather than on resolution.
DEMO chips will allow experiments able to address important points such as:

- Integration of electronic
- Origin of the signal and its quantification

The choice to go on the compression configuration (top-bottom contacts) was done in agreement with consortium.

2 DEMO layout

The full clean-room process flows have been validated by CEA experts and are presented in the D5.1.
The final architecture of the chip is given in Figure 1. The choice of the materials are described in the D3.2.

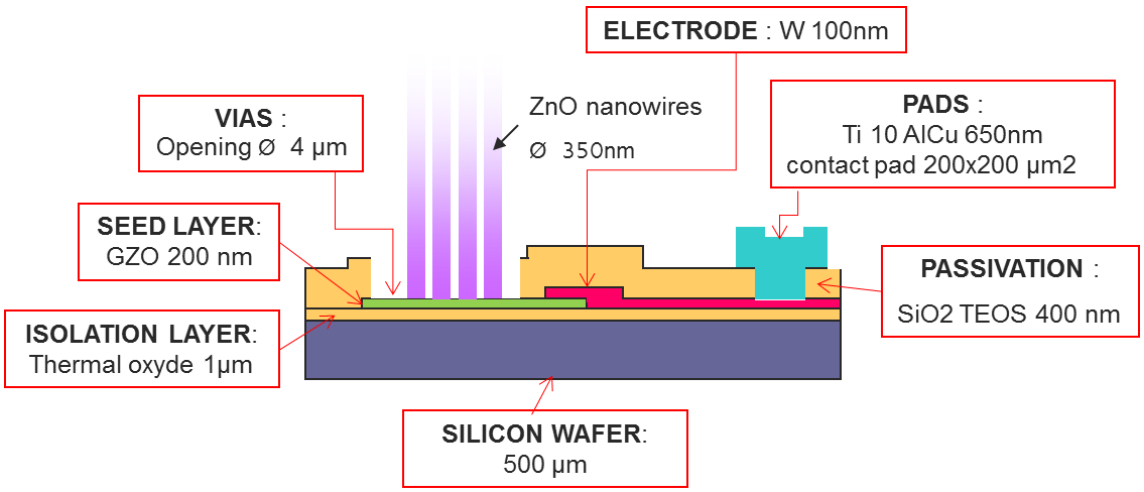


Figure 1: Architecture of the DEMO chip option 3.

A simplified flow is represented below in Figure 2, with 5 technological bricks for a total of around 100 process steps (including step of wafer identification, characterisation by SEM, FIB, optical microscope, thickness measurements, decontamination, electrical test, dicing…)

- Brick I. : deposition and etching of GZO: 16 steps
- Brick II. : deposition and etching of W lines: 18 steps
- Brick III.: deposition of SiO_2 TeOS and etching of SiO_2 on W (pad location): 10 steps
- Brick IV.: deposition and etching of Ti/AlCu pad: 14 steps
- Brick V.: etching of SiO_2 on GZO (future NW’s location): 11 steps

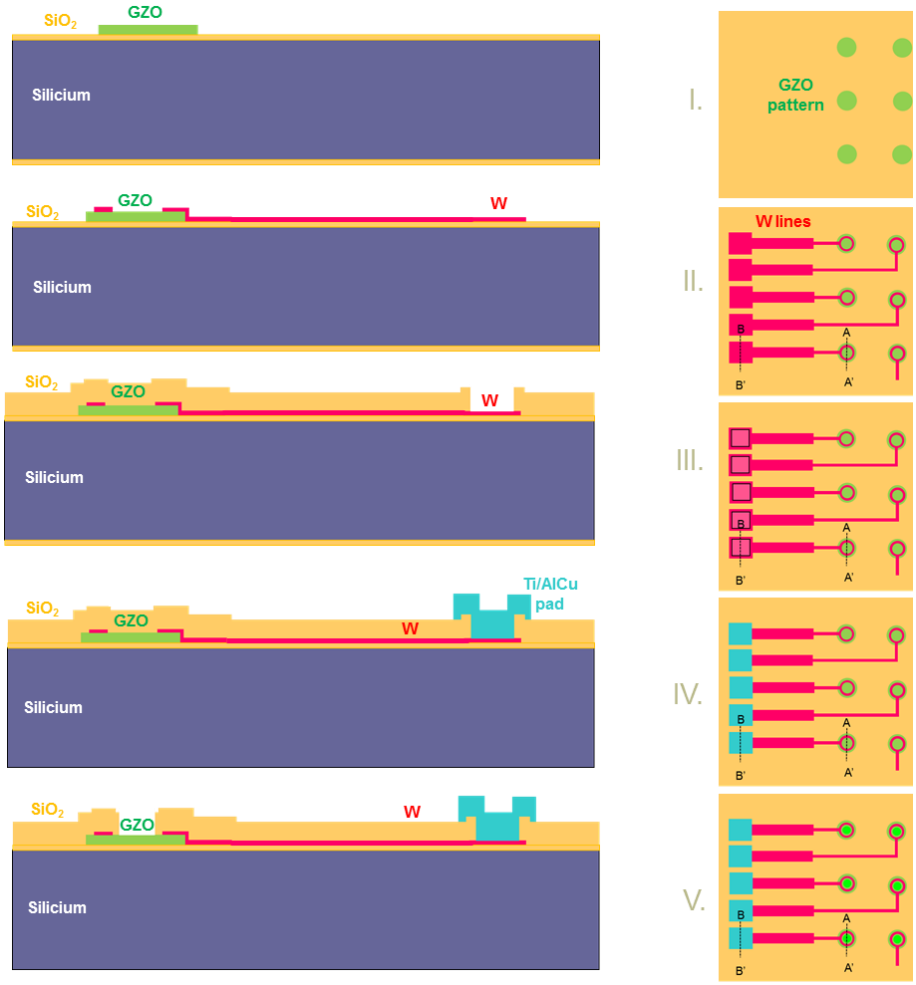


Figure 2: Process flow of DEMO option 3, cross-section view on left and top view on right.

The complete process was done on the main batch presented here in 5 bricks. The production of the chips (8 wafers with 43 chips) started in September 2016 (M35) and finished in February 2017 (M40).

3 Technological brick I: Zinc oxide doped with gallium seed layer pattern definition

During PoC3 processing, some issues appears:

- Corrosion and residues on GZO pattern. In-situ stripping and spray cleaning after etching are done to avoid this.
- No-reproducibility wafer to wafer and inhomogeneity on wafer.

The etching time was thus optimized and the plasma chemical composition was changed.

The challenges for DEMO chips are:

- Define GZO islands with Ø 8µm and with well-defined sloping slides
- Find a suitable process in order to have homogeneity on wafer
- Stabilize process for reproducibility wafer to wafer

For the GZO etching, a matrix of 25 x 10 GZO pattern is shown in Fig. 3. The GZO spots are well defined and spaced. The GZO layer is well etched between each pattern and the diameter of GZO pattern is around 8µm.

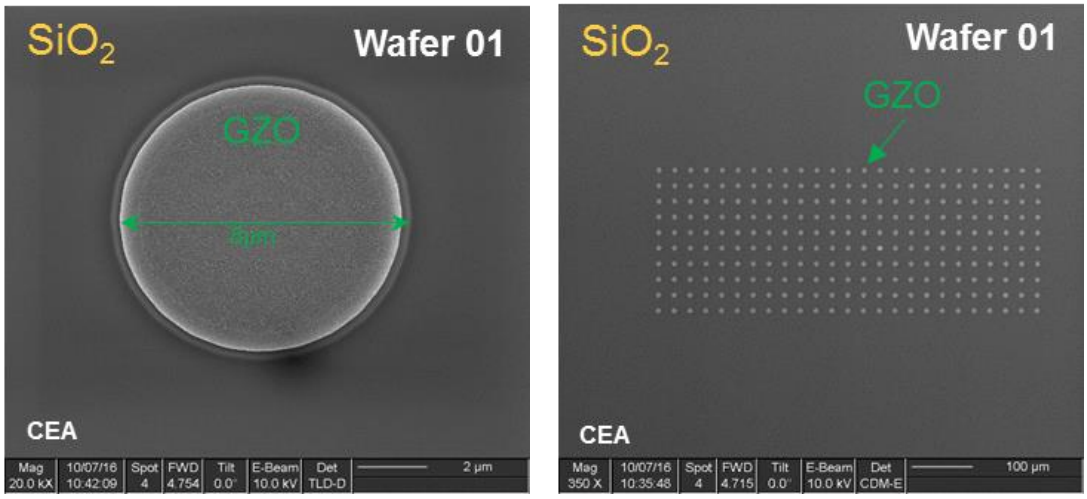


Figure 3: GZO patterns on SiO_2 layer

Like shown on figure 4, the Homogeneity on wafer and reproducibility wafer to wafer was really improve compare to PoC3.

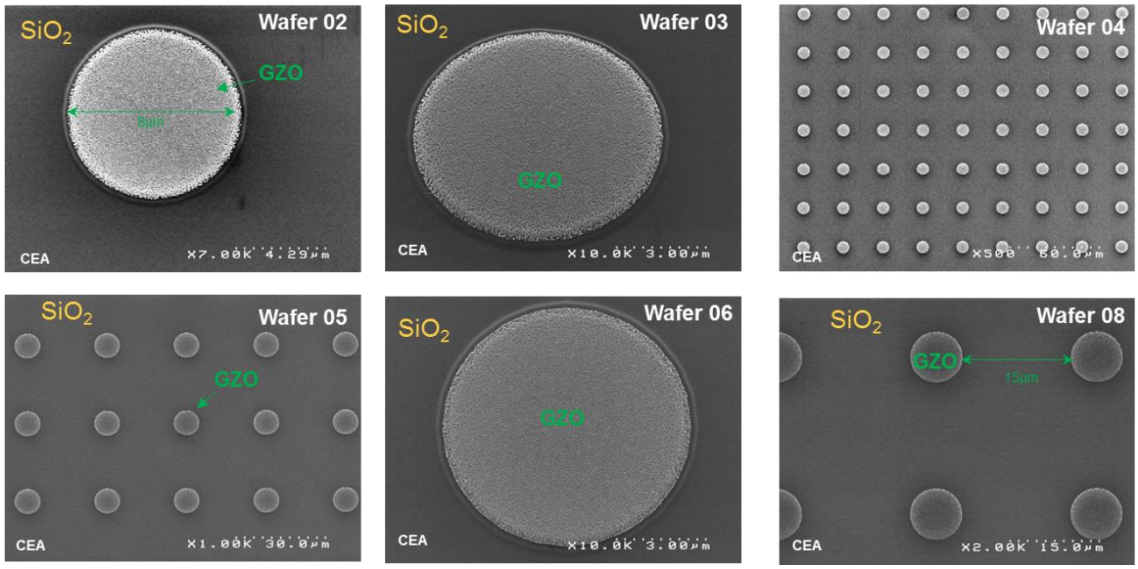


Figure 4: SEM micrographs of GZO patterns deposited on SiO_2 layer on different wafers

On figure 5, we noticed that sloping slides are well defined. This point is important for the conformity of the future “W ring” deposition. A phenomenon of microtrenching is observed in the SiO_2 just at the bottom of the pattern. The thickness of the seed layer is around 193nm.

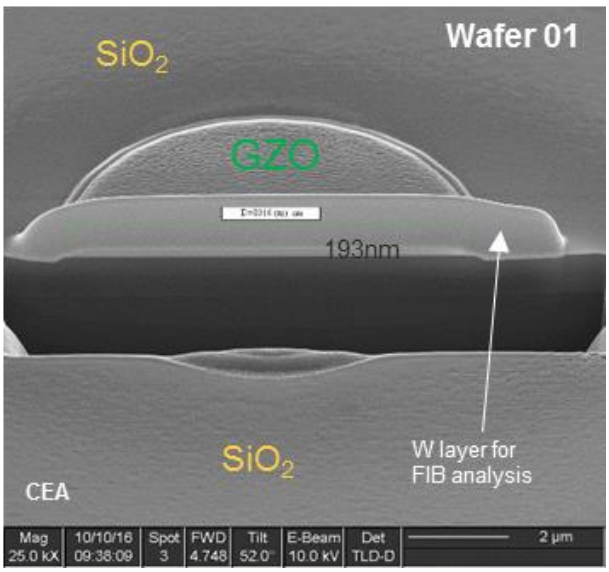


Figure 5: SEM micrograph cross-section on GZO pattern

4 Technological brick II. : Tungsten contact lines definition

4.1 Tungsten deposition and etching

During the etching of tungsten, some issues appeared on PoC3 during process:

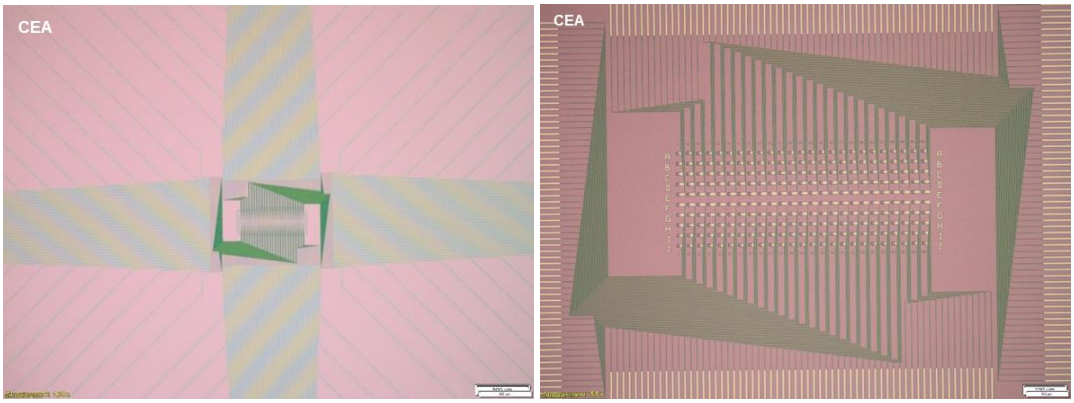
- Corrosion on W lines: to avoid this, stripping in-situ after etching is done and the TeOS is deposited as soon as possible after W etching.
- On final chip, short-cut between pads were found. The increase of distance between 2 W lines will avoid this problem in DEMO chips. Instead of lines 450nm / space 450nm on PoC, the pattern is composed of lines 1µm space 1µm.

Moreover, intermediate electrical tests after this step were completed to check that two consecutive W lines are isolated each other.

For DEMO chips, the challenges are the following:

- Avoid GZO removal during W etching
- Avoid contact between W lines and rings (short-cut)

A 100nm tungsten layer was deposited and etched in W lines and rings. Like shown on fig.6, W lines and rings are well defined. Each GZO pattern is covered by a ring and contacted to one individual pad.



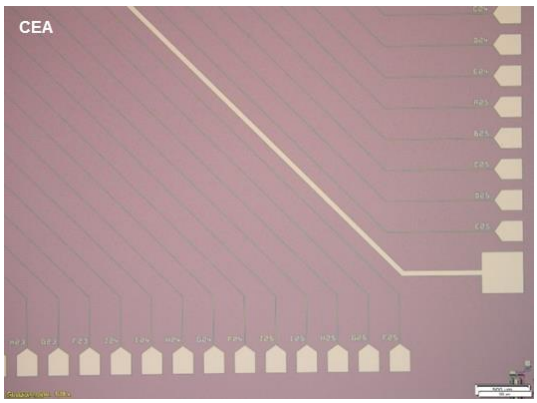


Figure 6: optical photo of W contact lines and rings around GZO pattern

The GZO layer is present under the W rings which will allow contact between future Nanowire and contact pads for piezo measurements. Some corrosion is observed on the GZO pattern, on the periphery (fig.7).

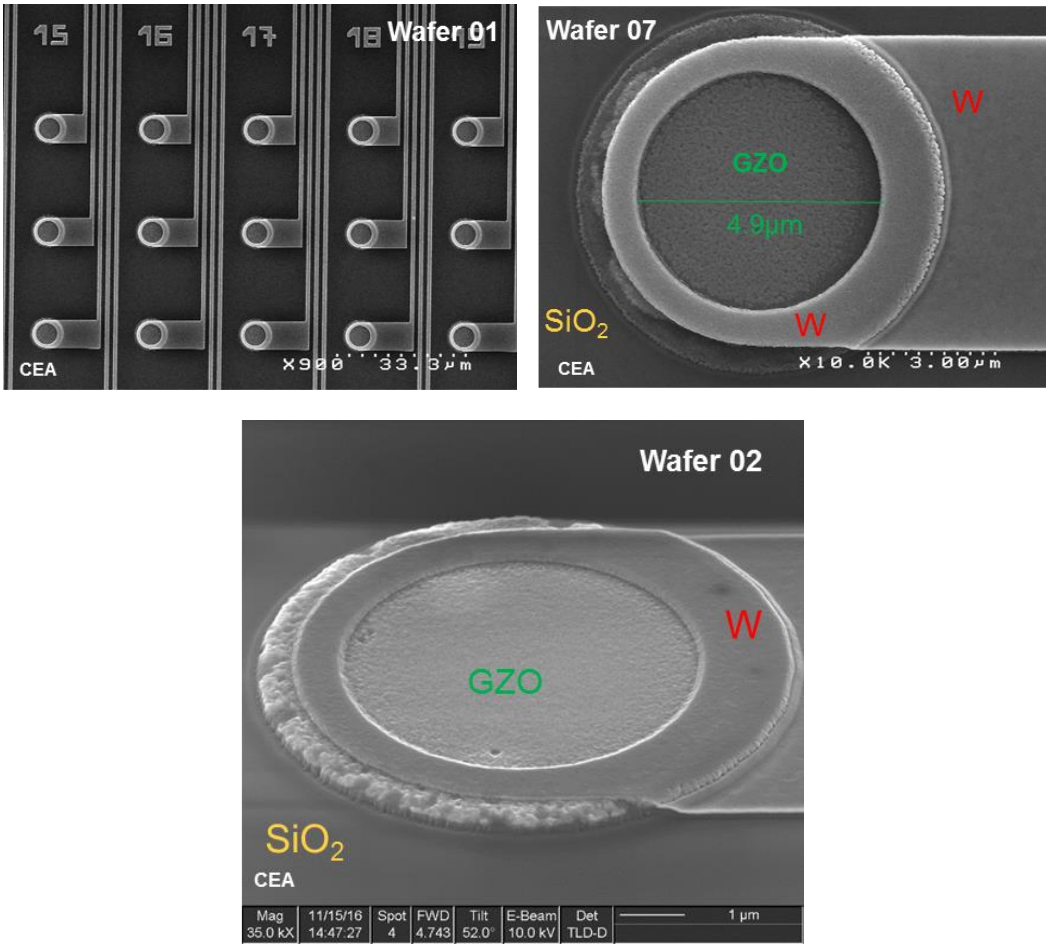


Figure 7: SEM micrographs of W contact lines and rings around GZO pattern

The GZO thickness is around ~180nm after this step. The W layer is conformed to the GZO patterns.

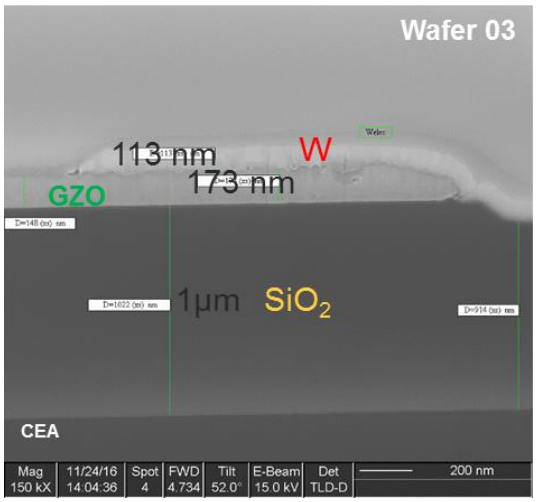


Figure 8: SEM micrograph cross-section on GZO pattern with W ring

4.2 Intermediate electrical tests

Intermediate electrical tests were performed in order to check:

- W pads isolation
- Contact between W and GZO
- Continuity and isolation of W lines

Two different measures were done with voltage measurement at 10µA to 1 mA according to tests devices and current measurement at 1V for pads.
Low current and voltage were applied to avoid breakdown voltage because there is no insulating layer at this stage.

9 chips are tested per wafer, localized like shown on figure 9:

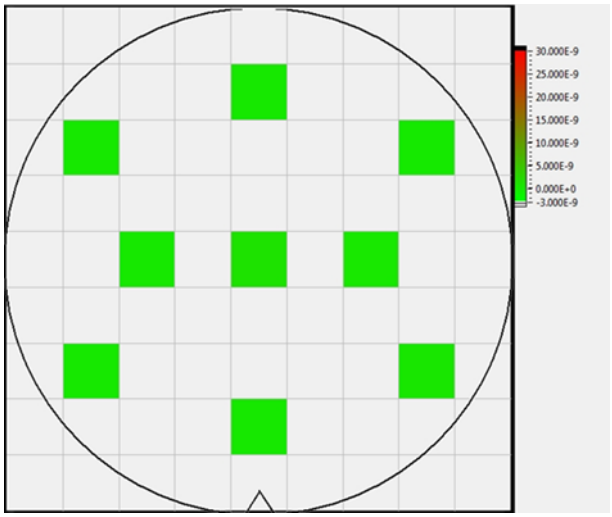


Figure 9: schematic localisation of chips tested on wafer

For each chip, 8 couples of pads are tested, consecutives pads or not referring to consecutive GZO pattern or not.
Figure 10 show each couple of GZO pattern tested; in blue close patterns and in red, distant patterns.

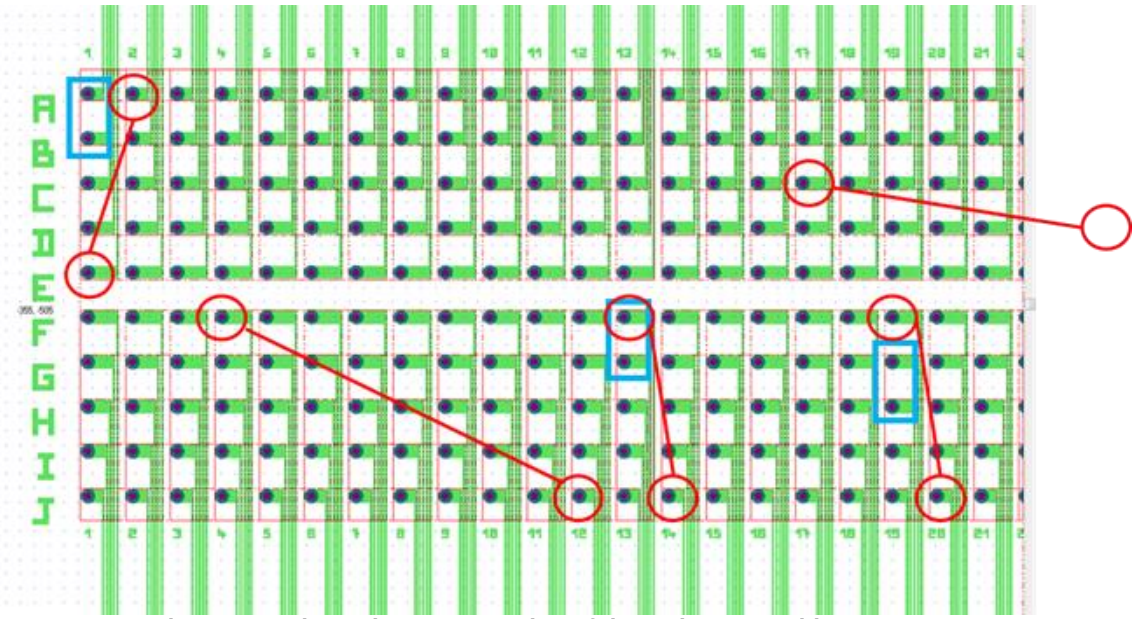


Figure 10: schematic representation of the active zone with GZO pattern

In figure 11, corresponding couple of pads are represented.

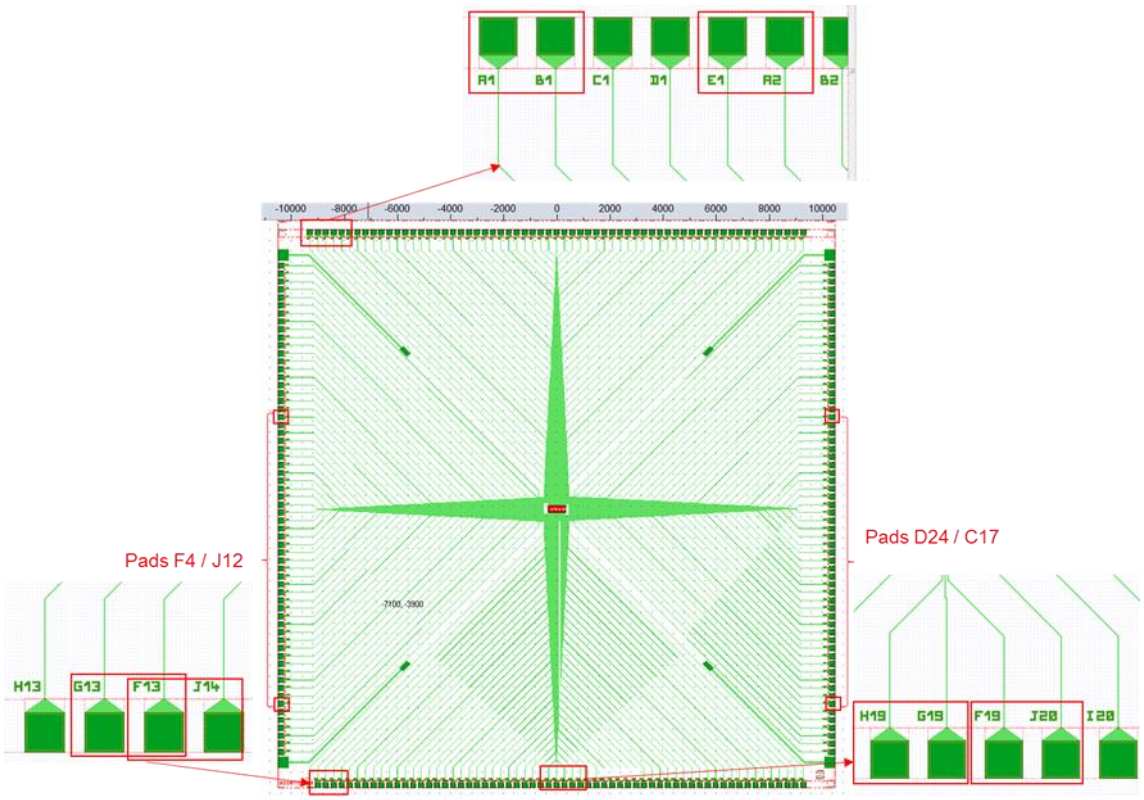


Figure 11: schematic representation of the pads on one chip

Electrical tests showed that there are no short cut between 2 consecutive W pads or distant pads and that all tungsten lines are well isolated from each other.

5 Technological brick III: SiO_2 TeOS deposition and etching of SiO2 on W (pad location)

The deposition and etching of SiO2 TeOS is a classical step at CEA clean-room. No issues appeared during PoC3 process.

After SiO_2 TeOS deposition and etching with W as a stop layer on pad location, the SEM micrographs showed that the opening for the future Ti/AlCu pad are well defined (fig.12 and 13). There are no more TeOS on W.

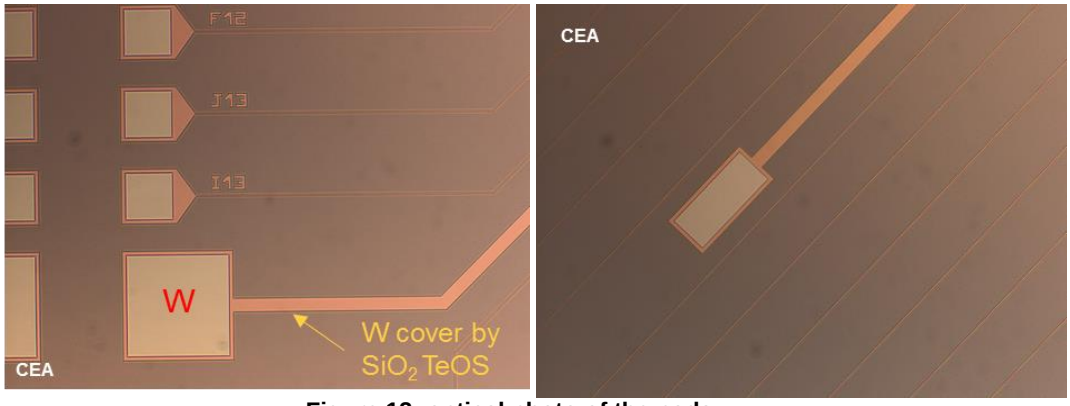


Figure 12: optical photo of the pads

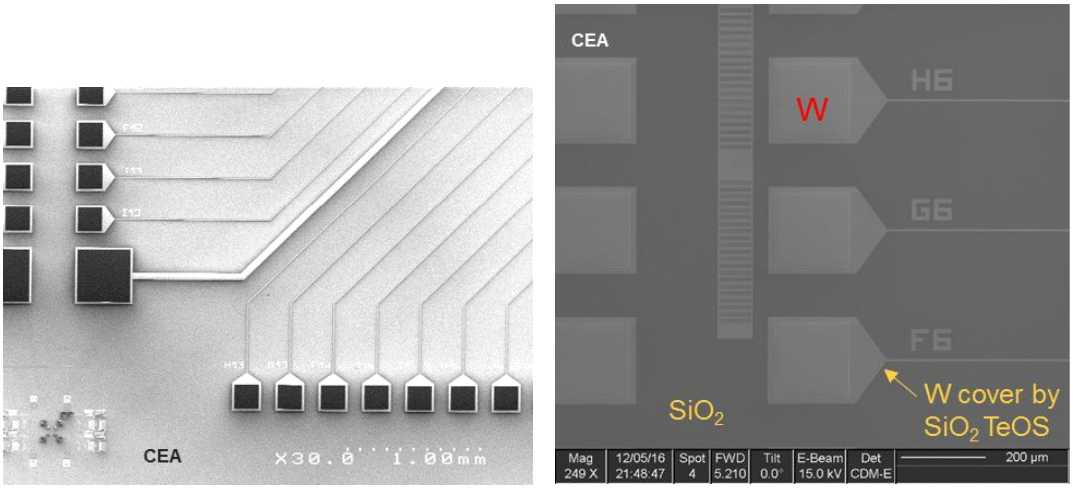


Figure 13: SEM micrograph of the opening of pads

6 Technological brick IV.: Ti/AlCu contact pad definition

To end the 250 contact pads, a full sheet Ti/AlCu layer is deposited and then etched like showed on SEM micrograph figure 14 and 15. This process is standard in CEA clean-room.
At this step, the Ti/AlCu layer deposited on pad is in contact with W lines and so to the future nanowires location site.

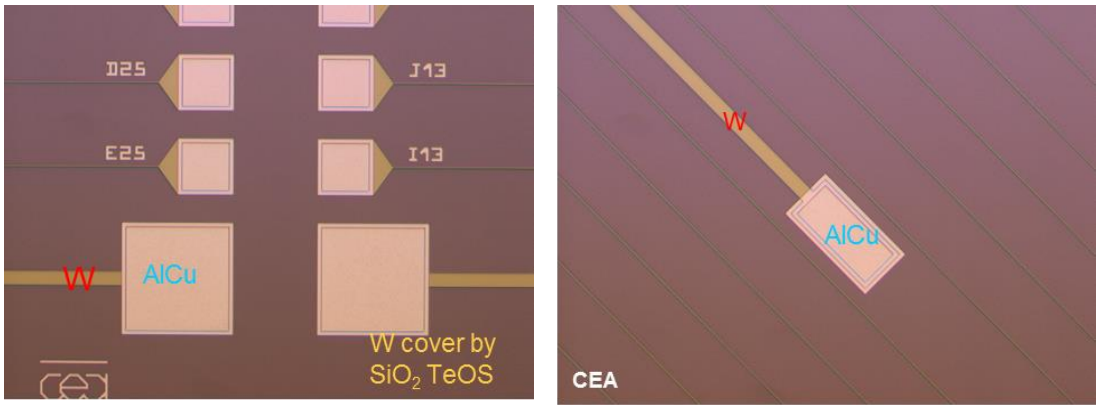


Figure 14: optical photos of the pads

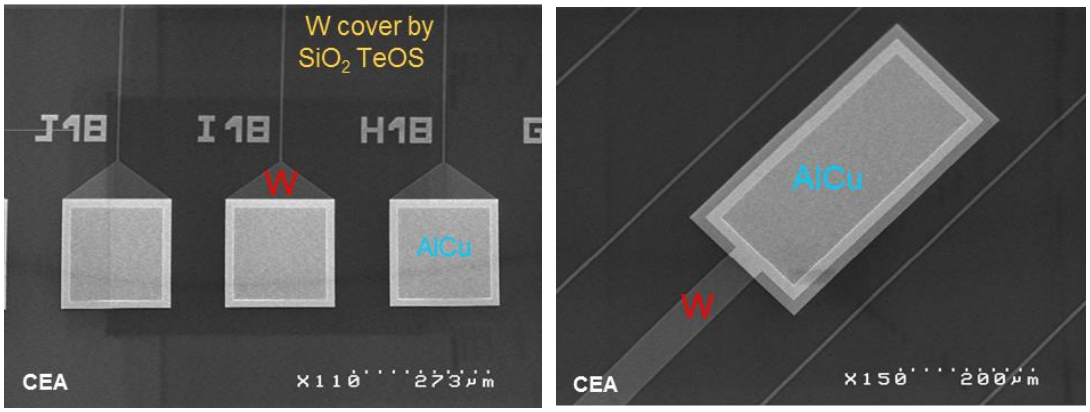


Figure 15: SEM micrographs Ti/AlCu pads

7 Technological brick V.: Opening of SiO_2 on seed layer: future NW’s location

The last step concerns the opening of nanowire location with the etching trough SiO_2 with GZO as a stop layer. This step is critical.

During PoC3 processing, we found some polymer residues on GZO after RIE etching. To avoid this, stripping is done directly after the etching.
We noticed also overetching in GZO, below SiO_2 layer with infiltration. To prevent this, the process parameters were optimized on the rest of wafers.

The challenge for DEMO chip is to avoid GZO removal during etching.

The trial on the first wafer was successful like showed on the micrograph fig.16, with GZO seed layer presence. Opening on seed layer well defined
Remain 170-180nm of GZO

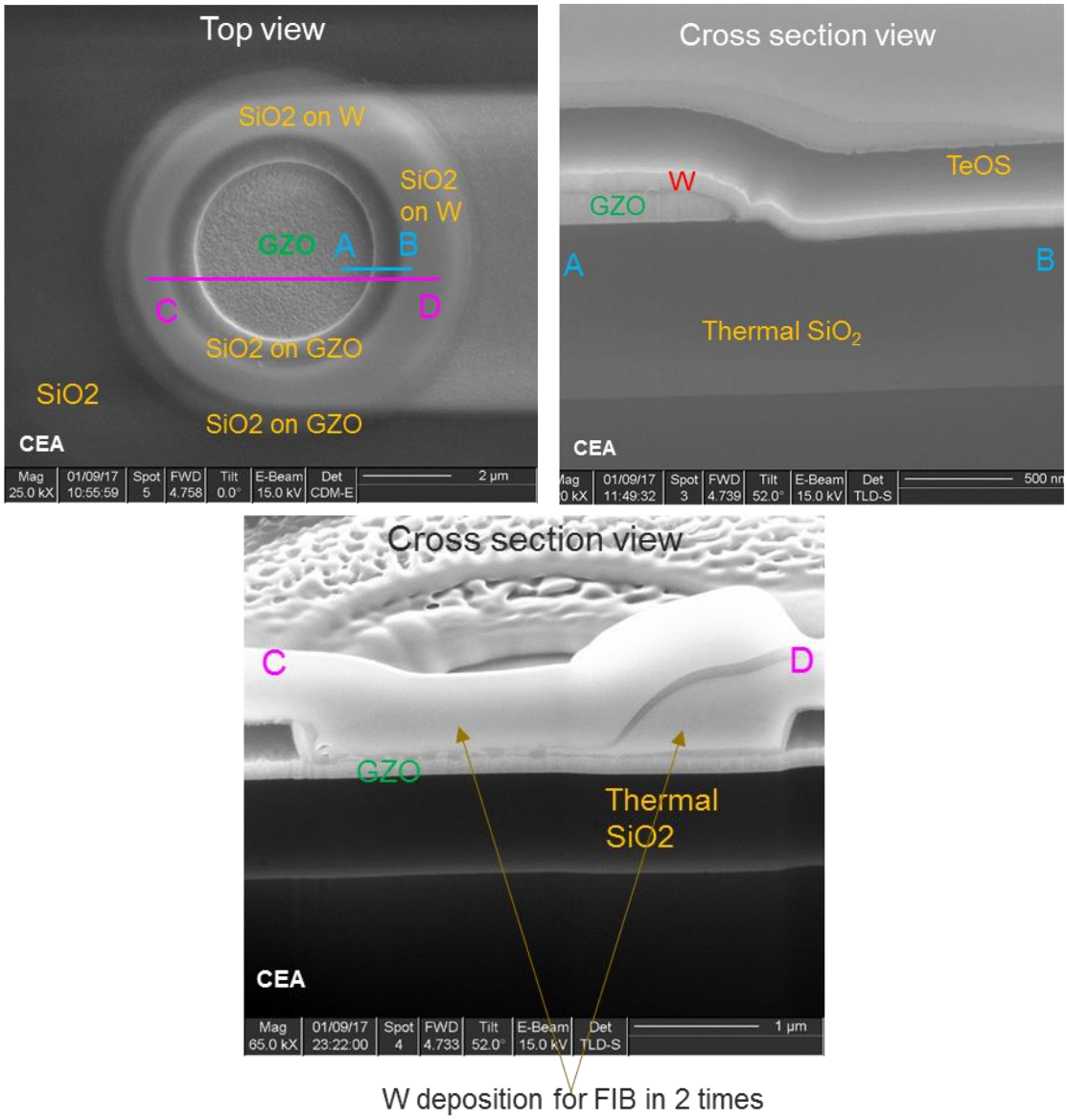


Figure 16: SEM micrograph of the final opening: NW site on P01

The same process was applied on the rest of wafers. However, a problem occurred during the etching of wafers P02 to P08. A non-identified layer remind on GZO like shown on fig.17.

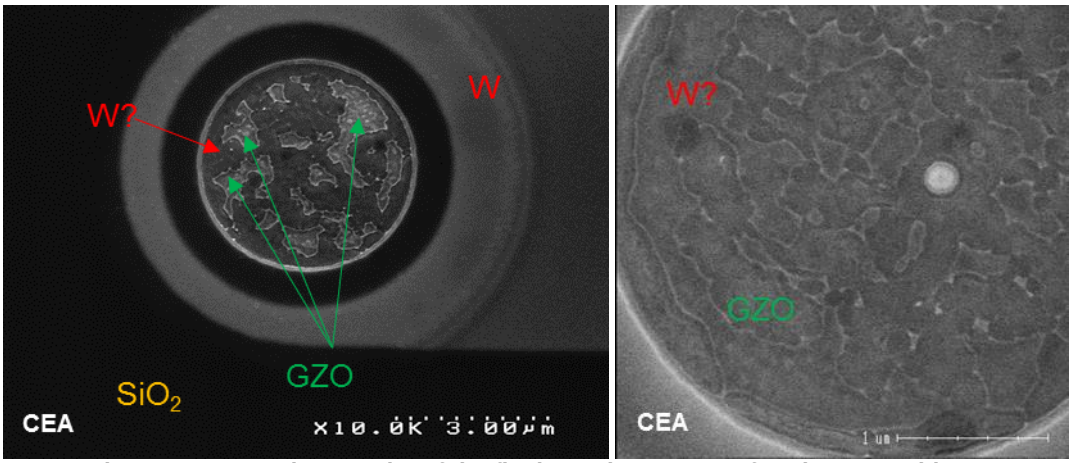


Figure 17: SEM micrographs of the final opening on P07 after the RIE etching

The solution to remove the unwanted layer was to etch by Ion Beam Etching (IBE). This mechanical etching allowed us to remove a thin layer in surface. But the disadvantage is the topography transferred on GZO. This was successful but the GZO quality could be lower.

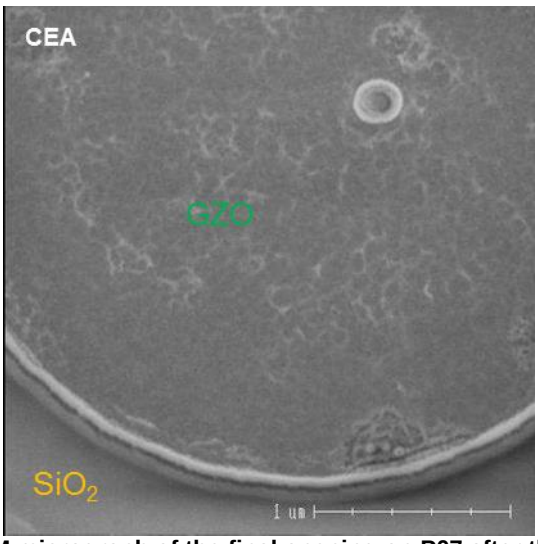


Figure 18: SEM micrograph of the final opening on P07 after the IBE etching

A second etching was thus processed on different wafers. The history of each wafer is summarized in the following table 1:

Figure 1: summary of the 8 processed wafers

Wafer number	Last etching: opening on seed layer		Comments
	1st etching by RIE	2nd etching by IBE	
P01	☺	-	NWs growth and electrical tests OK. Scratch on protective resist
P02	☹	☺	NWs growth and electrical tests OK.
P03	☹	X	No functional, dedicated to preliminary tests for encapsulation and set-up calibration
P04	☹	☺	NWs growth and electrical tests OK.
P05	☹	X	No functional, dedicated to preliminary tests for encapsulation and set-up calibration
P06	☹	☺	NWs growth and electrical tests OK.
P07	☹	☺	NWs growth and electrical tests OK. Scratch on protective resist
P08	☹	☺	NWs growth and electrical tests OK.

8 Grinding and dicing

43 chips were processed on each silicon wafer for a total of around 340 chips like presented on optical photo figure 18. The dimension of the chip is 2,13 x 2,13cm².

We have noticed the presence of scratch on the protective resist after the grinding of the 2 first wafers (P01 and P07). After removal of the resist, we verified that chips were not damaged.
No more scratch appeared on the others wafers due to particular precaution during process.

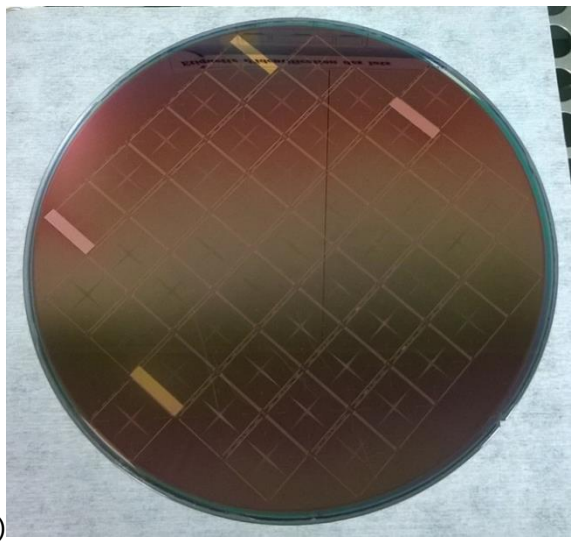
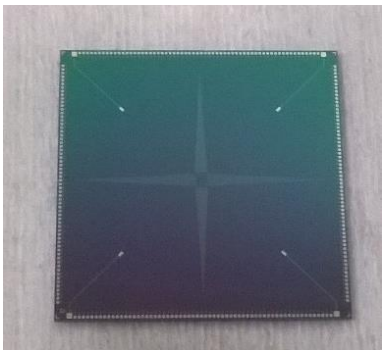
a)  b) 

Figure 18: final DEMO chip wafer (a) and chip (b) after clean-room process

9 Final electrical tests

The same tests as described in section 4.2 were done on each wafer.

These tests allow us to check:
- Pads isolation
- Electrical contact between AlCu/W (pads)
- Electrical contact between W/GZO (site for NWs)
- Continuity and isolation of W lines

All results are summarized in table 2.
Parametrics tests are realized on dedicated test patterns that will be removed at the dicing step.

Figure 2: electrical tests results

D16S1961	PAD Isolation	parametric tests									
		i(V) W/GZO	W pattern: lines 1µm / spaced 1µm		64 devices in serie : short cut ?	W lateral overetch (µm)	R^2 GZO (Ohm)	R^2 W (Ohm)	Rcontact AlCu/W (Ohm)	Rcontact W/GZO big surface (Ohm)	Rcontact W/GZO device (Ohm)
			isolation	resistance (kOhm)							
Number of chips tested by wafer	9	2	43	43	43	43	43	43	43	43	43
P01	100% ok	NA	98% ok	138.24	100% ok	0.14	65	1.68	98.85	NA	537.90
P02	100% ok	100% ok	84% ok	147.05	84% ok	0.21	62	1.63	102.73	421.95	574.34
P03	100% ok	75% ok	98% ok	141.65	100% ok	0.19	61	1.62	98.06	420.28	555.84
P04	100% ok	75% ok	100% ok	150.19	100% ok	0.23	78	1.65	104.64	425.13	636.52
P05	100% ok	100% ok	100% ok	150.77	100% ok	0.22	72	1.66	97.79	430.28	588.69
P06	100% ok	75% ok	100% ok	149.57	100% ok	0.20	72	1.70	105.11	439.00	582.86
P07	100% ok	100% ok	100% ok	148.29	98% ok	0.20	70	1.68	104.25	433.83	594.61
P08	100% ok	75% ok	100% ok	147.73	98% ok	0.19	59	1.69	103.73	434.87	532.48
Mean	100% ok		97.8% ok	146.69	97.5% ok	0.20	67.32	1.67	101.90	429.34	575.40
non uniformity on wafers (%)				3.92		7.76	21.49	3.61	2.59	5.58	24.79
non uniformity on the batch (%)				4.27		20.84	13.94	2.16	3.59	2.18	9.04

The main conclusions are the following:

- All pads are well isolated, there are no short cut between 2 consecutive W pads or distant pads.
- Current-voltage curves W/GZO are linear.
- The W lines grid are isolated. Each W line is well separated from the others.
- There is no interruption of circuit all along the W lines.
- W line width is lower than expected due to a light overetching.
- Compared to the reference measured on full sheet GZO layer (R^2=40 ohm), R^2 of patterned GZO increase due to the decrease of the GZO thickness after etching (GZO is used as stop layer twice: for W and final opening etching).
- There is electrical contact between AlCu/W (pads).
- There is electrical contact between W/GZO (site for NWs).
- Homogeneity of GZO etching on a wafer could be still improved.

All wafers presents good electrical results. Some electrical defaults were highlights on 7 chips from P02 wafer.

10 Conclusion

6 months were devoted to the DEMO chips design and layout’s definition, process flow description, set of mask fabrication, electrical test development.
Moreover, 4 and an half months were dedicated to the only fabrication of DEMO Chips option 3 (top-bottom contact) in CEA clean-room. 8 wafers were processed with 43 chips on each wafer but the functionality is not assured on all wafer.
Some issues appeared throughout the process (e.g. equipment out of order), making it sometimes difficult and requiring to find adapted solutions.

The main technological achievements are:

- The feasibility of the technological steps in clean-room with:
  - The development of stable and reproducible process for the ZnO doped gallium etching
  - The development of stable and reproducible process for the W etching, e.g etching of thin lines well separated
  - The development of stable and reproducible process for the opening on the seed layer
- The development of specific electrical tests to characterize our chips before sending to partners
- The demonstration of feasibility of localized and contacted NWs growth on a processed 200mm silicon wafer (refer D4.3 and D5.3)

DEMO chips were sent to different partners for the DEMO next steps. Functional chips were sent to MTA EK MFA and ULEI for nanowires growth. Unfunctional chips were sent to Specific Polymer for polymer encapsulation test without nanowires and to Safran I&S and Fraunhofer for the calibration of bonding tests and test set-up.

Partners	Functionnal chips?	Number of chips	Date of delivery
MTA EK MFA	Yes	16 chips P01, 2 chips P02, 2 chips P04, 2 chips P06, 11 chips P07 and 2 chips P08.	02/02/17, 06/02/17, 01/03/17 and 14/03/17
ULEI	Yes	1 chip P01 and 2 chips P07	06/02/17
Specific Polymers	No	9 chips P03 and 9 chips P05	17/02/17 and 01/03/17
Safran Identity and Security	Yes but without nanowires	5 chips P07	02/02/17
Fraunhofer	No	2 chips P03 and 3 chips P05	17/02/17