E2SWITCH
Energy Efficient Tunnel FET Switches and Circuits

Co-funded by the European Union

E²SWITCH

Energy Efficient Tunnel FET Switches and Circuits

Grant Agreement No.: 619509

Funding Scheme: Collaborative project

Thematic Area: Energy efficient switch, tunnel FET, nanotechnology III-V, SiGe and Ge, low power integrated circuits, digital and analog/RF circuits, CMOS, simulation and modeling of nano-electronic devices & circuits

Project start date: 01-11-2013

Deliverable D3.2 — Complete intrinsic compact model for n- and p-TFETs

Nature[1]: R

Dissemination level[2]: PP

Due date[3]: M18

Date of delivery: M20

Lead partner: EPFL

Contributing partners: JUELICH

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[1] R = Report, P = Prototype, D = Demonstrator, O = Other

[2] PU = Public, PP = Restricted to other programme participants (including the Commission Services, RE = Restricted to a group specified by the consortium (including the Commission Services), CO = Confidential, only for the members of the consortium (including the Commission Services)

[3] Measured in months from the project start date (M01)

Revision history

Version	Date	Author	Comment
0.1	03-07-2015	Arnab Biswas	First draft
1.0	30-07-2015	Kirsten Leufgen, Adrian Ionescu	Final version, approved by the coordinator

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Contents

Summary

In this report, a compact model based on an analytical closed form solution of the 1D Poisson's equation for a double-gate Tunnel FET is presented. Furthermore, the current levels are estimated by implementing an algorithm based on the Kane's band-to-band tunneling model. A good agreement with numerical simulations for varying device parameters is demonstrated and the advantages and limitations of the modeling approach are investigated and discussed.

The model is implemented in a Verilog-A based circuit simulator and basic circuit blocks like an inverter, a 2-bit half adder and a 15 stage ring oscillator are simulated to demonstrate the capabilities of the model. The switching energy of a Tunnel FET based circuit block is studied with V_{DD} scaling revealing interesting aspects of Tunnel FET circuit behavior.

Furthermore, the model has been calibrated on experimental results for both n & p type devices fabricated by JUELICH on strained silicon substrates. The calibrated models are available in Verilog-A for both n & p-type devices, with full capability of simulating digital and analog circuits. An update with calibration on E^{2}SWITCH Consortium optimized complementary devices will be performed as soon as these devices will be made available.

1 DC Model Description

The model development will be described step by step in this section. We consider an n-type all-Silicon DG p-in TFET as shown in Fig. 1(a). A gate length L_G=22nm, channel thickness of t_{Si}=10nm, gate oxide thickness tox=3nm with HfO_2 gate dielectric, source (drain) doping of Boron (Arsenic) at $10^{20}cm^{-3}$ and channel doping of $10^{15}cm^{-3}$ are used for all the simulations unless specified otherwise. For simplicity we consider abrupt doping profiles and ignore band gap narrowing effects in the model. Fermi statistics is included in the simulations to account for the high doping levels used. The Poisson's equation is solved in 1D only in the gated intrinsic body region of the device. As a consequence, we ignore any band bending inside the un-gated source and drain regions. This is an acceptable approximation for high source/drain doping levels as required for typical TFET specifications.

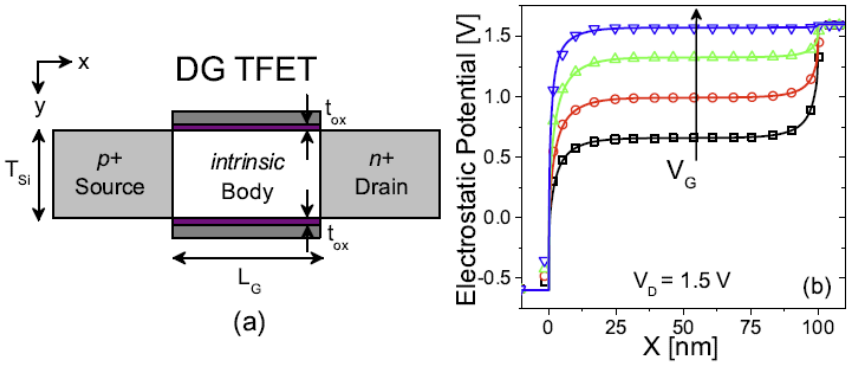


Figure 1: (a) Cross section of the device under study with typical dimensions marked (b) lateral potential profile of the channel in a DG-TFET at the oxide-Silicon interface at strong inversion for V_{GS}= 0,0.25,0.5,0.75,1V. Lines indicate the model and symbols TCAD simulation in all relevant plots.

1.1 Surface potential

The 1D Poisson equation is solved in the lightly doped body of the DG-TFET. Under the assumption of a 1D electric field [10] in the gate-oxide material the Poisson equation is transformed into a simplified form as in

$$\frac{\delta^2\psi_S}{\delta x^2} + \frac{\psi_{GS} - \psi_S}{\lambda^2} = \frac{qN_{ch}}{\epsilon_{Si}} \quad (1)$$

where ψ_S (x) is the surface potential, ψ_{GS} is the gate potential (= V_{GS} - V_{FB}) with V_{FB} being the flat band voltage, _Si is the dielectric constant of Silicon and _ is the natural length of a double gate structure [10]. The source and drain side side boundary conditions are defined as:

$$\psi_S(0) = (V_S - V_{B_{SRC}}) \text{ and } \psi_S(L_g) = (V_D + V_{B_{DRN}}).$$

With V_{BSRC} and V_{BDRN} being the built in potential of the source/drain-body junction respectively. The solution to (1) under the defined boundary conditions is given as:

$$\psi_S(x) = \psi_S^0 + (V_D - V_S + V_{B_{DRN}} + V_{B_{SRC}})\frac{\sinh(x/\lambda)}{\sinh(L_g/\lambda)} + \ldots$$
$$(V_S - V_{B_{SRC}} - \psi_S^0)\frac{\sinh(x/\lambda) + \sinh(L_g - x)/\lambda}{\sinh(L_g/\lambda)} \quad (2)$$

Where ψ_{0S} is the long channel surface potential of a DGTEFT from [11]. The results from (2) is compared to TCAD simulations in Fig. 1 (b) and show a good match.

1.2 Tunneling path estimation

Using the potential solution described above and the model described in [11], the hole band-to-band generation (B2BG) rate and the Fermi occupation is evaluated non-locally for an n-type device to understand the main operation regimes of a TFET. The operation of a TFET can be broadly divided in four regimes (i) OFF state (ii) ON state (iii) ambi-polar state (iv) breakdown state. Each of these states will now be explained to understand the device operation. Firstly, V_{DS}=0V results in zero Fermi occupancy window and hence zero tunneling current irrespective of the gate bias applied. In the ON state (e.g. $V_{DS} = V_{GS} = V_{DD}$), the positive V_{DS} applied results in a small Fermi window close to the source as shown in Fig. 2(a). The hole B2BG (in blue symbols) is confined just to the Fermi window (green solid line) as expected. In the ambi-polar case (e.g. $V_{DS} = V_{DD}$ and $V_{GS} = -V_{DD}$), as shown in the Fig. 2(b) the Fermi window shifts towards the drain and all the holes are generated only close to the drain. Finally, in the breakdown state (e.g. $V_{DS} >> V_{DD}$ and $V_{GS} = V_{DD}$), due to the large V_{DS} applied the Fermi window now extends across the entire body as shown in Fig. 2(c). Due to the very wide Fermi window, tunneling occurs near both source and drain junctions resulting in a large current.

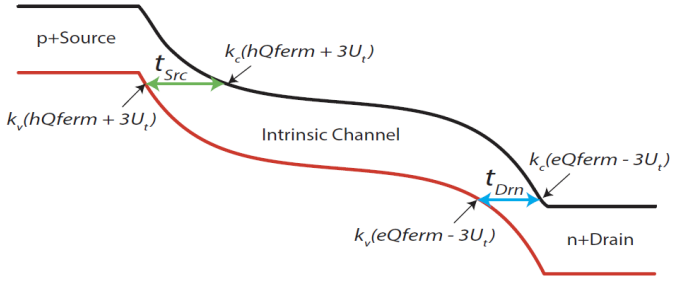
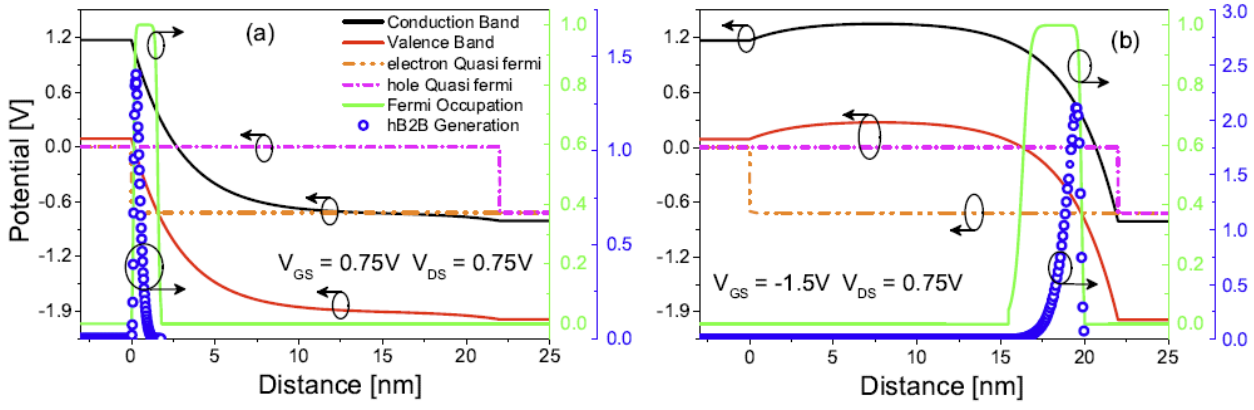


Figure 2: Schematic showing the location of the two tunneling paths considered. The breakdown state biasing is used here to show both the tunneling paths.

It is important to notice the location of the peak of the hole B2BG in all the three conducting states of a TFET in Fig. 2. On account of this observation, we can simplify the non-local tunneling process to a local process with the tunneling paths considered only at two locations: intersection of (i) ($hQferm + 3U_t$) level with the valence band and (ii) ($eQferm-3U_t$) level with the valence band, where U_t is the thermal voltage. The $\pm 3U_t$ term is included to consider the tunneling at the edges of the Fermi occupation window where the tunneling widths are the smallest. Fig. 3 shows the location of the ($e=hQferm - 3U_t$) levels along with the two tunneling paths. The above discussion is only for hole B2BG. The same analysis holds true for electron B2BG as well, which will be equal and opposite in magnitude to the hole B2BG.



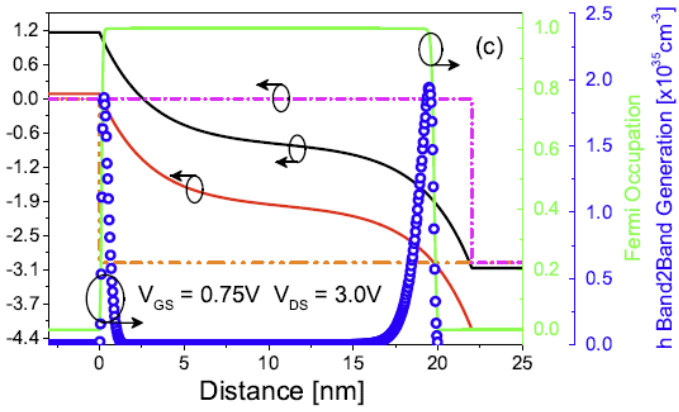


Figure 3: The operating regimes of a TFET (a) ON state with $V_{DS} = V_{GS} = V_{DD}$ (b) Ambi-polar state with $V_{DS} = V_{DD}$ and $V_{GS} = -V_{DD}$ (c) Breakdown state with $V_{DS} >> V_{DD}$ and $V_{GS} = V_{DD}$, where supply voltage V_{DD} = 0:75V.

1.3 Tunneling current calculation

The tunneling current consists of two components as explained in the section above. The Kane's model is used to estimate the tunneling generation rates from the tunneling width. The total tunneling current I_{tunn} is the calculated from the sum of G_{src} and G_{drn} as shown in (5).

$$G_{src} = A_{path}\left[\frac{E_g}{t_{src}}\right]^P \exp\left(\frac{-B_{path}t_{src}}{E_g}\right) \quad (3)$$

$$G_{drn} = A_{path}\left[\frac{E_g}{t_{drn}}\right]^P \exp\left(\frac{-B_{path}t_{drn}}{E_g}\right) \quad (4)$$

$$I_{tunn} = qW_{ch}t_{ch}\left(G_{src} + G_{drn}\right) \quad (5)$$

Where A_{path} and B_{path} are fitting parameters described in [12], P is a constant =2.5 for indirect tunneling [12], E_g is the energy band-gap of Silicon, q the electronic charge, W_{ch} & t_{ch} are the body width and thickness. t_{src} and t_{drn} are the source and drain side tunneling lengths defined as follows:

$$t_{src} = \kappa_C[CB(hQf + 3U_t)] - \kappa_V[VB(hQf + 3U_t)] \quad (6)$$

$$t_{drn} = \kappa_C[CB(eQf - 3U_t)] - \kappa_V[VB(eQf - 3U_t)] \quad (7)$$

where κ_C(E) and κ_V (E) are the inverse function of equation (2) which gives the values of position x for a given value of conduction band (CB) and valence band (VB) energy respectively. As described in section IIB and in Fig. 3, the tunneling lengths are evaluated by the difference in the position x, where the hole and electron quasi Fermi levels ±3Ut intersects the VB and the CB. κ(E) (evaluated in Matlab), gives us flexibility to choose a tunneling length at any point in the Fermi window. Hence, here we do not describe an expression for any specific tunneling path. Finally, a Fermi factor as described in [12] is multiplied to (5) to account for the available carriers at the beginning of the tunneling path, and for the available states into which they can tunnel, at the end of the tunneling path. This avoids non-zero current at V_{DS}=0V as well as results in a smooth and continuous current in all biasing conditions. This algorithm can be applied to any lateral tunneling TFET architecture, provided (E) exists for the surface potential solution used.

1.4 Comparison with simulations

The model is compared with TCAD [12] simulation results in this section. Fig. 4(a) shows the comparison of the transfer curves at three different V_{DS}. It can be seen that the model describes all the operation TFET regimes properly, including the ambi-polar regime in this case. Fig. 4(b) shows the output characteristics at three different V_{GS}. We can see from Fig. 4(b), that the model can describe the super-linear onset [6] and also the drain side breakdown of a TFET. This is possible due to physically meaningful assumptions and in particular the dual tunneling path consideration in this model. This algorithm is similar to a previously reported work [5], however, in this work we consider only 2 tunneling paths.

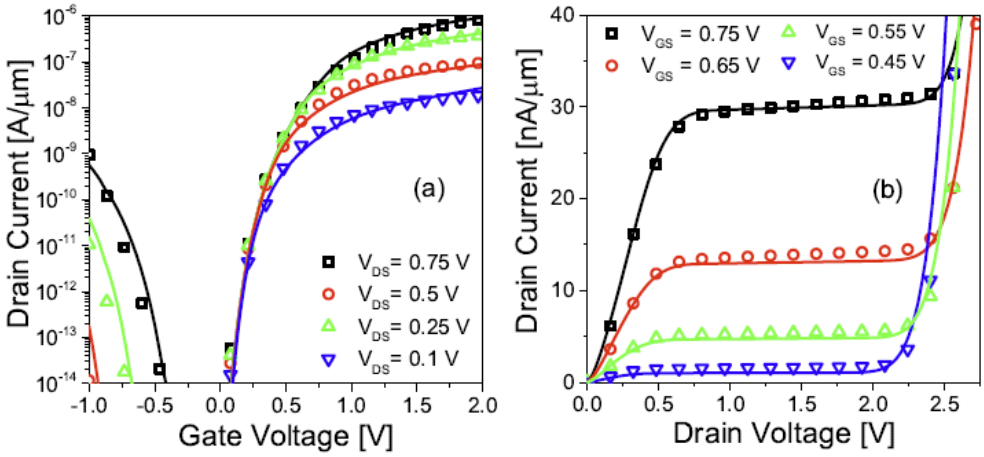


Figure 4: (a) Transfer characteristics for different V_{DS} (b) Output characteristics for different V_{GS}.

In Fig. 5(a) we compare the transfer curves for three different gate-oxide material at 3nm thickness. The effect of gate length scaling on a TFET is shown in Fig. 5(b). As expected, TFET has a weak dependence on gate length scaling (V_{DS}=constant), except when the gate length reduces to about 7.5nm, where the electrostatic control of the gate is too weak to have a reliable FET operation (for t_{ch}=10nm). As no leakage mechanism is included in this model at this stage, the match here is not perfect. However, the trend is captured correctly.

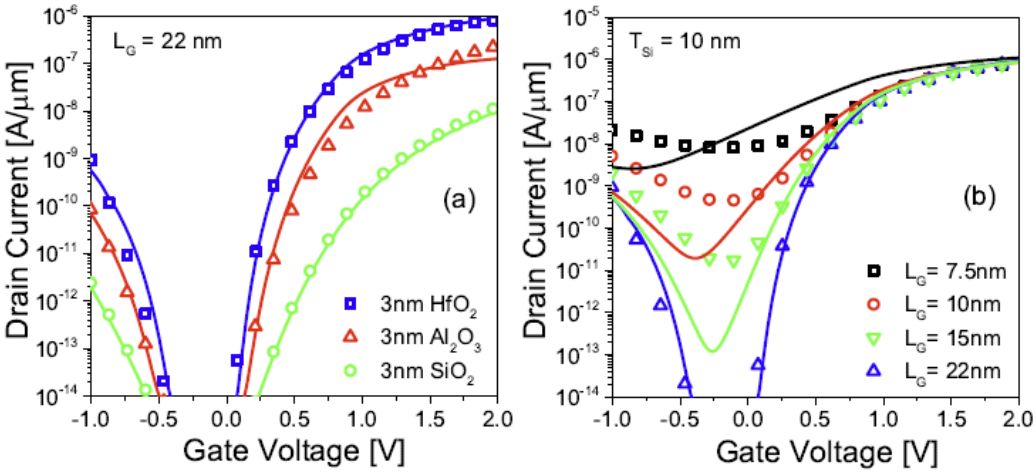


Figure 5: (a) Transfer curves with three different gate oxide material. (b) Transfer curves with gate length scaling with other parameters constant.

2 Charges in a TFET

In this section we present a simplified capacitance model for Double Gate TFETs**.** Capacitance-voltage measurements were done on all-Silicon SOI TFETs at different biasing schemes to support the model development. TCAD simulations of DG-TFETs were used to validate the model.

2.1 CV measurements and principle

Drain-gate capacitance was measured at different values of V_{DS} in Fig. 6b. Similarly source-gate capacitance was measured at different values of V_{DS} in Fig. 6c. We observe that gate-source capacitance (C_{GS}) under strong inversion remains negligible compared to gate-gate capacitance (C_{GG}) even at high V_{DS} = 1.5 V. So, it can be said that source has negligible contribution to the inversion charges, and that only depletion charges contribute to the source capacitance. Hence C_{GG} is dominated by the gate-drain capacitance (at least for low injection levels smaller than the depletion charges, as in the studied devices). This is also the reason for the strong miller effect in TFETs [4].

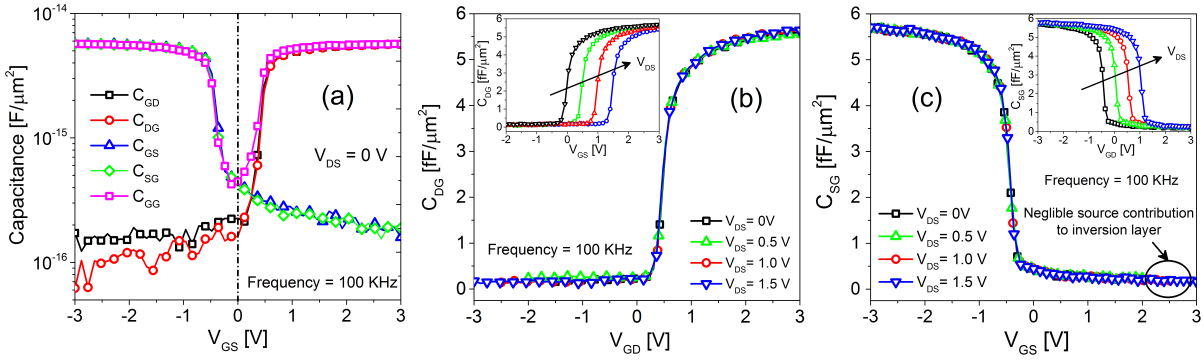


Figure 6: (a) Measured C_{GS}, C_{GD} and C_{GG} with respect to V_{GS}. Perfect symmetry is observed highlighting the ambi-polar nature of TFETs. (b) Measured Gate-Drain capacitance for different V_{DS}. Inset shows measured C_{GD} curves with respect to V_{GS}. (c) Measured Gate-Source capacitance for different V_{DS}

Further to the measurements, TCAD simulations were done to create a fictitious device TFET A with 2 orders of magnitude more current than a template 100 nm device in Fig. 7(top). As shown in the capacitance simulation in Fig. 7(bottom), the TFETA device with almost mA current level still has negligible C_{GS} compared to C_{GD}. TFET A shows a slightly higher C_{SG} and slightly lower C_{DG} compared to TFET B. This plot clearly shows that the additionally injected carriers from the source are still negligible compared to the inversion charge. So we can say that tunneling generated carriers has little or negligible role to play in the charge distribution of a tunnel FET. The following assumptions can now be taken reliably: (a) 100-0 charge partitioning scheme with 100% to drain. (b) Source depletion charge entirely dictates the source-gate capacitance.

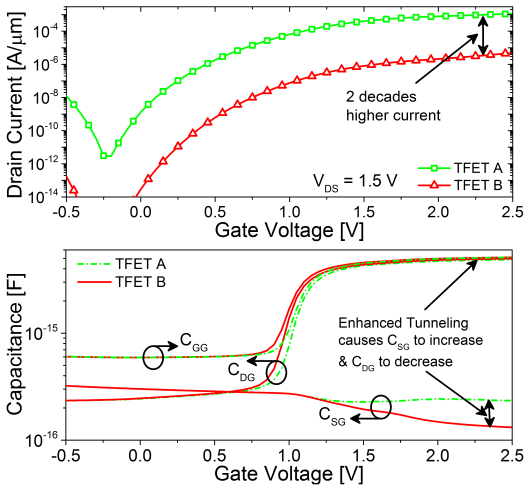


Figure 7: (top) TFET A simulated with artificially enhanced tunneling injection to have 2 order of magnitude more current than TFET B. (bottom) TFET A shows a slightly higher C_{SG} and slightly lower C_{DG} compared to TFET B. C_{SG} remains negligible compared to C_{DG} in TFET A.

2.2 Model Description

A 100nm double gate device with 3nm HfO_2 gate dielectric and 20nm silicon body thickness was used in the simulations. Source/drain doping was $1x10^{20}$ cm^{-3} and abrupt junctions were assumed. As described in [5], eqn. (8) is used to compute the gate charge Q_G. The gate charge Q_G is then used to compute the surface potential ψ_s in eqn. (9). The surface potential ψ_s is used with Gauss law to approximate inversion charges in eqn. (10). The drain-body depletion charge under the gate is also estimated by Gauss law in eqn. (11). The total drain charge is computed in eqn. (12) and finally the source charge is evaluated in eqn. (13) by the following charge conservation rule.

$$V_{GS} - V_{FB} - E_{fn} \approx \frac{Q_G}{C_{OX}} + U_T \ln\left(\frac{Q_G^2}{2\varepsilon_{Si} q U_T n_i} + \frac{2Q_G}{q n_i T_{Si}}\right) \quad (8)$$

$$V_{GS} - V_{FB} - \psi_s = Q_G / C_{OX} \quad (9)$$

$$Q_{D-INV} = C_{OX}(V_{GS} - V_{FB} - \psi_s)(L_G W_G) \quad (10)$$

$$Q_{D-DEPL} = \varepsilon_{Si}(V_{DS} + V_{BI} - \psi_s)(T_{Si} W_G)/\lambda \quad (11)$$

$$Q_{DRAIN} = -(Q_{D-INV}) + (Q_{D-DEPL}) \quad (12)$$

$$Q_{SOURCE} = -(Q_{DRAIN} + Q_G) \quad (13)$$

where λ is the characteristic length of a double gate structure, V_{BI} corresponds to the built in potential in the source-channel *pn* junction, U_T is the thermal voltage, C_{OX} is the gate-oxide capacitance, E_{fn} is the electron quasi Fermi level, V_{FB} is the flat band voltage, L_G and W_G are the length and width of the gate, V_{DS} is the gate-source bias, T_{Si} is the Silicon layer thickness. Capacitances are then evaluated as derivatives of the computed charges. Earlier work on capacitance behaviour of a TFET such as [18] is based on BSIM, whereas [19] also compute charges but do not discuss capacitances voltage behaviour.

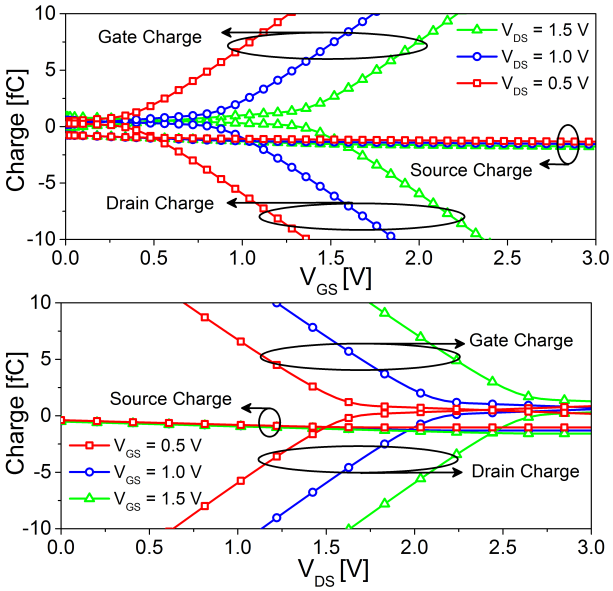


Figure 8: Modelled gate, drain and source charges of an n-type double gate tunnel FET (top) as a function of gate-source voltage and (bottom) as a function of drain-source voltage.

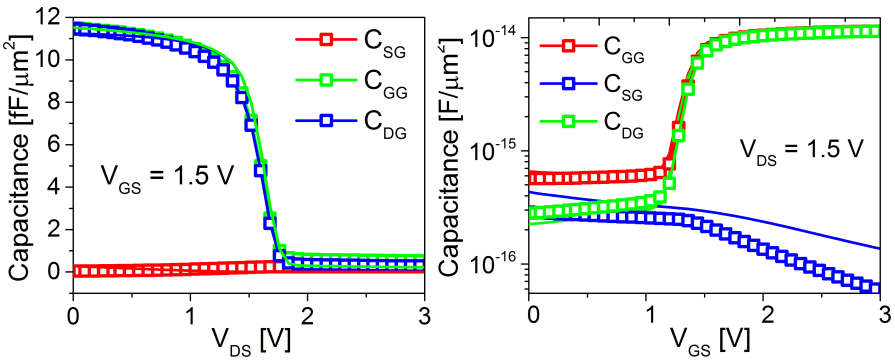


Figure 9: C_{SG}, C_{DG} and C_{GG} with respect to drain-source voltage at V_{GS}=1.5V (left) and gate-source voltage at V_{DS}=1.5V (right) computed by the simplified model and comparison with TCAD simulations. Symbols indicate simulations and solid lines indicate model for all relevant figures.

2.3 Comparison with TCAD simulations

The drain, source and gate charges with respect to V_{GS} and V_{DS} are shown in Fig. 8. As discussed earlier source charges remain negligible compared to drain charges even at V_{DS} = 1.5 V. The capacitance curves with respect to gate-source voltage (top) and drain-source voltage (bottom) are shown in Fig. 9. We see that in spite of the approximations introduced the model estimates the trans-capacitances with relative accuracy both above and below the inversion threshold. Finally as shown in Fig. 10, the model also works for varying drain voltages for C_{GG}, C_{SG} and C_{DG} @ V_{DS} = 0.5V, 1.0V, 1.5V. C_{SG} particularly shows large discrepancy due to the assumption of a constant depletion width for all T_{SI}. However the shape and the variation with V_{DS} and V_{GS} is captured in this model.

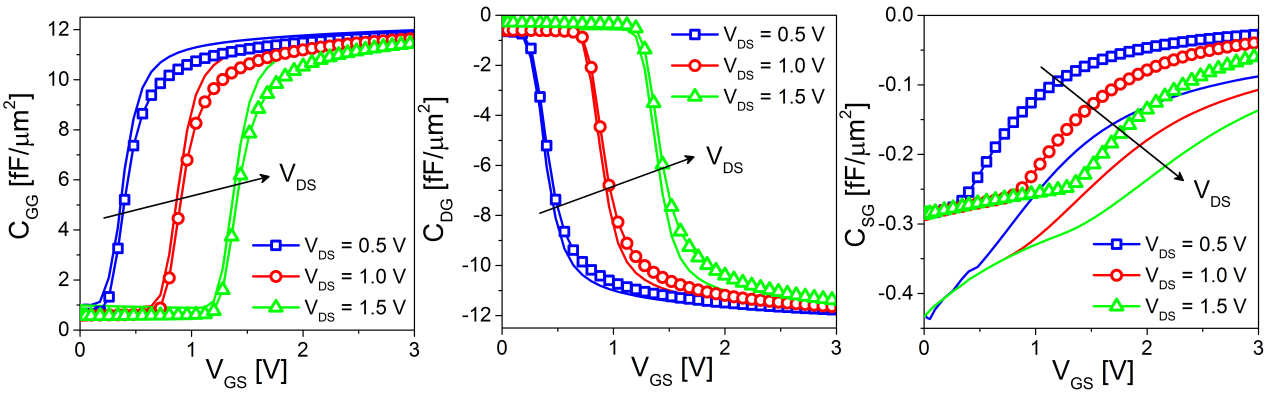


Figure 10: Modelled C_{GG}, C_{DG} and C_{SG} curves with respect to V_{GS} for three different drain voltages and comparison with TCAD simulations. Modelled C_{SG} curves with respect to V_{GS} although do not show a good match, predicts the trend correctly.

3 Verilog-A Implementation

The model described above has been implemented in Verilog-A. Simple circuit level simulations were carried out using Cadence Virtuoso. A p-type device was emulated from the n-type device for this study. To ensure continuity and smoothness of the model in all bias conditions, a basic diode model was added to take into account negative V_{DS}. This results in the typical uni-directional conduction feature of a TFET [9]. The dynamic behavior of TFETs is modeled with a 100/0 charge partitioning scheme with 100% to drain [9], [13]. Tunneling generation is assumed to be time independent and to have no impact on the charge distribution in a TFET. In order to show the capability of the model to capture the unique features of TFETs in circuit simulations, some based basic circuit blocks are simulated in this section. The model parameters and their values used in the following simulations are shown in table 1.

TABLE I
MODEL PARAMETERS AVAILABLE IN VERILOG-A

Parameter	Value	Parameter	Value
$A_{path}[cm^{-3}s^{-1}]$	$2.4 \cdot 10^{13}$	$N_{Src}/N_{Drn}[cm^{-3}]$	10^{20}
$B_{path}[V\,cm^{-1}]$	$3.3 \cdot 10^{7}$	$t_{ch}[nm]$	10
$L_g[nm]$	22	$t_{ox}[nm]$	3
$W_{ch}[\mu m]$	1	ϵ_{ox}	21
$Type\ (n\ or\ p)$	1 or -1	Gate work function $[V]$	4.1

3.1 Single stage inverter

A TFET based single stage inverter is simulated with different operation voltages (V_{DD}). The voltage transfer characteristic (VTC) is plotted in Fig. 11(a) and Fig. 11(b) shows the voltage gain for V_{DD}= 0.1 to 1V. A relatively high gain of 5 is observed for V_{DD} as low as 0.2V. However, as shown in Fig. 11(c), the inverter output during transient simulations shows large overshoots and undershoots with V_{DD}=1V and no load capacitance. This is due to the enhanced Miller capacitance originating from the 100/0 charge partitioning scheme of TFETs [13]. The over/under shoot is reduced by adding a load capacitance C_L= 2fF, however at the cost of an increased propagation delay from 12ns to 18ns (Fig. 11(c)).

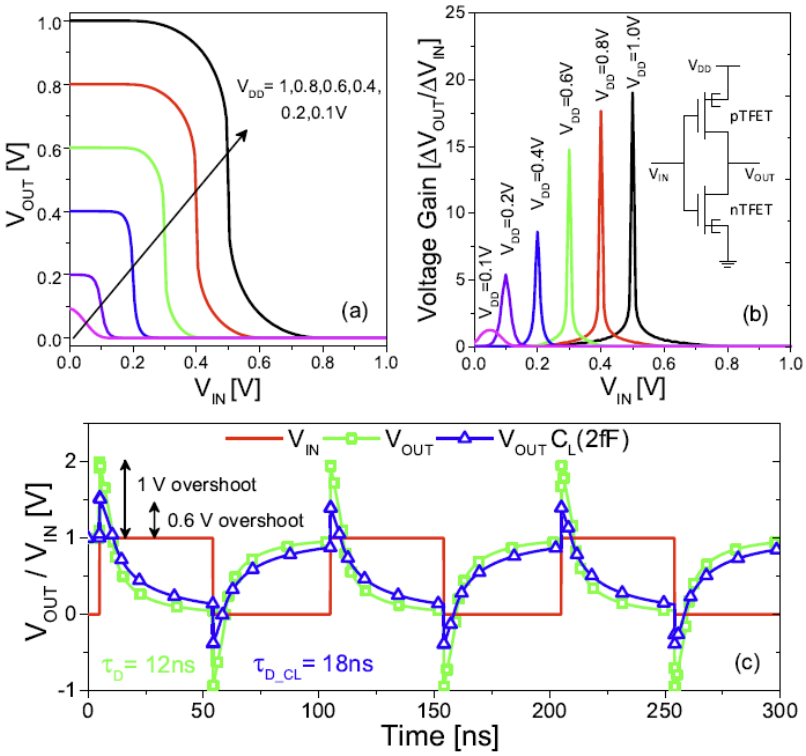


Figure 11: (a) VTC of a TFET based single stage inverter with V_{DD} 0.1V to 1V. (b) Voltage gain of the inverter for the same V_{DD} range. Inset shows the simulated single stage inverter. (c) Transient response of a single stage TFET inverter at V_{DD}=1V with C_L=0fF and C_L=2fF.

3.2 2-bit half adder

As benchmarking studies [14] commonly use 32 bit adders, we simulate here a 2-bit half adder. Fig. 12(a) show the input signals and Fig. 12(b) show the output sum and carry signals of a 2-bit half adder comprising a XOR and an AND gate.

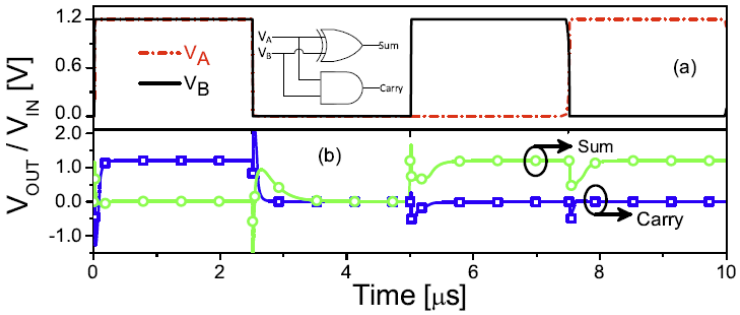


Figure 12: All-Silicon 22nm TFET based 2-bit half adder with V_{DD}=1.2V (a) the two input signals V_A and V_B (inset shows the schematic of the simulated 2-bit half adder) (b) the sum and carry output signals.

3.3 15 stage ring oscillator

A TFET based 15 stage ring oscillator is simulated for a V_{DD}=1V. The typical oscillation behavior of the outputs of first five odd numbered stages are shown in Fig. 13(a). The high over and under shoots are present as expected for a typical TFET. An oscillation period of 2.38μs is observed which gives a delay of 79.4ns (τ_D = period/2N, with N = 15).

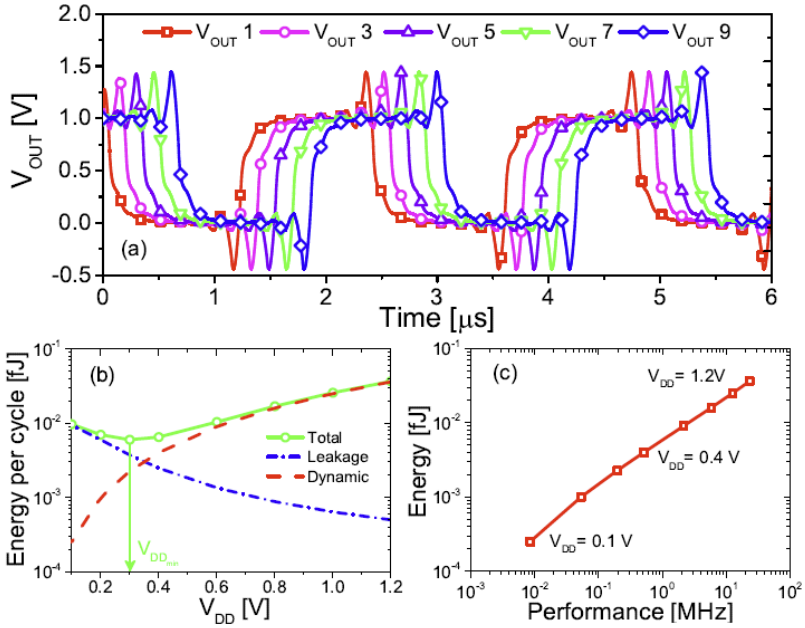


Figure 13: (a) All-Silicon 22nm TFET based 15 stage ring oscillator output for V_{DD}=1V. A delay of τ_D=79.4ns is observed. (b) Leakage, dynamic and total energy with V_{DD} scaling (c) Switching energy-performance comparison.

Fig. 13(b) shows the leakage, dynamic and the total energy [1], [15] with V_{DD} scaling. At 1% activity factor (typical for low power applications), we can see that the leakage energy dominates for lower V_{DD}. The V_{DD} at the point of minimum total energy, V_{DDmin} is seen at a relatively low value of 0.3V. Fig. 13(c) show the switching energy-performance comparison [1], [16]. At lower performance range, TFETs are expected to be more energy efficient than comparable CMOS technology [16]. In this work, we do not perform any benchmarking with CMOS technology as the TFET used in the simulations is not optimized for a given technology node.

4 Model callibration with experimental results

Fig. 17 depicts a schematic of the fabricated device in Juelich and process steps, validated in [17]. The investigated strained Si (sSi) NW array TFETs have nanowire cross section of 30×5 nm² (Fig.2), gate length of 350 nm and ~1.4GPa tensile strain booster (translated into bandgap reduction of the order of 95 meV per 1% axial strain). The gate stack applied on NW consists of 3nm HfO2 and 40nm TiN as gate metal. The source/drain (S/D) junctions are formed by tilted P+ and B+ implantations.

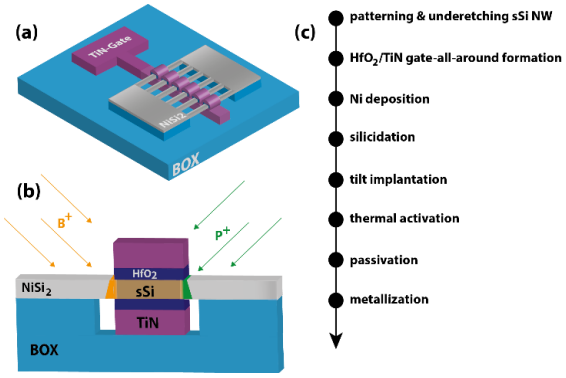


Figure 17: (a) Schematic of the fabricated sSi NW TFET with TiN/HfO_2 gate stack (b) Highly doped n+ and p+ pockets at the silicide edges are formed after a low temperature anneal (c) sSi NW TFET fabrication process using tilted B+ and P- ion implants into epitaxial $NiSi_2$ S/D contacts.

TFET transfer and output characteristics (Fig. 15 and 16) were measured from 25°C to 125°C and the model was accordingly calibrated with very good accuracy. We show that for both p- and n-type TFET the subthreshold swing (in the regions where BTBT dominates), the on-current, I_{ON}, and, the transconductance, g_m, have less dependence on temperature than CMOS (Fig. 17 and 18). Particularly remarkable is the reduced temperature dependence of g_{max} (Fig. 18) and of threshold voltage, V_T (Fig. 19) for sSi TFETs. The calibrated model does not take into consideration the trap-assisted tunneling (TAT), a fabrication artifact which partially affects the swing and its dependence on temperature due to defects at the interface HfO_2/Si and at the junctions (following tilted ion implantation and limited temperature annealing). The model includes temperature dependent SRH leakage. The calibration parameters are shown in the table below:

Table 1.4: Table of fitted parameter list for Verilog-A based model for both n & p type device at room temperature.

Model Parameter	n-type	p-type
$A_{path}[cm^{-3}s^{-1}]$	$7.2x10^{15}$	$6x10^{7}$
$B_{path}[V/cm]$	$8.4x10^{7}$	$9.3x10^{7}$

4.1 Transfer and output characteristics

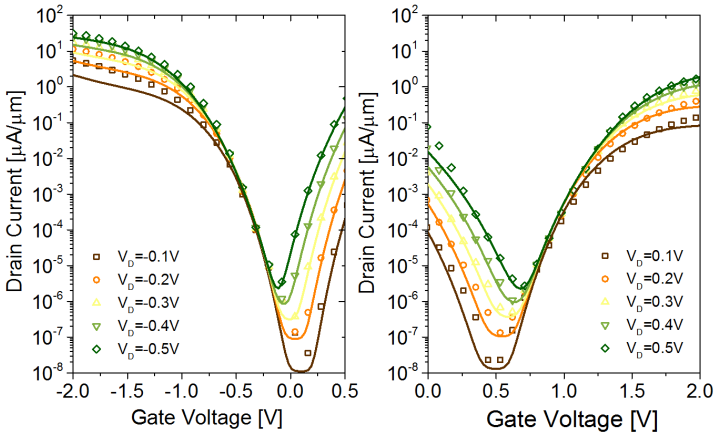


Figure 15: Measured transfer characteristics and calibrated model at different V_{DS} of the fabricated sSi NW TFET for (left) p-type and (right) n-type TFET at room temperature (Symbol: measurement, lines: model)

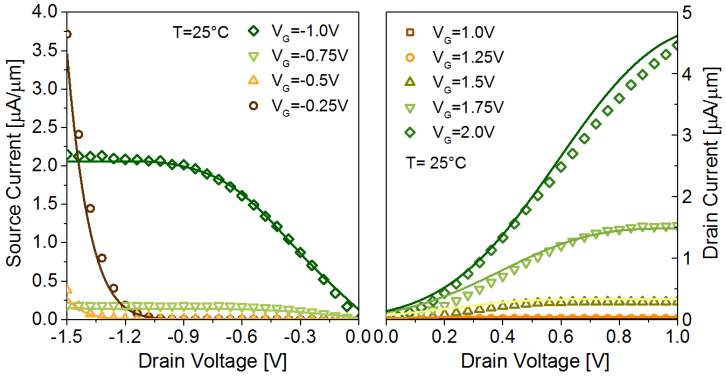


Figure 7: Measured output characteristics and calibrated model at different V_{GS} for (left) p-type (right) n-type TFET at room temperature.

4.2 Temperature dependent measurements

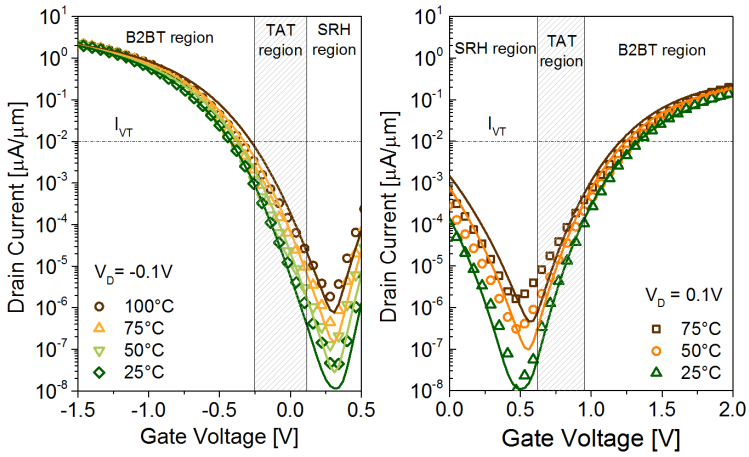


Figure 8: Measured transfer characteristics with temperature (25°C to 100°C) with calibrated model; achieved I_{ON} is ~20µA/µm and ~2µA/µm for p- and n-type sSi homo-junction NW TFET at V_{GS}=1.5V and min point swings, SSpt ~70-100mV/dec at room temperature and I_{OFF} <1-10nA/µm.

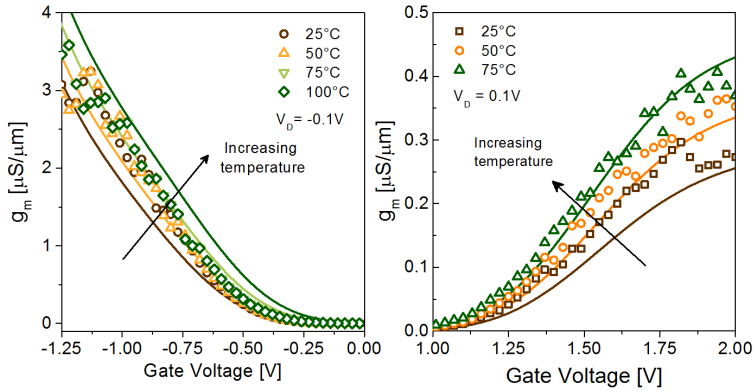


Figure 9: Measured transconductance and calibrated model at $|V_{DS}|$=0.1V with respect to temperature for p type (left) and n type (right) TFET.

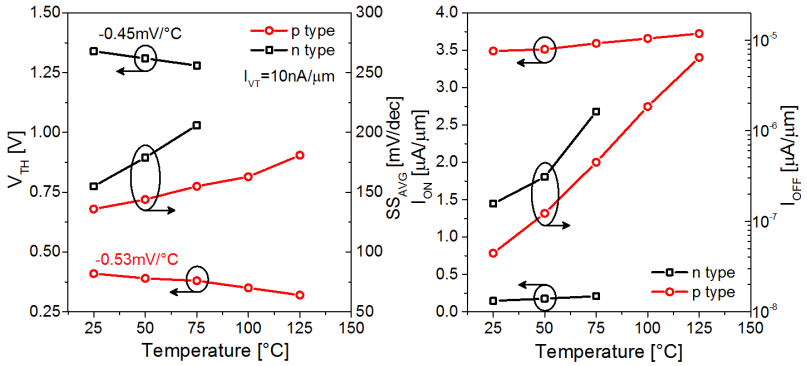


Figure 10: (Left) experimentally extracted V_{TH} and average subthreshold swing, SS_{AVG}, (over 4 decades of current) dependences, and, (right) I_{ON} and I_{OFF} dependences on temperature, from 25°C to 125°C.

5 Conclusions

In this report, we have developed a physics-based compact model for DG-TFETs describing all tunneling-related characteristics and implemented it in Verilog-A for circuit simulations. The model agrees well with TCAD simulations in all regions of operation. A simplified capacitance-voltage model is also presented. Using the model to perform basic circuit simulations has revealed some unique features of a TFET.

Additionally temperature dependence was added to the model which stems primarily from the energy bang gap dependence on temperature. Finally devices fabricated by Juelich were measured from room temperature to 125°C. IV and CV characteristics of both n and p-type devices were measured. The model was calibrated to the measurements for both n & p-type devices including the temperature dependence. The calibrated model is available to the consortium in Verilog-A form for circuit simulations.

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