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Contents

1 Introduction

In this report, we report on the compact modelling of TFETs including layout parasitics. Both Si and III-V models were planned to be delivered at the beginning of the project.

EPFL provided silicon Verilog-A model calibrated on experimental results for both N & P type devices fabricated by JUELICH. However, as it was shown in D6.1, performance of those devices was poor. Thus, we briefly discuss the Silicon model and focus on the III-V modelling.

Imec provided III-V Verilog-A model calibrated on experimental results for N type devices fabricated by Lund University and supported by TCAD simulations from ETHZ. The model has modular structure allowing to assess the impact of traps independently from the intrinsic device performance.

Parasitics modelling of vertical devices was performed by imec and was based on process assumptions for the scaled logic designs, because that's the only likely interception point for vertical architecture. Yet, the parasitics model is analytical and parameterized, so it could be upscaled to be suitable for the Lund vertical TFET devices. Combined with the core model, imec assessed the impact of the parasitics on device performance, both on DC level and on ring oscillator (RO) level.

2 Core TFET Model

2.1 Silicon model based on experimental data

EPFL developed a compact model based on the solution of the 1D Poisson equation in the lightly doped body of the DG-TFET. Under the assumption of a 1D electric field [1] in the gate-oxide material the Poisson equation is transformed into a simplified form as in (1).

$$\frac{\partial^2 \psi_S}{\partial x^2} + \frac{\psi_{GS} - \psi_S}{\lambda^2} = \frac{qN_{ch}}{\epsilon_{Si}} \quad (1)$$

where $\psi_S(x)$ is the surface potential, ψ_{GS} is the gate potential ($= V_{GS} - V_{FB}$) with V_{FB} being the flat band voltage and λ is the natural length of a double gate structure [1]. The source and drain side boundary conditions are defined as $\psi_S(0) = (V_S - V_{B_{SRC}})$ and $\psi_S(L_g) = (V_D + V_{B_{DRN}})$, with $V_{B_{SRC}}$ and $V_{B_{DRN}}$ being the built-in potential of the source/drain-body junction respectively. The solution to the above equation under the defined boundary conditions is given as:

$$\psi_S(x) = \psi_S^0 + (V_D - V_S + V_{B_{DRN}} + V_{B_{SRC}}) \frac{\sinh\left(\frac{x}{\lambda}\right)}{\sinh\left(\frac{Lg}{\lambda}\right)} + (V_S - V_{B_{SRC}} - \psi_S^0) \frac{\left(\sinh\left(\frac{x}{\lambda}\right) + \sinh\left(\frac{Lg-x}{\lambda}\right)\right)}{\sinh\left(\frac{Lg}{\lambda}\right)} \quad (2)$$

where ψ_S^0 is the long channel surface potential of a DGTFET from [2].

Using the potential solution described above and the model described in [2], the hole band-to-band generation (B2BG) rate and the Fermi occupation is evaluated non-locally.

The tunneling current consists of two components. The Kane's model is used to estimate the tunneling generation rates from the tunneling width. The total tunneling current I_{tunn} is the calculated from the sum of G_{src} and G_{drn}:

$$\boldsymbol{G_{src} = A_{path}\left[\frac{E_g}{t_{src}}\right]^P exp\left(-\frac{B_{path} t_{src}}{E_g}\right)} \quad (3)$$

$$\boldsymbol{G_{drn} = A_{path}\left[\frac{E_g}{t_{drn}}\right]^P exp\left(-\frac{B_{path} t_{drn}}{E_g}\right)} \quad (4)$$

$$\boldsymbol{I_{tunn} = qW_{ch}t_{ch}(G_{src} + G_{drn})} \quad (5)$$

where A_{path} and B_{path} are fitting parameters per [3], P is a constant =2.5 for indirect tunneling [3], E_g is the energy band-gap of Silicon, q the electronic charge, W_{ch} & t_{ch} are the body width and thickness. t_{src} and t_{drn} are the source and drain side tunneling lengths defined as follows: $t_{src} = \kappa_C[CB(hQf + 3U_t)] - \kappa_V[VB(hQf + 3U_t)]$, $t_{drn} = \kappa_C[CB(eQf - 3U_t)] - \kappa_V[VB(eQf - 3U_t)]$ where $\kappa_C(E)$ and $\kappa_V(E)$ are the inverse function of equation (2) which gives the values of position x for a given value of conduction band (CB) and valence band (VB) energy respectively. Figure 2-1 illustrates the simulation results obtained with the model calibrated and compared against experimental TFET structures fabricated by JUELICH within the E2SWICTH project, where an excellent agreement is seen.

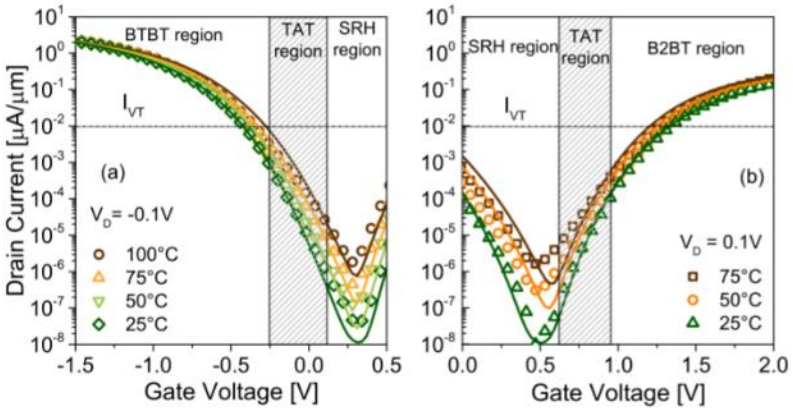

Figure 2-1: Measured Id-Vg (symbols) with temperature (25–100°C) and with calibrated model (lines) [4].

2.2 III-V model based on experiment-calibrated TCAD data

A semi-analytical compact model addressing the I-V and Q-V characteristics of III-V TFETs was developed at imec and calibrated to TCAD simulation data of a vertical InAs/InGaAsSb/GaSb nanowire TFET from ETHZ. This TCAD deck, which was in turn based upon experimental results of an N-type TFET from Lund University, had managed to capture the essential I-V characteristics observed in measurement [5] and complemented to lab-measured data the missing charge information at varying gate and drain biases, providing a reliable basis for predicting the capacitance behavior in circuit operation and a consistent data source for compact model calibration involving both I-V and Q-V; moreover, with well-calibrated traps in the TFET device, the deck offered great flexibility in estimating different device physics components present in a realistic device by selectively switching on specific types of traps, thus paving the way for separating different current conduction mechanisms which further facilitated model calibration.

Based on the ON/OFF status of "bulk traps" and "oxide traps", imec considered the following three components as the constituents of the I-V model: the band-to-band-tunneling (BTBT) current conduction, the trap-assisted-tunneling (TAT) current conduction and the electrostatic effect due to charged oxide traps. While the first two concerns primarily the I-V characteristics and were modelled with analytical equations from literatures [6 – 8], the last term that addresses the specific device was captured by a look-up table and was used to modify both I-V and Q-V characteristics to mimic the reality-based TCAD simulation data. For the Q-V model, the semi-empirical equations presented in [8] have been shown to be sufficiently compact yet containing reasonable physical assumptions; hence they were adapted into imec Q-V model which allows for circuit simulations over a broader bias range.

2.2.1 I-V model

2.2.1.1 BTBT conduction

Analytical BTBT conduction have been widely reported focusing on various TFET device architectures [6]. Imec I-V model in its BTBT part adopted the philosophy of [6] in maintaining both the device physics and the architecture-blind versatility but also incorporated a few additional innovations in its formalism.

Under the assumption of Kane-Sze model, the current density equation per [6] could be written as the following,

$$J = A_{BTBT}\,\xi exp\left(-\frac{B_{BTBT}}{\xi}\right)V_{TW}f \quad (6)$$

where A_{BTBT}, B_{BTBT} are BTBT coefficients defined by material properties; ξ is the maximum electrical field at source-channel junction; V_{TW} is the so-called "tunneling window" the refers to the cross-over of valence band maximum in source and conduction band minimum in channel; f is an empirical form factor that modulates the overall I-V profile.

In the original formalism in [6] imec identifies the following elements as integral to an BTBT conduction model:

a. A unified expression for V_{TW} for both subthreshold and above-threshold regimes with smooth transitioning.
b. Variable subthreshold slope characterized by introducing a linearity factor γ_0 ($0 < \gamma_0 < 1$) that accounts for the degree of nonlinearity of log(Id) versus Vg in subthreshold regime. Note γ_0 that is a fitting parameter left for calibration to specific device data.
c. Fitting parameters λ, Γ ($0 < \lambda, \Gamma < 1$) in form factor f that help to capture the "negative transconductance" (or in other words, "superlinear onset" on output characteristics) and V_{DS} saturation effect.
d. Linear and constant gate and drain bias dependence of ξ, with fitted linear coefficients.

On top of these assumptions, imec has further proposed to incorporate the following ingredients:

e. The drain bias dependence of subthreshold ideality factor n, threshold voltage V_{TH} and off voltage V_{OFF}, i.e., the electrostatic effect. Therefore,

$$X_i = X_{i0} + Y_{i0}V_{DS}^{Y_{i1}} \quad (7)$$

whereby X_i = n, V_{TH}, V_{OFF}; X_{i0} are values of them taken at zero drain bias; Y_{i0} and Y_{i1} are the individual pre-factors and power indices for V_{DS} dependence of the three different variables,

respectively ($Y_{i0} < 0$, $Y_{i1} > 0$). The values of X_i, X_{i0}, Y_{i0} and Y_{i1} are subject to calibration to given data series.

f. Ambipolar current ($V_{GS} < V_{OFF}$) simplified as a constant leakage floor I_{leak}, namely ambipolar conduction is suppressed as ideally.

g. Under forward drain bias, the current conduction is default to the leakage floor I_{leak}, assuming the forward tunneling is so inefficient as can be neglected and the absolute value of negative V_{DS} is sufficiently small such that forward diode current does not set in.

Under assumptions a to g, the overall BTBT current can be summarized as

$$\begin{cases} I_{BTBT} = \max(I_{leak}, W_{eff} t_{ch} A_{BTBT} \xi exp\left(-\frac{B_{BTBT}}{\xi}\right) V_{TW} f) \ (V_{GS} > V_{OFF}, V_{DS} > 0) \\ I_{BTBT} = I_{leak} \ (V_{GS} < V_{OFF}, V_{DS} > 0) \\ I_{BTBT} = I_{leak} \ (V_{DS} < 0) \end{cases} \quad (8)$$

where W_{eff} is the effective channel width, t_{ch} is the channel thickness, and A_{BTBT}, B_{BTBT} are BTBT coefficients defined by material properties [6]. Note that (8) describes current in one single nanowire; for a real device with multiple nanowires the current will be multiplied by the number of wires.

Figure 2-2 (a) shows the current-voltage curve from the DC simulation calibrated compact model plotted against the TCAD data from ETHZ, with device architecture assumptions given by [5]. In this set of simulation both "bulk traps" and "oxide traps" were turned off hence only BTBT conduction was contributing to the overall current. From the Id-Vg curves it is clear that except for the ambipolar current, the overall I-V characteristic is nicely captured up to V_{GS} = 0.4 V, including the drop in current with increasing V_{GS} for V_{DS} = 0.05 V at V_{GS} high than ~0.2 V (known as "negative transconductance"). More interestingly, the compact modelled output characteristics (Figure 2-2 (b)) is proved to capture the trait of "superlinear onset" effect in the TCAD data in which the current at very small V_{DS} values (< 0.2 V) grows slower at higher V_{GS} than at lower V_{GS} – this is exactly the Id-Vd representation of "negative transconductance" on Id-Vg curves. It should be noted that the BTBT model is not specifically developed for the device presented in [5], but by simply adjusting the fitting parameters λ, Γ in the form factor it has been attested to carry the peculiar I-V signature of this device and hence proved its flexibility.

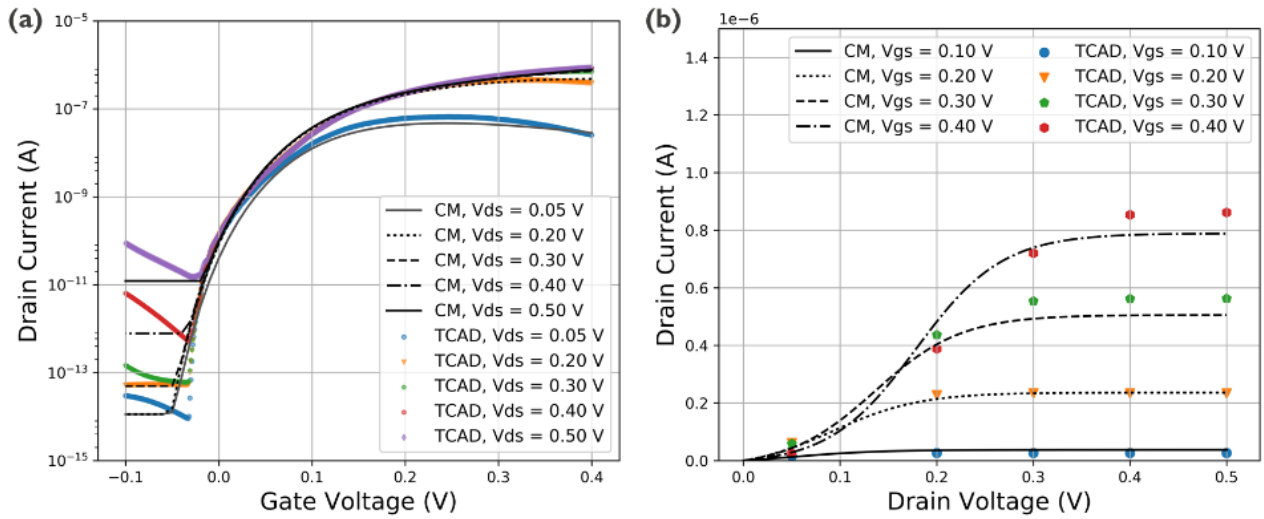

Figure 2-2: TCAD simulated (symbols, whereby both "bulk traps" and "oxide traps" were turned off) and calibrated compact model simulated (curves, denoted as "CM") (a) Id-Vg and (b) Id-Vd characteristics for one nanowire TFET (T = 300 K). Note the pronounced "superlinear onset" effect in (b), especially for V_{GS} = 0.4 V.

2.2.1.2 I-V model: TAT conduction

Bulk traps have been revealed to be a major contribution to subthreshold swing degradation [5], mainly through TAT at the source/channel GaAsSb/InAs heterojunction. It has been shown that with the introduction of bulk traps a secondary conduction channel, namely TAT, would have been turned on before the gate bias is high enough to switch the tunneling window for BTBT, which inevitably augments the

leakage floor and degrade the ideal subthermal swing of BTBT. To account for this, imec proposed to add to a second conduction mechanism in parallel with BTBT – the TAT model to reflect the observation from TCAD data in [5].

Imec considers the TAT model as the tunneling effect at the reversely-biased source-channel junction modulated by the form shaping effect similar to that in the BTBT model. The tunneling effect per [8] is described as an enhanced Shockley-Read-Hall (SRH) carrier generation process in the depletion region, while the overall charge generation is integrated over the entire length of depletion region, which timed by the form factor gives the TAT current density. The formalism reads

$$R_{TAT} = G_{TAT} R_{SRH} \quad (9)$$

$$J_{TAT} = q R_{TAT} l_{dep} f' \quad (10)$$

where R_{TAT}, G_{TAT}, R_{SRH} are the TAT generation rate, enhancement factor, SRH generation rate, respectively; l_{dep} is the equivalent depletion region length at the source-channel junction which is intended to represent the integration of R_{TAT} with spatial variation and is a fitting parameter; f' is the form factor that dictates TAT current which is given by (11)

$$f' = \frac{1 - exp\left(-\frac{V_{DS}}{\Gamma'}\right)}{1 + exp\left(\frac{\lambda' \tanh(V_{GS} - V'_{OFF}) - V_{DS}}{\Gamma'}\right)} \quad (11)$$

Similar to the treatment in [6], f' is expressed as a function of λ', Γ' and V'_{OFF} which bear similar meanings but different values to their counterparts found there.

The enhancement factor G_{TAT} in (9) per [8] considers the emission of a trapped carrier as a combination of thermal excitation (from trap level E_T to within the energy window ΔE to E_C as shown in Figure 2-3) and subsequent tunneling to the channel. The formalism reads,

$$G_{TAT} = \frac{\Delta E}{k_B T} \int_0^1 \exp\left[\frac{\Delta E}{k_B T} u - \frac{4}{3} \frac{\sqrt{2m^*} (\Delta E)^{3/2} u^{3/2}}{q\hbar\xi}\right] du \quad (12)$$

where k_B is the Boltzmann's constant, m* is the reduced tunneling effective mass.

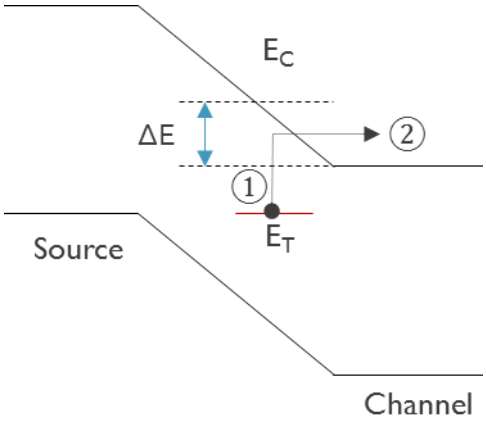

Figure 2-3: Emission of a trapped carrier at energy level E_T: thermal excitation (step 1) and subsequent tunneling (step 2).

Finally, the TAT current is expressed as

$$I_{TAT} = W_{eff} t_{ch} J_{TAT} \quad (13)$$

It should be pointed out that a successful TAT model should not only be able to capture the essential feature of early turn-on in subthreshold, but also capable of converging to a slowly-growing current component at high gate bias where BTBT conduction completely dominates. Therefore, special attention should be given to the empirical form factor f' as it is the only term in the formalism that is able to damp the current at increase gate bias while other factors keep monotonically growing with V_{GS}. Consequently the fitting parameters in (11) have to be properly chosen so as to satisfy these requirements.

While in principle the overall effect of bulk traps should also include the SRH generation current I_{SRH},

$$I_{SRH} = W_{eff} t_{ch} J_{SRH} = W_{eff} t_{ch} q R_{SRH} l_{dep} \quad (14)$$

compared to I_{TAT}, I_{SRH} is significantly small in magnitude owing to the nature of TAT as enhanced SRH effect and is thus ignored in the overall current contribution, which turned out to be a safe assumption from the model calibration result (see below).

Figure 2-4 shows the compact modelled I-V curve plotted against TCAD data from ETHZ. The bulk trap distribution was reduced to an equivalent single location, with trap energy level, trap density and interaction volume aligned to in [5]. Hence in compact model based DC circuit simulation both BTBT conduction and TAT conduction were introduced. Compared to Figure 2-2a, the leakage floors at various V_{DS} are drastically elevated and the onset slope (~V_{GS} < 0 V) are degraded, which comes exactly from the contribution of TAT current introduced by bulk traps at low V_{GS} before BTBT conduction sets in. However, with the addition of TAT conduction model on top of the BTBT model, it is observed that the subthreshold regime is reasonably fixed with the correct estimation of the order of magnitude of current at low gate bias (again except for the ambipolar current); and even if the fitting is not perfect it is expected to be able to reflect the impact of subthreshold degradation when going to simulations that mimic the operation of circuits. At the same time, both the TCAD data and compact model simulation confirm that TAT conduction is overwhelmed by BTBT conduction at higher gate bias, where the Id-Vg data is captured by the BTBT model alone.

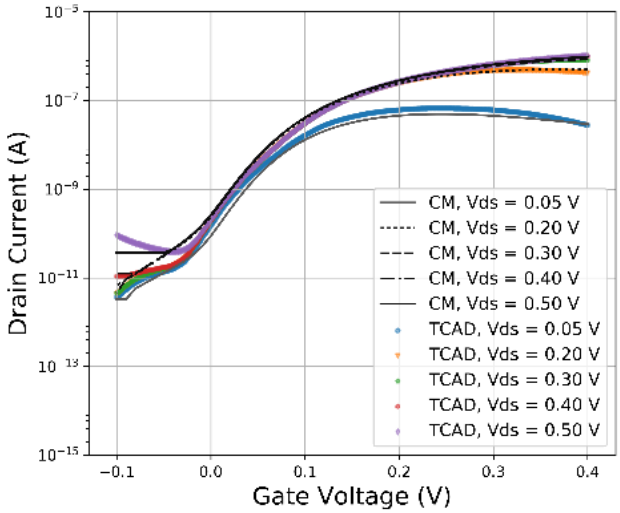

Figure 2-4: TCAD simulated (symbols, whereby "bulk traps" were turned on whereas "oxide traps" were turned off) and calibrated compact model simulated (curves, denoted as "CM") Id-Vg characteristics for one nanowire TFET (T = 300 K)

2.2.1.3 I-V model: electrostatic effect of charged gate oxide traps

Charged interface states at channel/gate oxide have been shown to give rise to change in electrostatic control of the gate stack [5]. On one hand, if these interface states behave in a donor-like manner, they will positively charged before being filled by the Fermi level, which effectively modifies the flatband voltage [9] per

$$V_{FB} = V_{FB,0} - \frac{Q_{it}(E_f)}{C_{ox}} \quad (15)$$

where $V_{FB,0}$ is the flatband voltage in the absence of interface states, Q_{it} is the signed interface charge quantity and E_f is the Fermi level in the channel. As a result, the effective V_{GS} that the channel "feels" tend to be higher when the net interface charge is positive (as is the case for the TCAD source data and the experimental TFET in [5], see Figure 2-6 (a)) and vice versa.

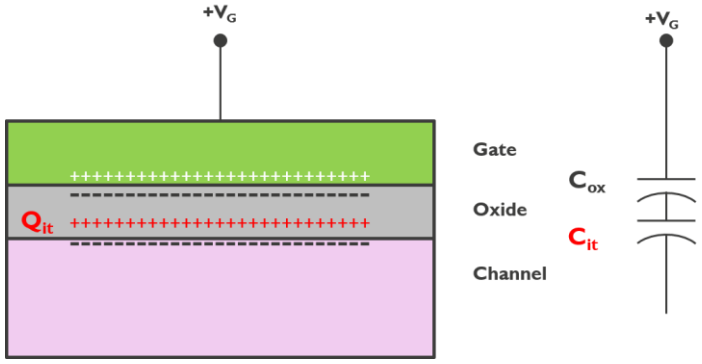

Figure 2-5: Schematic of the screening effect of the charged interface states. Q_{it} essentially creates a "body capacitor" C_{it} in series with C_{ox} and hence the voltage drop at the channel interface decreases.

On the other hand, the existence of electrically active interface states screens part of the gate charges (equivalent to a "body capacitor" C_{it} in series with gate capacitor C_{ox}, see Figure 2-5) and weakens the gate control of the surface potential in the channel and consequently the source-channel junction field. These two competing effects combine to produce a stretched-out Id-Vg profile at low gate bias where Q_{it} is still active, characterized by an apparent gate work function shift such that the Id-Vg curves move to lower V_{GS} values at the beginning, yet later on it goes away even before Q_{it} completely drops to zero owing to the fact that the voltage drop lost to C_{it} cannot be compensated by the "excessive" gate voltage contributed by Q_{it}, as illustrated in Figure 2-6 (b).

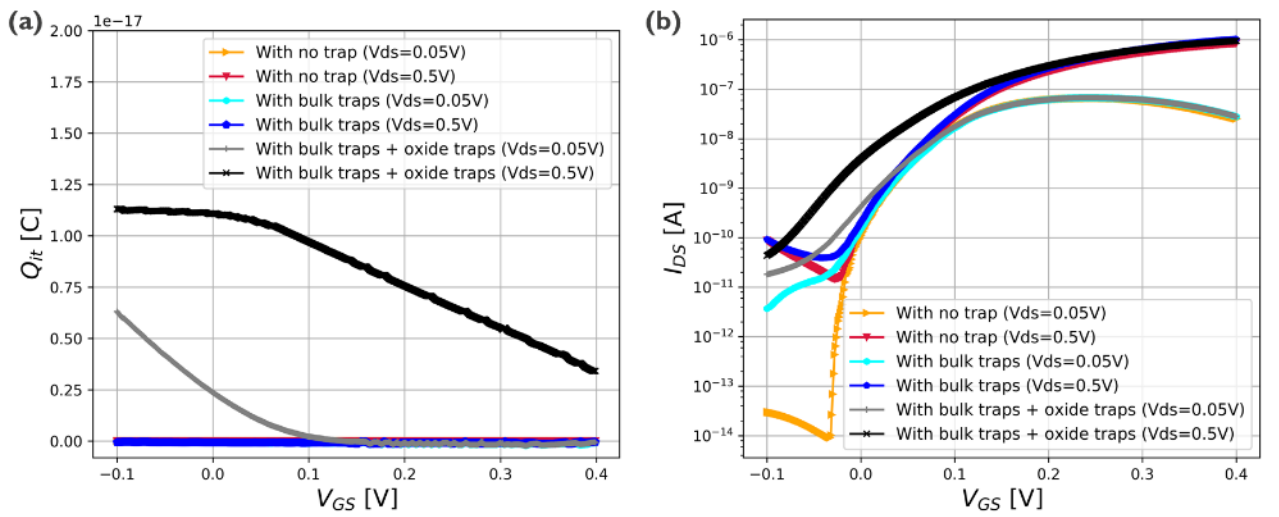

Figure 2-6: TCAD simulated (a) net amount of interface charge and (b) Id-Vg characteristics for one nanowire TFET described in [5]. Three different trap statuses are presented: turn off all traps ("with no trap"), turn on bulk traps only ("with bulk traps") and turn on both bulk traps and oxide traps ("with bulk traps + oxide traps"), each carried out at drain biases equaling 0.05 V and 0.5 V, respectively. Notably, the net amount of interface charge is essentially zero in the case of either "with no trap" or "with bulk traps", while "with bulk traps + oxide traps" sees a finite amount of positive charge owing to the donor-like nature of the "oxide traps". All simulations were assumed to have occurred at T = 300 K.

Therefore, to account for the electrostatic effect brought by the donor-like interface states, both equivalent body capacitor in Figure 2-5 and excessive gate charge in Figure 2-6 (a) have to be taken care of. Here imec proposed to introduce gate voltage modifications that link the Q_{it} to Id-Vg profile. Suppose $Q_{it}(V_{GS},V_{DS})$ is known from a look-up table that comes either from TCAD simulation or from capacitance measurement extraction, the effective V_{GS} owing to Q_{it} alone would appear as $V_{GS,eff}$ in the I-V model

$$V_{GS,eff} = V_{GS} + S_1 \frac{Q_{it}(V_{GS}, V_{DS})}{C_{ox}} \quad (16)$$

where S_1 is a constant scaling factor as a fitting parameter. Therefore, in the case where the Q_{it} is positive, the effective V_{GS} owing to Q_{it} alone would always be greater than the nominal value.

However, to bring in the effect of C_{it}, the voltage window opened between $V_{GS,eff}$ and V_{OFF} has to be reconsidered. For simplicity, imec chose to downscale all ($V_{GS,eff} - V_{OFF}$) used in BTBT model and TAT model by a second scaling factor S_2, i.e.,

$$I_{BTBT}(V_{GS} - V_{OFF}) \rightarrow I_{BTBT}\left(S_2 \cdot (V_{GS,eff} - V_{OFF})\right) \quad (17)$$

$$I_{TAT}(V_{GS} - V'_{OFF}) \rightarrow I_{TAT}\left(S_2 \cdot (V_{GS,eff} - V'_{OFF})\right) \quad (18)$$

where S_2 is subject to fitting to I-V data but should be smaller than unity. As Q_{it} is high at small V_{GS} and gradually drops to zero at higher gate bias, it is envisioned that the apparent I_{TAT} will appear much greater in subthreshold, whereas the constant scaling factor S_2 will eventually degrade the on-current at very high gate bias where Q_{it} vanishes and $V_{GS,eff}$ converges to plain V_{GS}.

While in the analyses above only the electrostatic effect of gate oxide traps is discussed, it is worth mentioning however that these traps also contribute the overall current via interface SRH generation. Nevertheless, as has been pointed out in [5] that observed leakage floor increase and SS degradation is dominated by bulk traps, implying that interface SRH generation would be eclipsed by the "apparent I_{TAT}" on Id-Vg curves in subthreshold. In this sense, the interface SRH generation brought by the interface states can be safely neglected in current calculation.

With these modifications, imec demonstrates the Id-Vg curves simulated with compact model in Figure 2-7. Here the device assumption again came from [5] but with both bulk traps and oxide traps switched on; Q_{it} data was extracted by comparing the terminal charge data in "all-trap" condition and "no-trap" condition and summarized as a look-up table (see 2.2.2 for more details). Indeed, the apparently shifted Id-Vg curves at small V_{GS} (< 0.2 V) reasonably coincide with what the compact model predicts (despite somewhat overestimated leakage floor at higher drain bias); at the same time, the on-current remains roughly unaffected up to V_{GS} = 0.4 V for both TCAD data and the compact model.

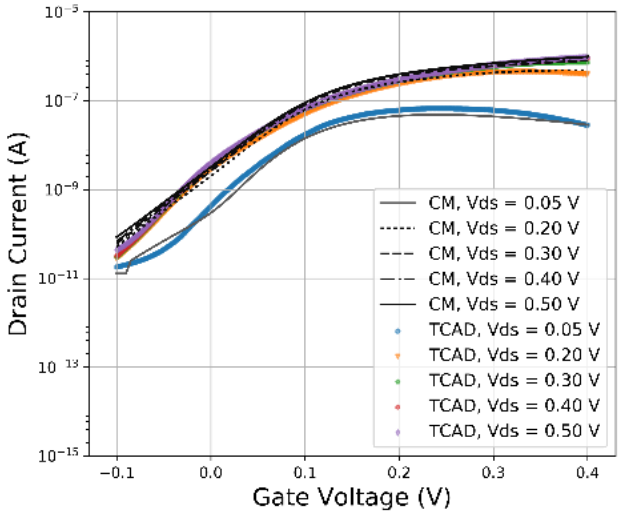

Figure 2-7: TCAD simulated (symbols, whereby both "bulk traps" and "oxide traps" were turned on) and calibrated compact model simulated (curves, denoted as "CM") Id-Vg characteristics for a single-nanowire TFET (T = 300 K).

2.2.2 Q-V model

Charge-based capacitance model was seen as essential to the maintain the charge conservation in all cases [7]. For the purpose of being compatible with the above I-V model in terms of genericity and versatility, imec decided to adopt a similar methodology in model development in [7] and largely adhered to the original model presented thereof, with a few adjustments made to fit in the TCAD-mimicked TFET in the project as well as to improve convergence.

In agreement with [7], imec aimed at an N-type TFET with high-doping P-type source and N-type drain and unintentionally doped channel without bringing in any electrically charged traps in the device; moreover, the mobile charges in the channel are attributed to the drain terminal, namely,

$$Q_S = ionized\ source\ dopants + source\ e^-(inverted) + source\ h^+(accumulated)\ (19)$$

$$Q_D = ionized\ drain\ dopants + drain\ e^-(accumulated) + drain\ h^+(inverted)$$
$$+ionized\ channel\ dopants + channel\ e^-(accumulated) + channel\ h^+(inverted)\ (20)$$

Therefore, in low V_{GS} limit, the source is in accumulation (through fringe capacitance and overlap capacitance if any) and the (channel + drain) is in inversion, thus the only capacitor that is in effect is the gate capacitor, which yields a linear dependence of Q_S and Q_D on V_{GS}; similarly, in high V_{GS} limit, the source is in inversion and the (channel + drain) is in accumulation which again gives rise to the linear dependence of Q_S and Q_D on V_{GS}. Within an intermediate V_{GS} range, the exact solutions of both Q_S and Q_D would rely on the very local surface potential dependence and require the integration over the entire terminal each, which leads to – both in [7] and consequently in imec model – a mathematical "stitching" of low V_{GS} and high V_{GS} parts that mimic the Q-V and C-V behaviors in that region.

Following [7], the drain terminal charge per TFET is expressed as

$$Q_D = \frac{W_{eff} L_D \kappa_{SiO2} \epsilon_0}{EOT}\left\{-E_D A_D\, ln\left[1 + exp\left(\frac{V_{GS} - B_D}{A_D}\right)\right] + C_D V_{GS} + D_D\right\}\ (21)$$

whereby W_{eff} is the effective width of the device as in I-V model; L_D is the length of the gate that covers the channel and the drain (i.e., gate-channel overlap + gate-drain overlap); κ_{SiO2} is the dielectric constant of SiO_2; EOT is the equivalent oxide thickness of the gate oxide; A_D, B_D, C_D, D_D, E_D are fitting parameters and each assumes a linear function of V_{DS}, namely

$$X_D = X_{D1} V_{DS} + X_{D2}, X = A, B, C, D, E\ (22)$$

As for the source charge, a similar expression exists as

$$Q_S = -\frac{W_{eff} L_S \kappa_{SiO2} \epsilon_0}{EOT}\{A_S\, ln[2 + tanh(B_S V_{GS} + C_S)] + D_S V_{GS} + E_S\}\ (23)$$

Whereby L_S is the gate-source overlap; A_S, B_S, C_S, D_S, E_S are fitting parameters as linear functions of V_{DS} similar to their counterparts in drain charge model, namely

$$X_S = X_{S1} V_{DS} + X_{S2}, X = A, B, C, D, E\ (24)$$

In low V_{GS} limit, Q_D and Q_S reduce to

$$Q_D = \frac{W_{eff} L_D \kappa_{SiO2} \epsilon_0}{EOT}\{C_D V_{GS} + D_D\}\ (25)$$

$$Q_S = -\frac{W_{eff} L_S \kappa_{SiO2} \epsilon_0}{EOT}\{D_S V_{GS} + E_S\}\ (26)$$

whereby the constant "2" in (23) instead of "1" in the original model in [7] allows for the convergence of the logarithm function in (23) converging to 0. From (25) and (26) it is clear that the drain and source capacitance become independent of V_{GS} as contemplated in the inversion (source)/accumulation (drain) assumption.

In high V_{GS} limit, Q_D and Q_S reduce to

$$Q_D = \frac{W_{eff} L_D \kappa_{SiO2} \epsilon_0}{EOT}\{(C_D - E_D) V_{GS} + E_D B_D + D_D\}\ (27)$$

$$Q_S = -\frac{W_{eff} L_S \kappa_{SiO2} \epsilon_0}{EOT}\{A_S\, ln(3) + D_S V_{GS} + E_S\}\ (28)$$

where the linear dependence of Q_D and Q_S on V_{GS} again dominates in accumulation (source)/inverison (drain).

Finally, the gate charge is derived by charge neutrality

$$Q_G = -(Q_D + Q_S)\ (29)$$

Figure 2-8 (a) illustrates the Qd-Vg and Qs-Vg characteristics obtained in circuit simulations with calibrated compact model (CM) plotted against TCAD simulation source data from ETHZ, with neither "bulk traps" nor "oxide traps" turned on. It can be seen that while Q_S remains largely unaffected by drain bias and keeps

getting more and more negative at a steady slope, the onset where Q_D starts to significantly accumulate more electrons can be offsetted to higher gate bias by increasing V_{DS}, below which the drain charge only slowly getting low in its algebric value. Note that the device assumptions per [5] stipulates a finite gate-source and gate-drain overlap in the model parameters, which is different than the original "test device" architectures (gate entirely sitting on the drain) presented in [7] for their model calibration, yet per Figure 2-8 (a) one clearly sees the good agreement between compact model and TCAD data at various drain biases over a large gate bias range. Moreover, the source, drain and gate capacitance comparison in Figure 2-8 (b) further confirms that the charge model is not only able to follow terminal charge itself but also to keep close track of its derivative with respect to gate voltage, the gate capacitance, which is more desirable for non-DC circuit simulations where good precision of capacitive components is indispensible.

Interestingly, the capacitance characteristics in Figure 2-8 (b) present a peculiar evolution trend with respect to gate voltage, i.e., the dominance of source capacitance and hence the non-monotonicity of gate capacitance, which is in sharp contrast to what is reported in [6] and [7] where the gate capacitance is dominated by monotonically increasing drain capacitance. This is understandable for the specific device architecture in [5] where the gate-source overlap is significant (~65 nm), which enables effective gate control of the source part but also inevitably adds to extra capacitance.

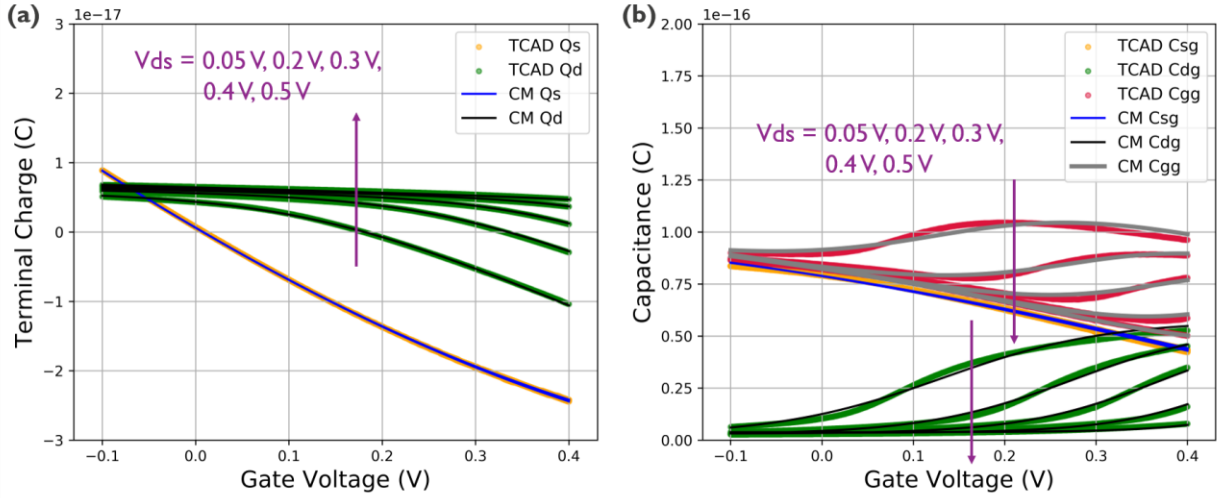

Figure 2-8: TCAD simulated (symbols, whereby all traps including "bulk traps" and "oxide traps" were switched off) and calibrated compact model simulated (curves, abbreviated as "CM") (a) terminal charge VS gate bias and (b) gate capacitance VS gate bias for a one nanowire TFET (T = 300 K).

Apart from the "intrinsic" charges that sit "inside" the TFET device, those that come from electrically charged traps in non-ideal scenarios should also be taken care of. Seeing that this "extrinsic" part of charges a highly specific to individual devices (either fabricated or TCAD-simulated) for imec considers them separately from the intrinsic part, and while the intrinsic part is assumed unchanged with respect to the scenario of ideal, no-trap case, the extrinsic part alone is obtained by subtracting from the entire charge quantity the intrinsic part and compiled as a look-up table. In other words, assume Q_D', Q_S' represent the drain and source charges in the trap-on case and Q_{D0}, Q_{S0} as their counterparts in the trap-off case, then

$$Q'_D(V_{GS,}V_{DS}) = Q_{D0}(V_{GS,}V_{DS}) + table(V_{GS,}V_{DS}, \Delta Q_D) \quad (30)$$

$$Q'_S(V_{GS,}V_{DS}) = Q_{S0}(V_{GS,}V_{DS}) + table(V_{GS,}V_{DS}, \Delta Q_S) \quad (31)$$

In this way, the intrinsic and extrinsic terminal charges can be separately extrapolated to desired bias range.

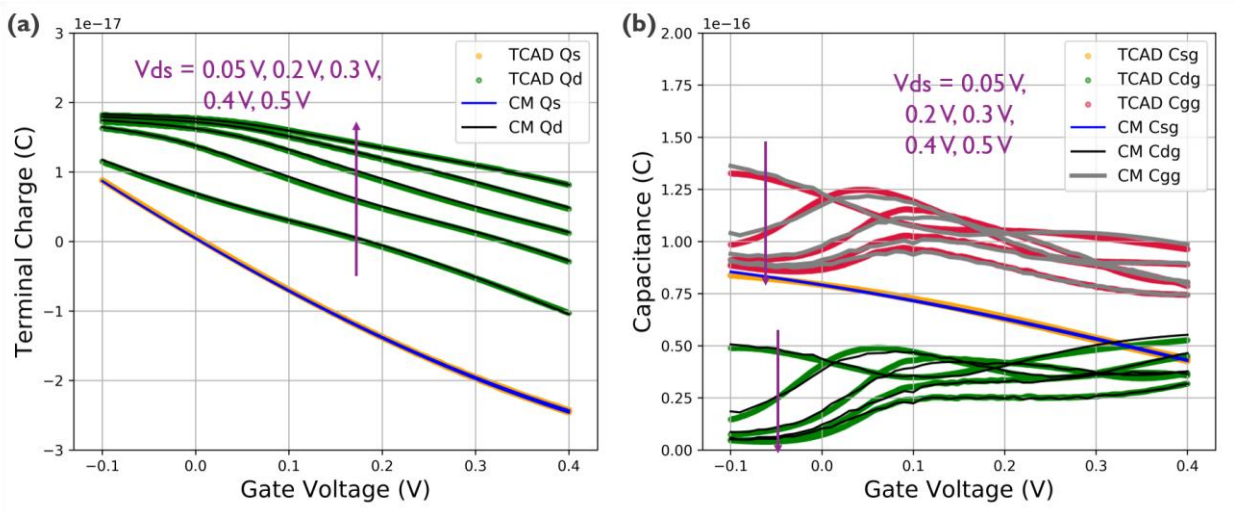

Figure 2-9 TCAD simulated (symbols, whereby all traps including "bulk traps" and "oxide traps" were turned on) and calibrated compact model simulated (curves, abbreviated as "CM") (a) terminal charge VS gate bias and (b) gate capacitance VS gate bias for a one nanowire TFET (T = 300 K). Compared to the previous figure, charges introduced by "oxide traps" are added to through a look-up table at different (V_{GS}, V_{DS}) combinations.

The calibration of trap-on counterparts to Figure 2-8 (a) is shown in Figure 2-9 (a). For this specific device, the "bulk traps" turned out to be electrically inactive thus not contributing to terminal charge quantities; the "oxide traps" in the gate-source-overlapped region also remain inactive per [5]. As a result, it is only the positively charged "oxide" traps that are contributing to drain terminal charge – which is exactly the Q_{it} discussed earlier in 2.2.1.3 – and give rise to considerable upward shift in Q_D compared to Figure 2-8 (a), while source terminal charge remains unaffected. These donor-like interface traps, energetically distributed in the bandgap of InAs channel (see Figure 2-10), carry positive charges at the gate/channel interface, the amount equaling the integration of trap density above Fermi level multiplied by elementary charge. As the gate bias increases, the channel Fermi level moves closer and closer to the E_C of the channel and the net amount of positive charge shrinks; on the other hand, increasing drain bias pulls channel Fermi level away from E_C, leaving more and more traps unfilled and hence charged, which in the end adds to more positive charges at the interface.

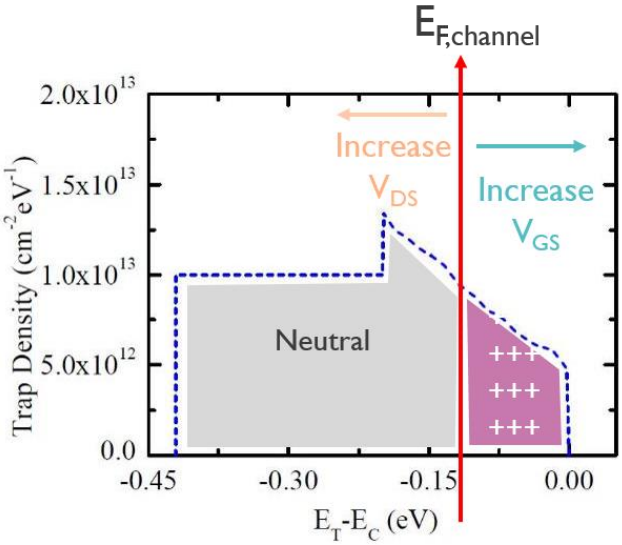

Figure 2-10: Schematic of energetic distribution of donor-like interface states at gate/channel interface in [5]. $E_{F,channel}$ denotes the channel Fermi level; (E_T – E_C) labels the trap level with respect to the channel conduction band edge E_C. In the figure the traps that are below channel Fermi level are filled therefore stay neutral, while those sit above Fermi level are positively charged. The net charge quantity contributed by the traps is the integration of trap density above $E_{F,channel}$ multiplied by elementary charge.

It is worth mentioning that the introduction of Q_{it} by "oxide traps" not only lead to the stretching effect of Id-Vg as discussed in 2.2.1.3, but also gives rise to more distortion in the gate capacitance. Compared to Figure 2-8 (b), both the drain and gate capacitance curves in Figure 2-9 (b) exhibit pronounced "bumps" at lower gate bias, instead of the original S-shaped curves that offset rightward with increasing V_{DS}. The increased capacitance that the TFET sees at lower V_{GS} – where the "sweet zone" of TFET is likely to be – also poses a potential detrimental effect to both switching speed and energy consumption in circuit operations.

3 Vertical TFET Parasitic Modelling

3.1 General scaling trends

Transition from one technological node to another has happened with ~0.7x scaling of contacted gate pitch (CGP) and metal pitch (MP), which both define the logic standard cells area. With an assumption that this scaling pace will continue, CGP will be about 42 nm at 7 nm technology and 32 nm at 5 nm technology (Figure 3-1). The 42 nm gate pitch is still sufficiently large for lateral devices, but at 32 nm gate pitch the S/D contacts as well as gate length are scaled so much, that the feasibility of lateral architecture is questionable. Thus, vertical devices may be introduced for further technology scaling at 5nm technology time, but this will unlikely happen before. Therefore, the developed vertical TFET model extension, which allows to compute parasitic device resistances and capacitances analytically, mainly targets the 5nm-like dimensions.

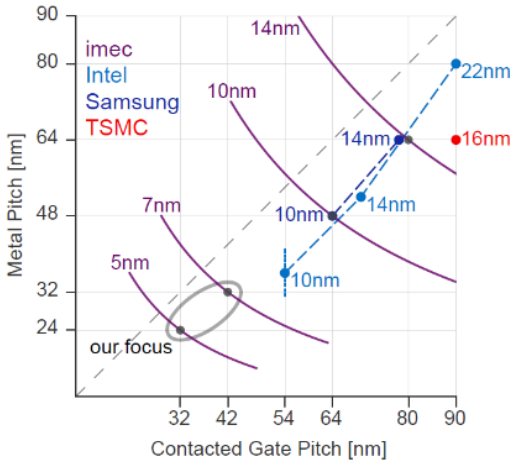

Figure 3-1: - Technological nodes having same name do not necessarily have the same ground rules. However, the transition from one node to another comes with roughly 0.5× scaling of MP and CGP product.

3.2 Process assumptions

The lithography assumptions go together with the design rules. To optimize manufacturing costs, it is needed to operate close to the cliff of a given patterning solution. These are the dimensions beyond which certain lithography techniques do not work (Figure 3-2). For example, TSMC 16nm technology uses MP of 64 nm: minimum which may be achieved with the double litho-etch patterning technique at the 193i lithography.

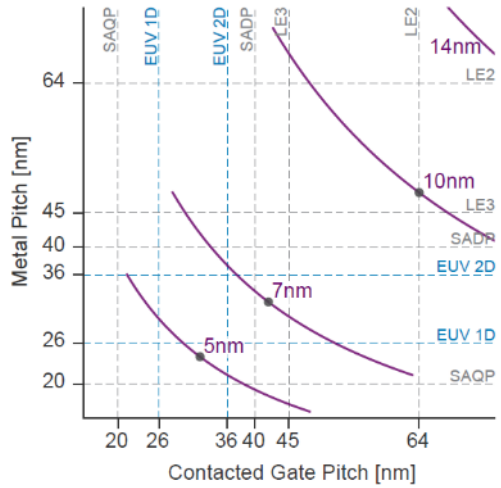

Figure 3-2: Various patterning cliffs should be taken into account when ground rules are being defined. Blue colours correspond to the single exposure limits of the EUV lithography. Grey colours are for the limits of various multi-patterning techniques in 193i lithography. Grey round markers indicate the nominal ground rules for imec technologies.

At 5nm technology, it would be possible to operate either at quadruple patterning cliff or at extreme ultraviolet 1D single exposure cliff. 1D means, that all the metal lines should be unidirectional. This has a direct impact on device layouts as well as on the material choice.

The 3D sketch of a vertical TFET device is shown in Figure 3-3. Parasitics model supports both nanowire and nanosheet shaped channels. The experimental data from the consortium comes from the nanowire based devices. Yet, for the target dimensions of the 5nm technology, nanowires would be problematic to use as they would have to be placed at very tight pitch which is challenging for both lithography and gate stack engineering. Transition towards a nanosheet would relax process complexity.

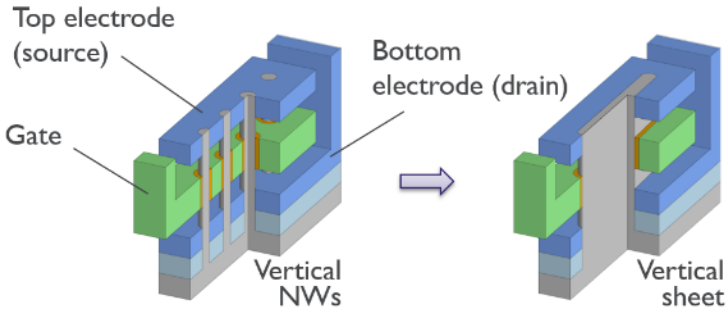

Figure 3-3: 3D sketch of a vertical device. Vertical TFET may be built with nanowires or nanosheets.

3.3 Parasitic resistances

Vertical devices are asymmetrical with a source resistance not being equal to a drain resistance. A contact to a bottom electrode needs to be done through a deep and narrow via, which translates into a highly resistive path (Figure 3-3). As a result, this asymmetry has to be taken into account in parasitics compact model to enable accurate performance estimation. Because of the small via size, the choice of metal material becomes critical. The baseline for our study is tungsten with thin liner and barrier on the sidewalls. The analytical tungsten resistivity model is calibrated to imec experimental data. Materials like cobalt or ruthenium may also be considered for metallic electrodes.

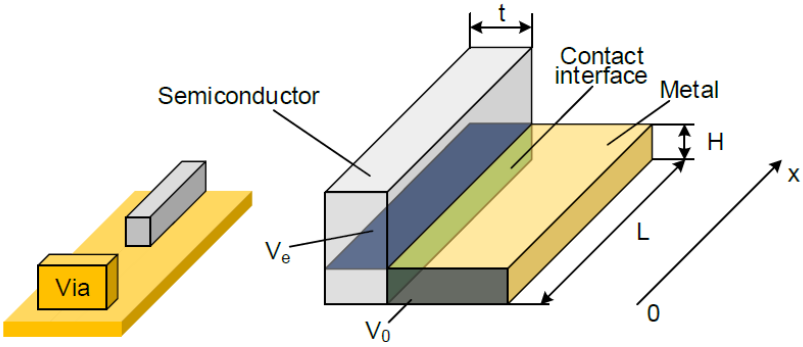

Figure 3-4: Left: the bottom electrode wrapping the elongated channel around has a via to the top placed by the short side of the channel. Right: the detailed schematics of the bottom electrode to the channel contact.

On top of the vertical via resistance, because of small dimensions, metal resistivity at the bottom horizontal electrode level should also be taken into account (Figure 3-4). Therefore, the model of contact resistance between bottom electrode and semiconductor was developed based on the transmission line model. This model accounts for metal resistance (which is typically neglected), metal-semiconductor interface resistance and semiconductor resistance, and handles all the spreading components correctly. The validity of the model is verified through the comparison with the finite element modelling computations (Figure 3-5).

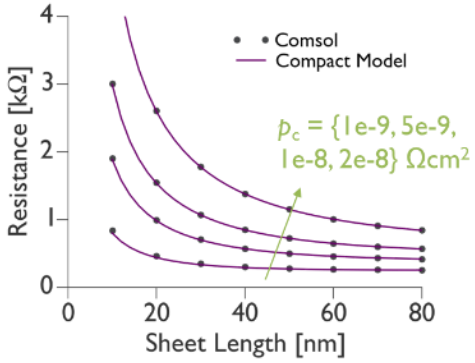

Figure 3-5 - Match of contact resistance calculations between analytical solution and finite element modelling (made with Comsol) is good for various specific contact resistivity values and contact lengths.

All the analytical equations needed for parasitic resistance calculations have been implemented in Verilog-A enabling accurate assessment with the compact models.

3.4 Parasitic capacitances

Parasitic capacitances of a vertical device differ from those of a lateral device. The key difference is due to the capacitances originating from the interconnects around the device, like top to bottom via (Figure 3-6).

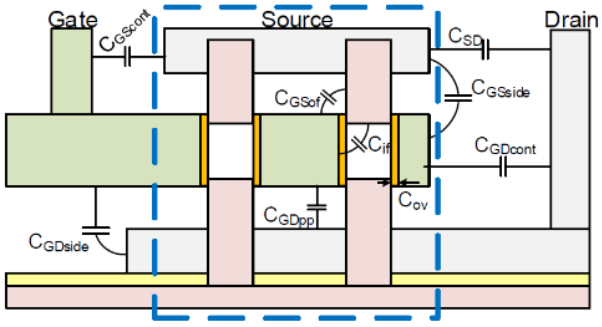

Figure 3-6: The cross-sectional view of a vertical device with the key parasitic capacitances. A lot of capacitances originate from the interconnects around the device.

All of the device capacitances may be expressed through a composition of basic capacitances like fringing or parallel plate capacitance. Modelling of these capacitances is based on the methodology from [10], which relies on the calculation of the elliptic integral modulus *k*. In order to compute *k* for various device geometries, these geometries should be conformally mapped to the $\Re$ axis of the complex plane. We perform this mapping with the holomorphic function $\cos(y\pi/t)$, where *y* is the complex coordinate in the original plane and *t* defines the width of the stripe in the original plane where capacitance should be computed. Essentially by using this function we decompose the VFET device into several strips, where capacitances are computed. This parasitic capacitance model supports various materials and was verified with the 3D TCAD for various geometries (different extension lengths, spacer thicknesses, etc.) as shown in Figure 3-7.

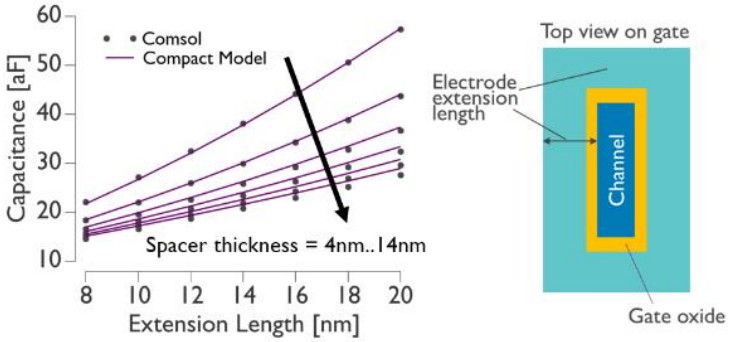

Figure 3-7: Total gate to source and gate to drain parasitic capacitances computed analytically match finite element modelling results for various geometries.

4 Combined Core and Parasitics Compact Model

In order to quantify the impact of parasitics on the device behaviors (both on DC level and on RO level), it is essential that different layers in a vertical TFET be designed with proper dimensions, which in turn requires careful consideration of process assumptions. For the purpose of being systematic with further benchmarking exercises, an inverter (INV) cell consisting of 6 NWs for PFET and NFET each with process technology comparable to foundry-equivalent 16 nm node (fN16) is used as the starting point, whereby the core P-TFET devices are assumed to be completely symmetric to N-TFETs before adding parasitics. The different layers of such a cell are indicated in Figure 4-1, inheriting from fN16 CGP = 90 nm, MP = 64 nm. More details in dimension design and justification is to be addressed in D6.3.

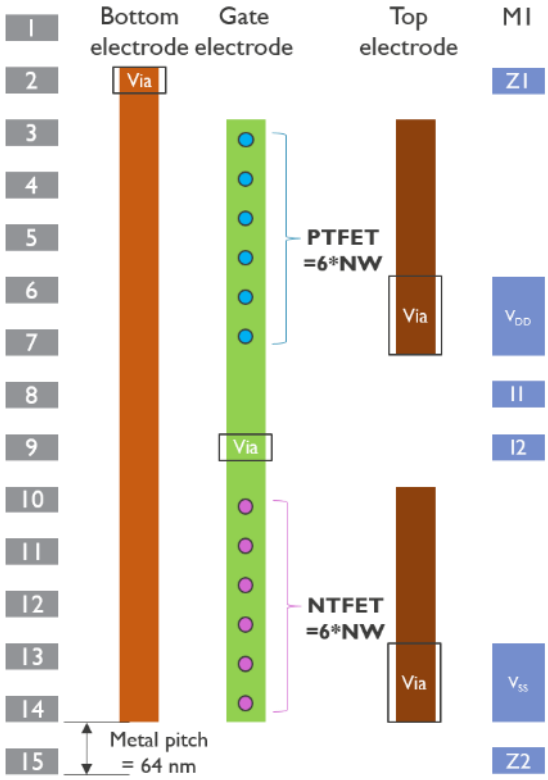

Figure 4-1: Layered view of the layout of an INV cell used for assessment of parasitics impact.

The underlying device assumptions herein are schematically drawn in Figure 4-2, which are essentially inherited from the assumptions in TCAD source data with the following modifications –

a. Simplification of source geometry: the 300-nm-long GaSb contacting segment with increased diameter in the original device was shortened to a high-doping contacting GaSb layer with a uniform diameter of 20 nm (intended for forming low contact resistivity with the top electrode).
b. Substitution of SiO_2 source spacer for the original organic counterpart for compatibility with general fabrication process.
c. Insertion of a high-doping InAs contacting layer to the bottom electrode for the same purpose as the source-contacting layer.

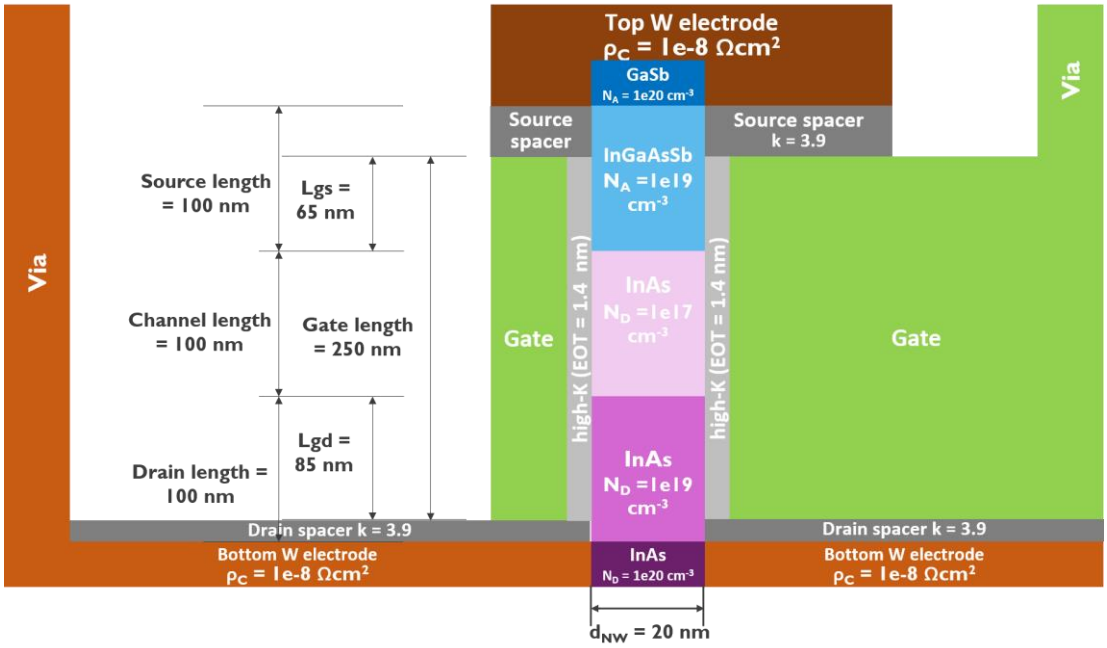

Figure 4-2: Schematic of 1 NW of the NTFET in the INV cell (in total 6 NWs), not drawn to scale; PTFETs are assumed to be symmetric to NTFETs.

Finally it should be pointed out that in exercises 4.1, 4.2 and 4.3 the core models will assume all the effects addressed in 2.2, meaning that the case in which all traps on including "bulk traps" and "oxide traps" is to be considered; and since core PTFETs are symmetric copies to core NTFETs, in DC/AC exercises (4.1, 4.2) it would suffice to characterize NTFETs only when it comes to the impact of parasitics.

4.1 Current degradation due to parasitic resistances

To assess the effect of parasitic resistances, DC simulation is carried out at Vdd = 0.45 V both with and without parasitics, with off current target (Ioff) set to 2 nA. The rationale behind such (Ioff, Vdd) combination is to pick relatively high numerical values of them within reasonable range such that the on-current Ion can be maximized, which in turn will render more pronounced voltage drop over parasitic resistance and thus more visible current degradation. The simulated results are plotted in Figure 4-3 as Id-Vd curves.

From Figure 4-3, it is found that the two curves representing with and without parasitic resistances largely overlap and the difference is too minor to be noticeable. In fact, if one looks at the on-current Ion and on-resistance Ron in each case, it is clear from Table 4-1 that Ion degrades only 0.24 % with parasitic resistances and compared to Ron, the source and drain parasitic resistances add up to merely 0.66 % of it. This is understandable from the following aspects:

a. The DC current so small that voltage drop on electrodes and semiconductor/metal interface is negligible.
b. The long contacting segment in the source part (300-nm GaSb) is simplified as a simple high doping contacting layer such that the extension resistance in source part is minimal.
c. The long source and drain segments (100 nm each) have been essentially included in the core model as in the source TCAD data to which the core model was calibrated[5], meaning that the extension resistances are now part of the channel resistance. Consequently, when calculating parasitic resistances, the long and relatively low-doping source and drain extensions were excluded to avoid double count, which also artificially underestimate the linear parasitic resistances existing in the device. However, as the DC de-biasing effect has been anyway reflected in the core model, the total Ron does not come with an error – it is only about the partitioning of channel resistance and parasitic resistance.

[5] In TCAD it was unrealistic to decouple the influence of the source/drain extension parts that only serve as resistors, therefore they were kept as part of the BTBT data.

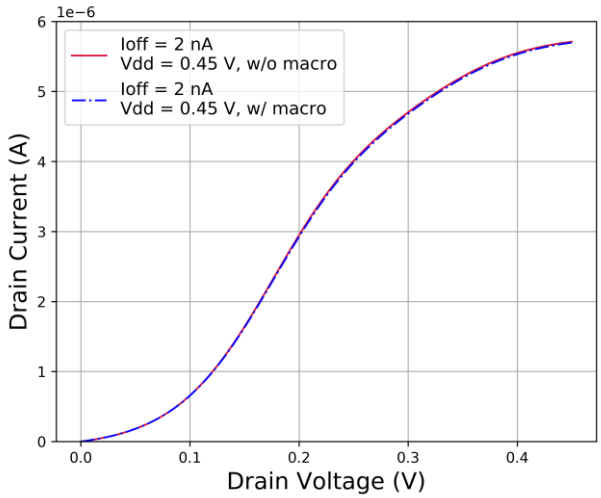

Figure 4-3: Simulated Id-Vd curves of the NTFET (6*NW) in the INV cell in Figure 4-1 at different Ioff target 2 nA at Vdd = 0.45 V. Here "w/ macro" indicates the results simulated with parasitics, while in results labelled "w/o macro" parasitic resistances are not considered

Table 4-1: Summary of on-current (Ion), on-resistance (Ron) and parasitic resistances for DC simulations in Figure 4-3. Ion is the current at Vgs = Vdd, Vd = Vdd; Ron is the nonlinear resistance derived by Vdd/Ion; Rs,tot and Rd,tot refers to the parasitic resistances in the source and drain part, respectively.

Parasitics	**OFF**	**ON**
I_{on} (µA)	5.7107	5.6969
R_{on} (kΩ)	78.8	79.0
$R_{S,tot}$ (kΩ)	0.229	
$R_{D,tot}$ (kΩ)	0.289	

4.2 Device capacitance increase due to parasitic capacitances

To estimate the capacitance increase that originates from parasitics, AC simulations with and without parasitics were conducted on the same NTFET device as in 4.1 with identical Ioff and Vdd.

Table 4-2 summarizes the major components of gate capacitances seen in a full "parasitic" picture. A quick calculation gives ~ (15 – 20) % contribution of (Cgs,tot + Cgd,tot) compared to the intrinsic gate capacitance (the gate capacitance without parasitics), depending on the bias point of the gate. Although in the table only two Vg values are counted (Vg = 0 for Cgg,off, Vg = Vdd for Cgg,on), the relatively large distance in bias point ensures that they are representative capacitance values in the whole sweeping range of Vg; plus, it is obvious from **Figure 2-9** (b) that at fixed drain bias, Cgg varies no more than a factor of 2 within a large gate bias for one NW, therefore for a device consisting of six NWs here it is reasonable to expect that the relative change in Cgg during a Vg sweep would not deviate significantly and that the way to look at Cgg,off and Cgg,on would be safe to assess the overall magnitude of gate capacitance of a device during its operation.

It has to be reminded that compared to the "real" device presented in [5], it is possible that the contribution of Cgs,tot in the parasitics deviate from the original scenario, seeing that the device architecture assumptions are adopted as mentioned previously. However, as the shortening of source contact is in some sense counterbalanced by the higher k values of SiO_X, it is expected that the relative weight of Cgs,tot with respect to intrinsic gate capacitance would remain close to what has been simulated with the compact model, thus leading to a reasonably reliable assessment of circuit-level behaviors.

Table 4-2: Summary of on-capacitance (Cgg,on), off-capacitance (Cgg,off) and parasitic resistances for AC simulations. Cgg,on is the gate capacitance at Vgs = Vdd, Vd = 0; Cgg,off is the gate capacitance at Vgs = 0, Vd = 0; Cgs,tot and Cgd,tot refers to the parasitic capacitances seen by the gate in the source and drain part, respectively; Cpara gives the sum of Cgs,tot and Cgd,tot; Cggi,off and Cggi,on are simply the Cgg,off and Cgg,on without parasitics

Parasitics	**OFF**	**ON**
$C_{gg,off}$ (aF)	817	939
$C_{gg,on}$ (aF)	607	729
$C_{gs,tot}$ (aF)	52.8	
$C_{gd,tot}$ (aF)	68.9	
$C_{para}/C_{ggi,off}$ (%)	14.9	
$C_{para}/C_{ggi,on}$ (%)	20.0	

4.3 Impact of parasitics on the ring oscillator performance

The characterization of parasitics impact on a circuit level connects INV cells into a loop to form a ring oscillator (RO). For a quick assessment of the shift in a few metrics (frequency, switching energy, etc.) in the presence of parasitics it suffices to run the transient simulations on a simple 15-stage FO1 RO (RO15) with zero back-end-of-line (BEOL) load, as shown in Figure 4-4.

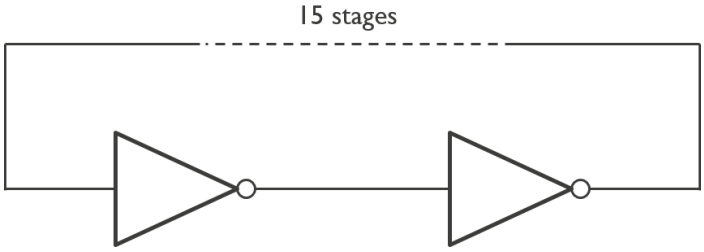

Figure 4-4: Schematic of the 15-stage RO testbench.

Figure 4-5 demonstrates the switching energy versus frequency in transient analyses on RO15 with and without parasitics, where Ioff targets are set to either 200 pA (typical for standard-V_{TH} applications) or 2 nA (typical for low-V_{TH} applications) and Vdd is swept from 0.15 V to 0.45 V. It is observed that parasitics have indeed given rise to pronounced degradation in terms of both switching energy and speed, with a maximum of 6.19X iso-energy frequency drop (for Ioff = 200 pA) and 1.74X iso-frequency energy increase (for Ioff = 2 nA).

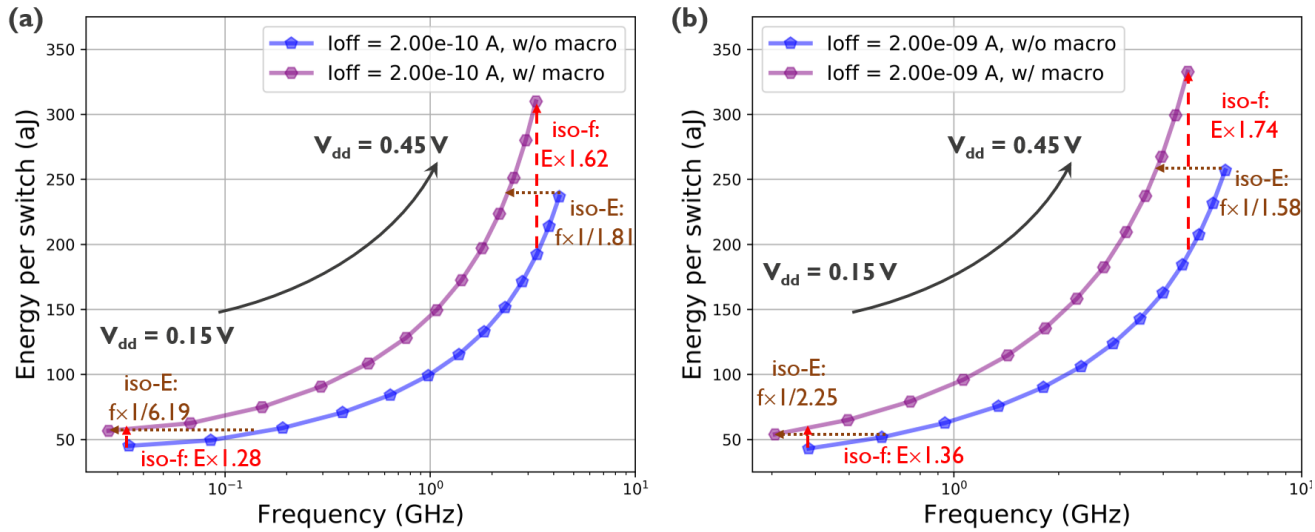

Figure 4-5: Comparison of the energy-frequency sweep results for 15-stage RO with (purple, labelled "w/ macro") and without (blue, labelled "w/o macro") parasitics: (a) Ioff = 200 pA and (b) Ioff = 2 nA. Vdd sweep range is [0.15 V, 0.45 V] at a step of 0.25 V. With the introduction of parasitics, a maximum of 1.62X and 1.74X of iso-frequency energy increase is observed for Ioff = 200 pA and 2 nA, respectively, and maximum iso-energy frequency degradation is up to 6.19X and 2.25X, respectively.

Table 4-3 lists the RO level performance degradation at a few Vdd points that were swept, where the definition of Ieff and Ceff follows $I_{eff} = f \times Energy/V_{dd}$ and $C_{eff} = Energy/V_{dd}^2$, respectively. As shown in the table, while the Ieff drop is rather slight due to negligible current degradation as discussed in 4.1, the percentage of Ceff growth is quite remarkable (from ~ 25 % up to > 30 %) which is more drastic than the ΔCgg% seen in AC simulations in 4.2 (~ (15 – 20) %), reflecting the Miller effect which multiplies the drain capacitance in an inverter.

Table 4-3: Summary of performance degradation after adding parasitics on a 15-stage FO1 RO, including frequency drop (Δf %), switching energy increase (ΔE %), effective current drop (ΔIeff %) and effective capacitance increase (ΔCeff %).

Vdd (V)	**0.15**		**0.30**		**0.45**	
	I_{off} = 200 pA	I_{off} = 2 nA	I_{off} = 200 pA	I_{off} = 2 nA	I_{off} = 200 pA	I_{off} = 2 nA
Δf %	-20.5 %	-20.0 %	-22.2 %	-21.4 %	-23.0 %	-22.0 %
ΔE %	+25.8 %	+25.5 %	+29.6 %	+28.0 %	+31.0 %	+29.5 %
ΔI_{eff} %	-0.03 %	-0.33 %	-0.80 %	-0.59 %	-0.79 %	-0.96 %
ΔC_{eff} %	+25.8 %	+25.5 %	+29.6 %	+28.0 %	+31.0 %	+29.5 %

5 Conclusions

In this deliverable we discuss the challenges related to TFET compact modelling on various levels: core transport, trap-assisted tunneling, RC parasitics.

Analytical compact models for Silicon and III-V devices are implemented in Verilog-A and are suitable for SPICE simulations, showing good convergence and run-time expected from compact models.

The RC parasitics model for the vertical devices is developed in the context of scaled logic. Yet, being parametrized and scalable, it is used at 16nm-like dimensions. It is shown that because of small currents from TFET, parasitic access resistance has little impact on performance, while parasitic capacitance degrades the performance significantly (as there is lack of current to drive these parasitic capacitances).

Decoupling of intrinsic device performance from traps influenced one in the compact models allows to further assess the potential of TFETs for digital applications.

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