E2SWITCH
Energy Efficient Tunnel FET Switches and Circuits

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E²SWITCH

Energy Efficient Tunnel FET Switches and Circuits

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Simulation-based investigation of the effect of dimensionality in DOS TFET with the selection of the best device candidates.

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[1] R = Report, P = Prototype, D = Demonstrator, O = Other

[2] PU = Public, PP = Restricted to other programme participants (including the Commission Services, RE = Restricted to a group specified by the consortium (including the Commission Services), CO = Confidential, only for the members of the consortium (including the Commission Services)

[3] Measured in months from the project start date (M01)

Revision history

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0.1	07-10-2015	Cem Alper	First draft
0.2	10-11-2015	Cem Alper	Revisions
1.0	18-11-2015	Adrian Ionescu, Kirsten Leufgen	Final version, approved by the coordinator

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Contents

Summary

This report compiles the simulation data obtained so far within the project and classifies each studied device with a dimensionality. Inspired by the benchmarking efforts by IBM in WP6, a general benchmarking framework is given in the first section to put the simulated devices in comparison against published experimental data.

In sections 2 and 3, various dimensionality cases are compared to one another to search for possible beneficial characteristics for a given dimensionality case. The simulations are performed with various different techniques (EMA, EMA-NP, k.p, atomistic) already described in the previous deliverables, except a new modified version of the EMA code described in the appendix of this document, which emulates quantization along the transverse direction.

1 Benchmarking Different TFET Architectures Using Experimetal Data and Simulations from Previous Deliverables

The first part of this report aims to benchmark the aggressively scaled TFETs studied by simulation in WP3 and WP4 against published experimental data to assess what is the gap between what can be fabricated and the best devices identified by simulation. We follow the approach proposed by IBM in WP6: we plot the subthreshold slope averaged over 3 decades SS_{3dec} versus the ON current normalized to V_{DS}. For the simulation data, we will denote the dimensionality of the carrier gases involved in the band-to-band tunneling (BTBT) process to pinpoint any trends that depend on the dimensionality of gases.

1.1 Simulated Devices from D3.3 vs. Experiments

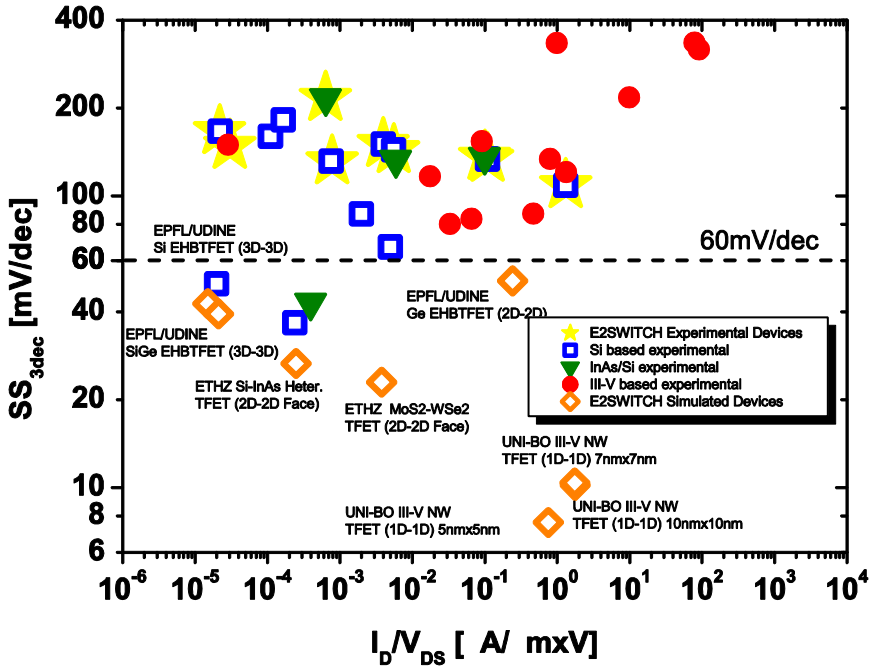


Figure 1: Benchmarking comparison plot of experimental data collected by Moselund *et al.*for WP6 activities. The additional orange points are the ones simulated by WP3 partners and reported in D3.3 in sections 2-4.

As from the DoW, in D3.3 we have identified the most promising TFET architectures. The performance of these devices is plotted in Fig. 1 along with the experimental data compiled by Moselund *et al.* As stated before, we denote for each point the carrier gas dimensionalities in parentheses.

The SS and I_{ON} extraction procedure for the simulated devices is as follows: whenever available, I_{OFF} is defined as the minimum current given in the data-set, typically the ambipolarity change point where the device switches from n-type to p-type (or vice versa). Then ON current is set as $I_{ON} = 1000 I_{OFF}$ @ $I_D(V_{ON})$. Then, the SS is calculated as $SS = 1000 \frac{V_{ON}-V_{OFF}}{\log_{10}(\frac{I_{ON}}{I_{OFF}})}$. This is not possible for the EHBTFET data-sets since they are obtained using a 1-D model which sets I=0 below the alignment voltage. The extraction procedure for those points is described in the following section.

It is seen that all the devices picked-up from D3.3 perform in the 'sub-thermal' region, meaning that their $SS_{3dec} < 60mV/dec$. The $2D-2D_{face}$ devices (described in D4.1, D4.3 and D3.3) simulated by ETH and EPFL/UDINE seem to sit on the $SS_{3dec} = 20-40mV/dec$ range, whereas the nanowire devices simulated by IUNET-BO (reported in D3.3) seem to offer slightly higher current levels with steeper switching. A trade-off between the ON current and the SS is observed for the nanowires with changing nanowire cross section: compared to 7nm×7nm, the 5nm×5nm nanowire offers better SS but lower ON current. Note that the nanowires are normalized with respect to the square cross-section edge.

1.2 Electron-Hole-Bilayer-TFET: 1D vs 2D Models

In this subsection, we compare (considering again the SS vs. I_D/V_{DS} plot) all the Electron Hole Bilayer TFET (EHBTFET, see Fig.2) simulation data from different partners. The aim is to compare different materials and different simulation techniques. In particular, here 1D and 2D denote the real-space, not the gas dimensionality, i.e. 1D simulations consider only one device section in the overlap region, assuming that the potential profile does not change along the channel in the overlap region; 2D simulations instead account for the potential variation along the channel direction. It should be noted that what we call "1-D simulations" in Fig. 3 impose a constraint of $V_{n-gate} - V_{p-gate} = 2V$, whereas no such limitations are present for other data points. This constraint assumes utilization of midgap gate metal workfunctions and can be lowered by utilizing lower and higher workfunction metals in the n and p gate, respectively. Note that anti-crossing that causes a drastic asymmetry between the real and imaginary branches of the heavy hole subbands [1] is neglected in the 2D simulations of InGaAs. 1-D simulations show that neglecting anti-crossing should result in the underestimation of the ON current by about one order of magnitude [1].

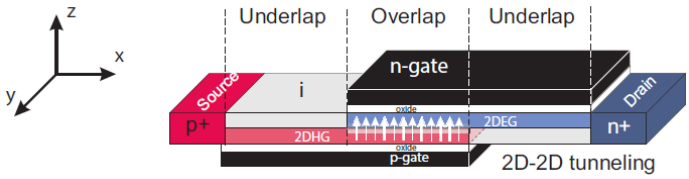


Figure 2: Electron Hole Bilayer TFET device structure.

Since 1-D models cannot predict the OFF state lateral leakage current of the EHBTFET, a special treatment for them is necessary. We employ the following method: The ON current is extracted as $I_{ON} = I_d(V_{align} + \frac{2}{3}V_{DD})$. The OFF state current is taken at $I_{OFF} = \frac{I_{ON}}{1000} = I_d(V_{OFF})$, which is typically very close to V_{align}. SS is calculated using the formula in the previous section. A sample I-V curve depicting the extraction procedure is given in Fig. 4(left).

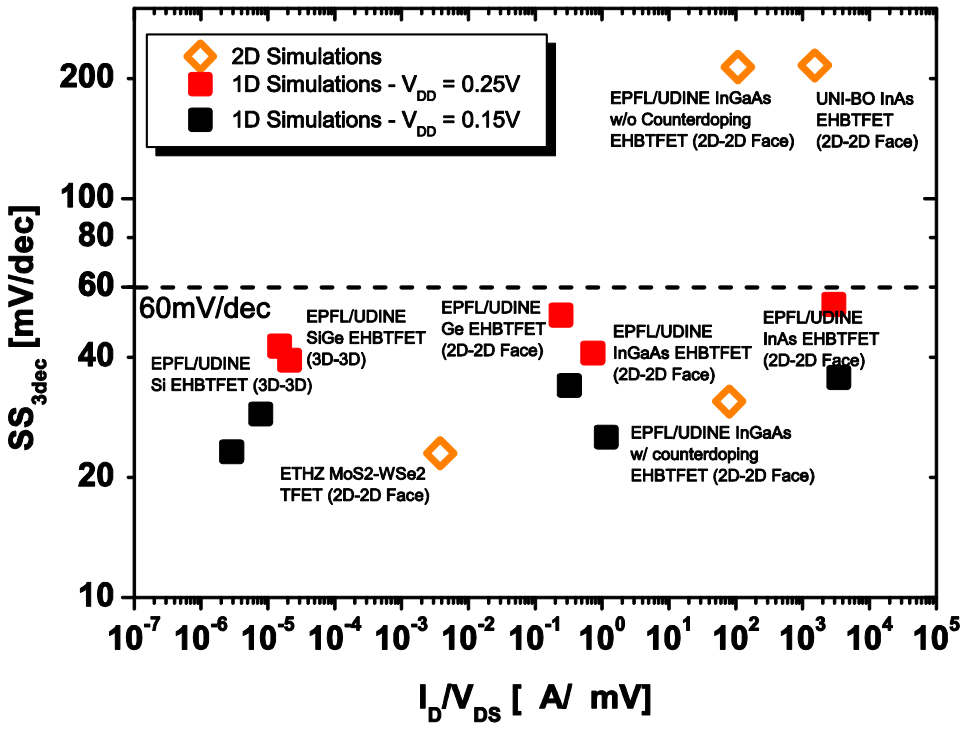


Figure 3: Comparison of EHBTFET simulation data compiled from different partners.

In Fig. 3, we have labeled some of the 1-D EHBTFET simulations as "3D-3D" whereas some are labeled "2D-2D", each corresponding to the carrier dimensionality observed in the devices. As discussed in D4.3,

2D-2D tunneling behavior is observed in III-V or Ge based EHBTFETs, whereas the large masses of Si and SiGe result in 3D-3D tunneling. We note that both 2D-2D and 3D-3D tunneling cases are below 60mV/dec, except the 2D-simulated EHBTFETs, which show poor SS behavior due to lateral leakage mentioned in the previous deliverables. Optimization strategies that suppress this leakage current have been proposed in D4.3 and also will be mentioned in the following sections. The main reason for the relatively poorer performance of the high supply voltage cases is the saturation behavior of the 2D-2D tunneling devices, as will be further investigated in section 2.4.

The low SS is obtained by all the modeling approaches, except the discrepancy between SS predicted by the 1D EMA-NP results and the 2D k.p results of UNI-BO for InAs EHBTFET as well as the difference between 1D and 2D EMA+NP simulations for the InGaAs one w/o counterdoping. This is caused by the fact that 1D simulations ignore the lateral leakage. We remind once more (see also D4.3) that lateral leakage can be very effectively suppressed using counterdoping as seen below in Fig 3 (right).

A detailed comparison between 1D and 2D simulations using the EMA model from EPFL/Udine is reported in Fig. 4(right) and reveals that a general agreement exists between the two simulation approaches when counterdoping is used. As expected, the 1D simulator cannot detect the finite slope of the Id(Vgs) below the alignment voltage that is caused by the lateral leakage. In addition, a slight discrepancy of the alignment voltage is seen due to the fact that non-parabolicity corrections could not be taken into account for 2D simulator. NP corrections typically alleviate the strength of quantization [2], therefore it is expected to have earlier onset of tunneling when NP corrections are included (compare 1D with parabolic model, black, and with non-parabolic correction, red). Without counterdoping, instead, the lateral leakage is so strong that 1D and 2D simulations largely differ. In the figure, we also show the impact of anti-crossing [1] that has been included in the 1D model but is not easily extendable to the 2D one.

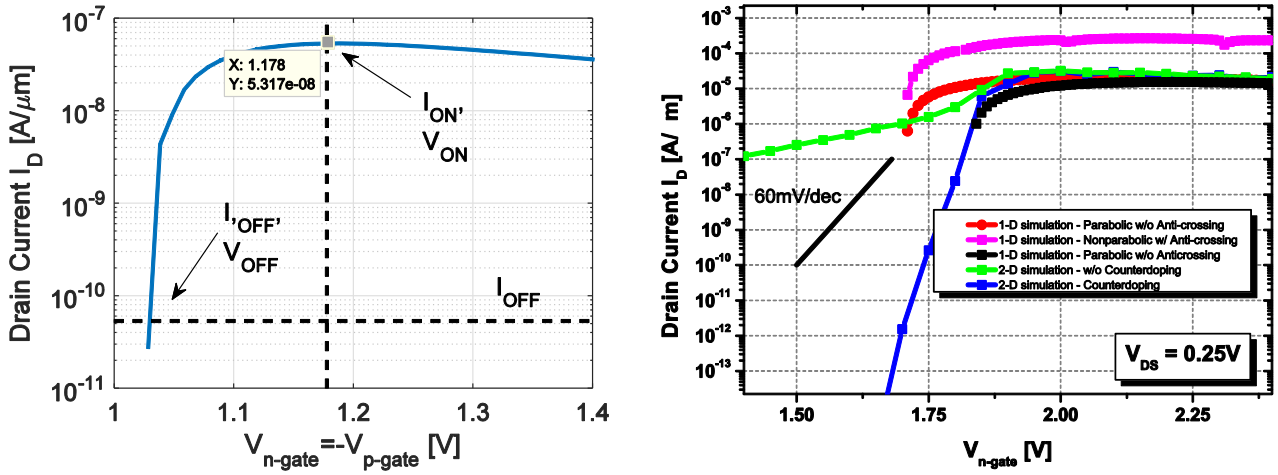


Figure 4: (Left) I_{OFF} extrapolation scheme for 1D simulations for $V_{DD} = 0.25V$. The dashed curve indicates extrapolated I-V regions. (Right) Transfer characteristics for an $In_{0.53}Ga_{0.47}As$ EHBTFET with and without counterdoping [3]. The 2D model is parabolic w/o anticrossing. Different options are shown for the 1D model.

2 Impact of Carrier Gas Dimensionality

In this section we systematically analyze situations involving tunneling from electron and hole gases with different dimensionality. The general classification of the different combinations follows [4]. For convenience explanatory sketches that denote each dimensionality cases are given in Fig. 5.

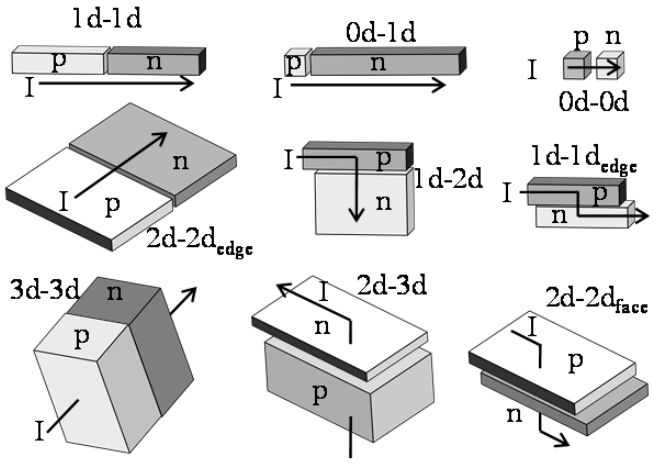


Figure 5: Sketch of the possible dimensionality cases for tunneling between carrier gases [4]. Note that not all the cases given in the figure are considered in this report.

The characteristics of the device depend not only on the dimensionality of the gases, but also on how the electron and hole gases get aligned. Face tunneling indicates that BTBT occurs along the faces where the two gases overlap along a large area, whereas edge tunneling occurs when the electron and hole gases are aligned over their edges so BTBT occurs at a small concentrated region.

2.1 EHBTFET: 2D-2D Face vs 2D-2D Edge Tunneling

The first situation we consider is 2D-2D tunneling. We first aim to compare 2D-2D face and 2D-2D edge tunneling. The 2D EMA simulator developed by EPFL/Udine allows us to study this aspect considering an InGaAs EHBTFET (2D-2D face tunneling) and an InGaAs Ultra Thin Body TFET (UTBTFET, 2D-2D edge tunneling). For a fair comparison, we use the same channel and oxide thicknesses for both devices. We utilize the counterdoping technique explained in D4.3 to suppress the lateral leakage in the EHBTFET.

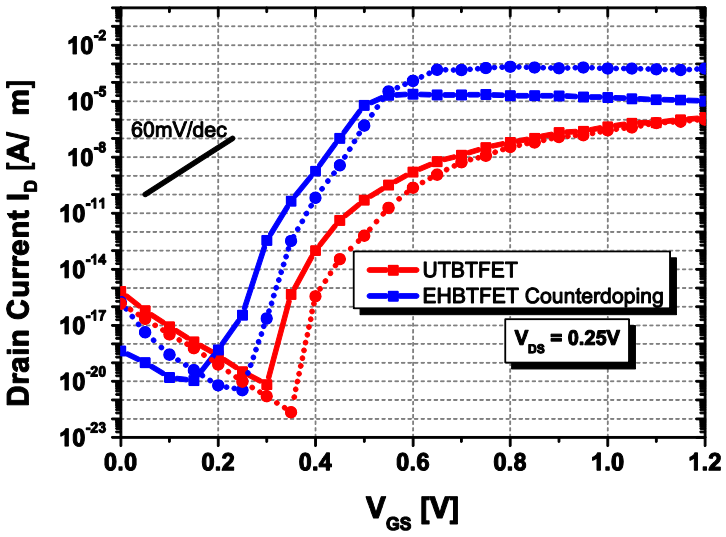


Figure 6: Transfer characteristics comparison for (red) UTBTFET and (blue) EHBTFET with $In_{0.53}Ga_{0.47}As$ channel. Note that the EHBTFET curves are shifted rigidly along the x-axis for ease of viewing together with the UTBTFET results. (Solid) $T_{CH} = 10nm$ (Dotted) $T_{CH} = 7.5nm$. EOT=1nm S/D doping=$1\times10^{20}cm^{-3}$.

In the Fig. 6 we see that using the same EOT=1nm and the same channel configuration (i.e. thickness and material), significantly higher current levels and steeper switching slopes can be obtained with 2D-2D face tunneling. This signals that, *once isolated from parasitic effects,* utilizing 2D-2D face tunneling could be a viable ON current booster. Another interesting contrast between the 2D-2D face and 2D-2D edge tunneling is that the channel thickness essentially has no impact on the maximum obtainable current for 2D-2D edge tunneling, as the $T_{CH} = 7.5\text{nm}$ and $T_{CH} = 10\text{nm}$ cases converge to the same current value at high V_{GS}.

We also note an important contrast between edge-tunneling and face-tunneling devices. Face tunneling devices tend to exhibit a saturation behavior due to the fact that quantization occurs along the direction that is transverse to the direction that carriers enter into the device. This result alters the relationship between the electrostatics and the DOS involved in tunneling. A monotonous increase with increasing gate voltage is typically seen for edge tunneling devices, where the carrier injection direction from the source (drain) is aligned with the tunneling direction.

2.2 EHBTFET: 2D-2D Face vs 1D-1D Face Tunneling

It should be noted that the dimensionality effects are inherently intertwined with electrostatic effects in TFETs. To put on clear terms, let us give an example case of a bulk TFET and a nanowire one. It is of course expected that the nanowire TFET outperforms the bulk one. However, it is not at all obvious what portion of this improvement comes from the electrostatic improvement. The electrostatic control of the nanowire TFET is much better than the bulk one so it is expected that a significant portion of the performance improvement should result from it. It is however an open question whether the reduction in the carrier dimensionality (3D gas in bulk vs 1D gas in nanowire) is also beneficial for the BTBT current.

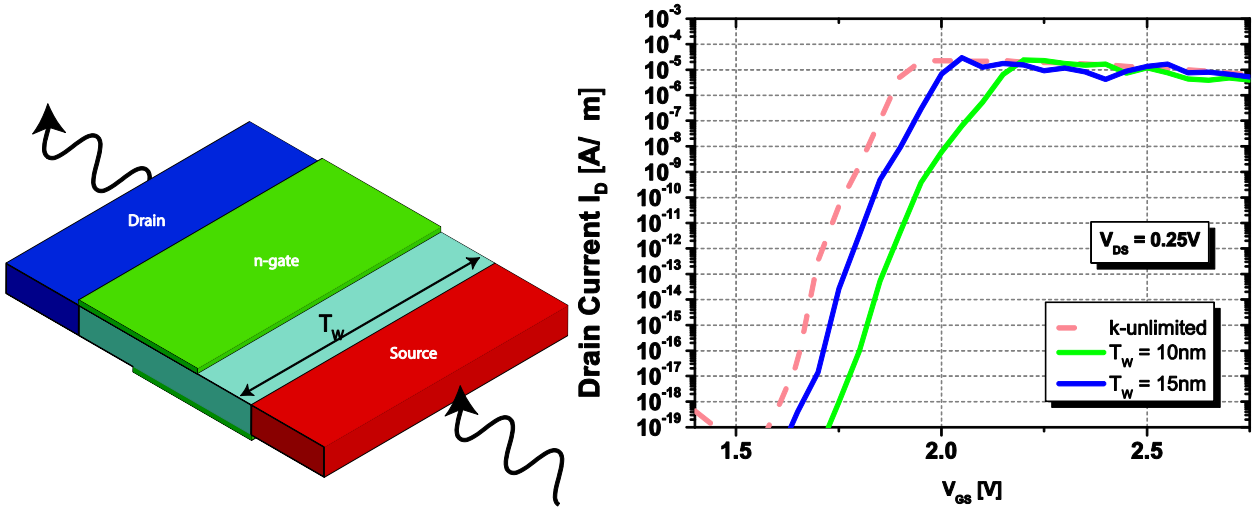


Figure 7: (Left) The device structure with transverse direction thickness T_W indicated (Right) Transfer characteristics for InGaAs EHBTFET with counterdoping for varying transverse thicknesses T_W.

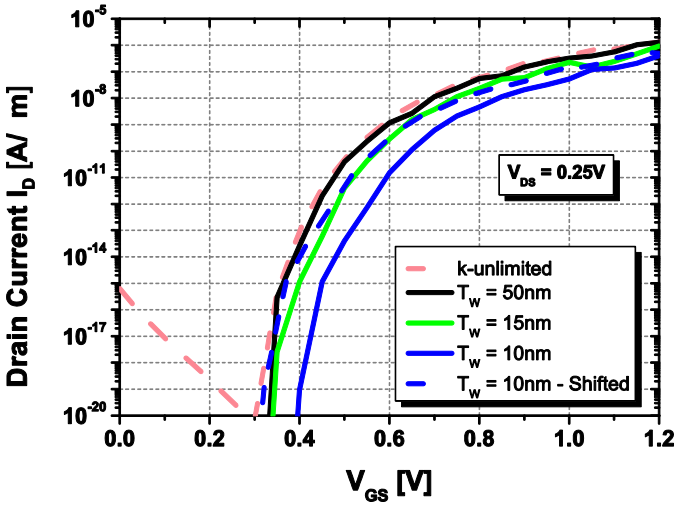
To this end, we have developed a method that isolates the impact of the carrier gas dimensionality effects from the electrostatics. The method is based on modifications to the EMA code developed by EPFL/Udine (described in D4.1, D4.2 and D4.3) to limit the transverse length of the device along one direction w/o modifying the electrostatics. The modifications actually consists of: i) shifting the band edges rigidly to account for the size-induced quantization along the transverse direction, ii) to alter the density of states (DOS) from 2-D to 1-D k-space. We are simply using the same electrostatic potential profiles calculated from the original EMA code, and run the k-limited code as post processing.

We use such simulator to compare 2D-2D and 1D-1D face tunneling cases. We consider an InGaAs EHBTFET with counterdoping to study the impact of limiting the k states. We simulate the cases with different transverse thicknesses T_W in Fig. 7. The first observation is the shift of the onset voltage, which is expected, due to increased band gap associated to size-induced quantization along the transverse direction. Most strikingly, it is seen that the ON current density and the slopes are similar, which signals that no visible benefit is gained as the carrier dimensionality switches from 2D to 1D. The slight degradation of the slope for the $T_W = 10\text{nm}$ case is caused by the formation of inversion layers in the overlap regions at high gate voltages. Since we do not include the transverse quantization while calculating the potential profile, we are

essentially neglecting the related quantum capacitance effects that are induced by the electron concentration inside the channel region.

2.3 2D-2D Edge vs 1D-1D Edge Tunneling

Another aspect that can be investigated using the modified EMA code is comparing 2D-2D and 1D-1D edge tunneling. To this end, we simulate and compare an InGaAs UTBTFET with and without transverse k-space limitation. Different transverse thicknesses are considered in Fig. 8.



Thickness	SS_{5dec} [mV/dec]
k-unlimited	58
$T_W = 10nm$	60
$T_W = 15nm$	56
$T_W = 50nm$	53

Figure 8: (Left) Transfer characteristics for the InGaAs UTBTFET for different transverse thicknesses T_W. (Right) Corresponding SS extracted over 5 decades.

In contrast to the face tunneling case, switching from 2D-2D edge to 1D-1D edge tunneling results in more evident changes in the transfer characteristics. Similar to the previous case, a shift of tunneling onset is seen as the transverse thickness is decreased as seen in Fig. 8. Moreover, differently from face tunneling, a reduction of the ON current and switching slope is observed in edge tunneling as seen clearly from the shifted $T_W = 10nm$ curve (blue, dashed). Another interesting feature in the 1D-1D tunneling scenarios is the suppression of the so-called ambipolar region (V_{GS}<0.3V in Fig. 8). The main reason for that is the suppression of the BTBT current that is caused by light hole tunneling. Light holes have much smaller effective masses compared to the heavy holes, therefore the transverse quantization pushes their subbands to so low energy to contribute to the current. So, a desirable side effect of the transverse quantization is the suppression of the unwanted ambipolar behavior.

The extracted SS values are also reported in the table above. We note a slight degradation of SS with decreasing T_W, which is also in line with the degradation of I_{ON}.

2.4 2D-2D Face Tunneling vs 3D-3D Face Tunneling

2.4.1 EHBTFET Simulations

As discussed in D4.3 and as seen in Fig. 3, in the EHBTFET we can have situations of 2D-2D tunneling and 3D-3D tunneling depending on the channel material. In D4.3, it was shown that for thick Silicon channels ($T_{CH} > 12.5nm$), formation of a pseudo-3D carrier gas occurs, due to the high effective masses of heavy holes and the Δ_2 valley electrons. For a more detailed comparison, we plot in Fig. 9 the transfer characteristics of the Ge EHBTFET with $T_{CH} = 7.5nm$ and of the Si EHBTFET with $T_{CH} = 15nm$ for different oxide thicknesses.

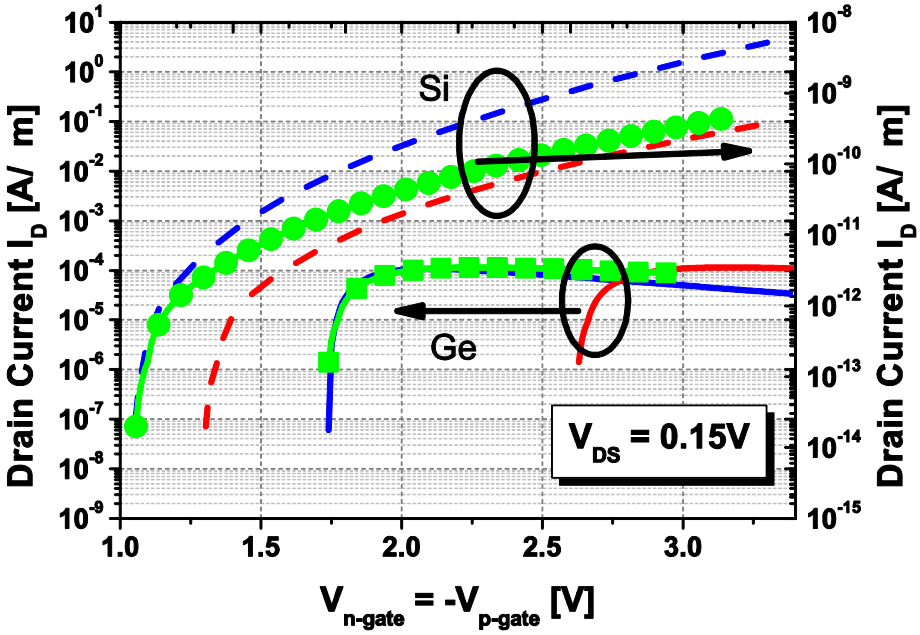


Figure 9: I-V transfer characteristics for Si (T_{CH} = 12.5nm) and Ge EHBTFETs (T_{CH} = 7.5nm) for different (blue) T_{OX} = 2nm and (red) T_{OX} = 1nm. The green curves are the shifted versions of the T_{OX} = 2nm (blue) cases to better highlight the difference in slope and current levels.

The most striking observation is that the improvement of the electrostatic control gained from the thinner oxide thickness (1nm) has essentially no impact on the ON current and the switching behavior of the 2D-2D tunneling case, except the expected shift in the tunneling onset voltage. In contrast to the 2D-2D case, the 3D-3D tunneling case exhibits a drastic improvement of the slope and therefore of the ON current. This is caused by the fact that in 2D-2D tunneling the number of states contributing to tunneling is constant until a new subband alignment is reached, which occurs at very high voltages. In the 3D case, however, a better electrostatic control always results in the addition of new states available for tunneling, thereby increasing the current. As demonstrated in Fig. 9, 2D-2D face tunneling inherently seems to be more suitable for low voltage operation, since the ON current very rapidly saturates with increasing V_{DD}.

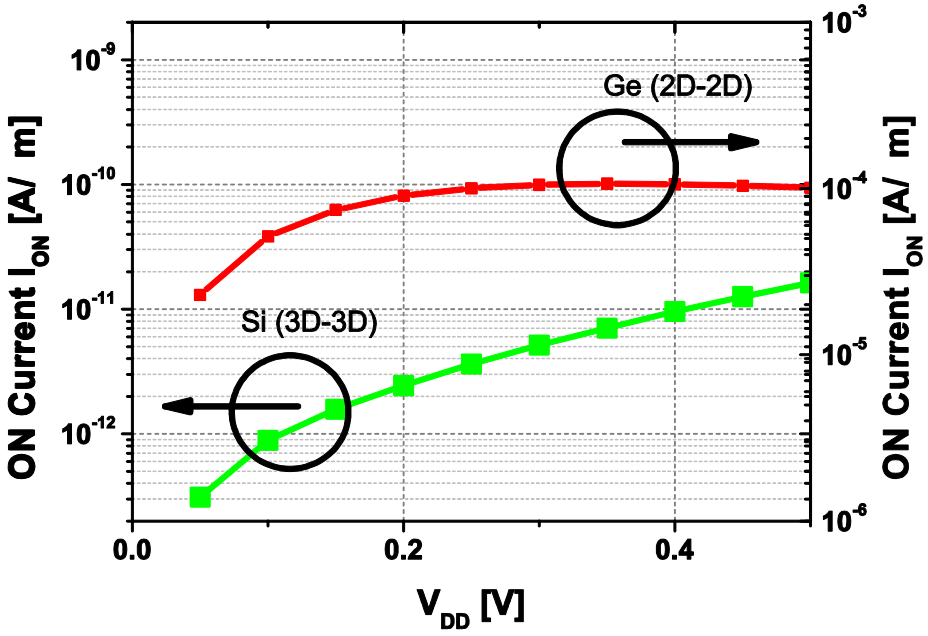


Figure 10: ON current versus gate overdrive ($V_{n-gate} = \frac{V_{align}}{2} + V_{DD} = -V_{p-gate}$) for 2D-2D and 3D-3D face tunneling devices.

2.4.2 Si-InAs Heterojunction TFET Simulations

In this subsection, we report the new results obtained by ETHZ using the atomistic simulator OMEN. The device is categorized as 2D-2D face tunneling since it utilizes an InAs quantum well embedded in a Si quantum well. This is confirmed by the generation plots in Fig. 11, the BTBT generation occurs along the entire gated region.

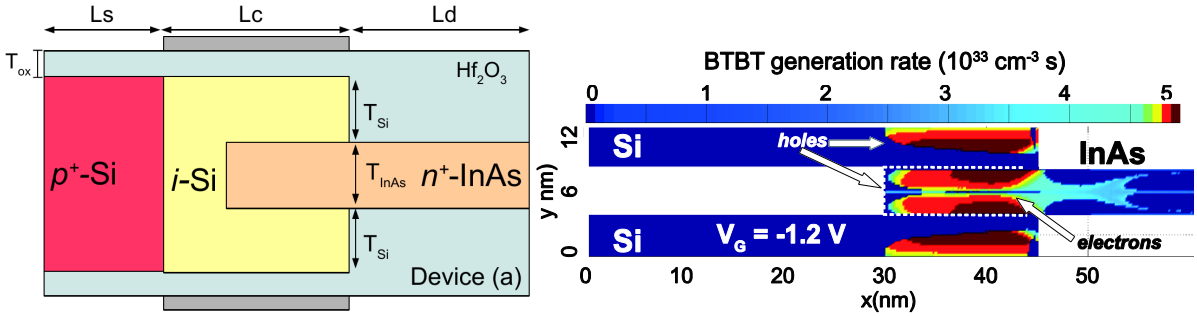


Figure 11: Si-InAs Heterojunction TFET BTBT Generation plot in the ON state.

The study shows an interesting trade-off between the ON current and the SS attainable in Fig. 12(Left). It is shown that lateral tunneling can be suppressed by narrowing down the InAs and Si film thicknesses. The transfer characteristics below seems to indicate that 2D-2D tunneling , occurring for narrower channels, may offer steeper switching compared to the 3D-3D ones, albeit having lower ON current levels, due to suppression of lateral leakage.

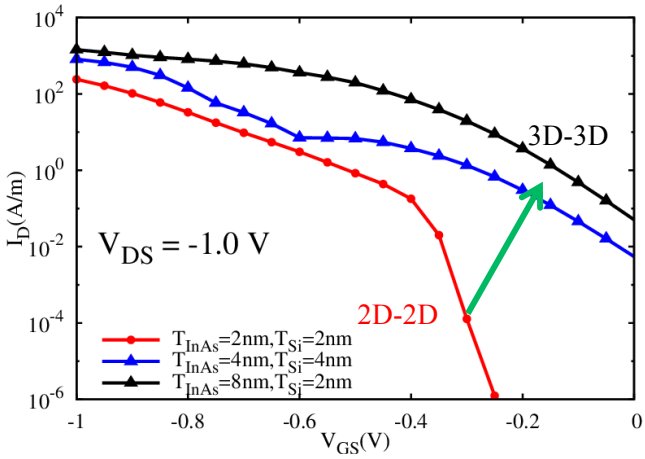


Figure 12: The transfer characteristic of InAs-Si EHBTFETs with different thicknesses.

3 Nanowire TFETs: Impact of Quantization and Heterojunctions

For this section, we utilize the nanowire TFET (see Fig 10(Left)) simulations performed by UNI-BO using 4-band k · p-NEGF simulations, for various square nanowire cross sections. We shall be investigating the impact of the cross section and discuss dimensional effects, as well as comparing the homo/heterojunction cases. Note that the heterojunction cases (InAs/GaSb NW TFETs) are already reported in D3.3, but here in this context the results will be reevaluated within the dimensionality context.

The nanowire TFETs studied here fall into the category of 1D-1D edge tunneling devices, the impact of the cross section area change is expected to be similar to the 1D-1D edge tunneling devices reported in section 2. Fig. 13(Right) reports the simulated I-V characteristics for InAs homojunction TFETs with different cross section areas. Similar to the k-limited cases studied in section 2, we see a very efficient suppression of the ambipolar leakage at low V_{GS}, due to the fact that as size-induced quantization becomes stronger; the low mass bands which typically contribute at low gate voltages are pushed to very high energies. Similar is the reduction in the ON current with decreasing cross section area due to enlarged bandgap.

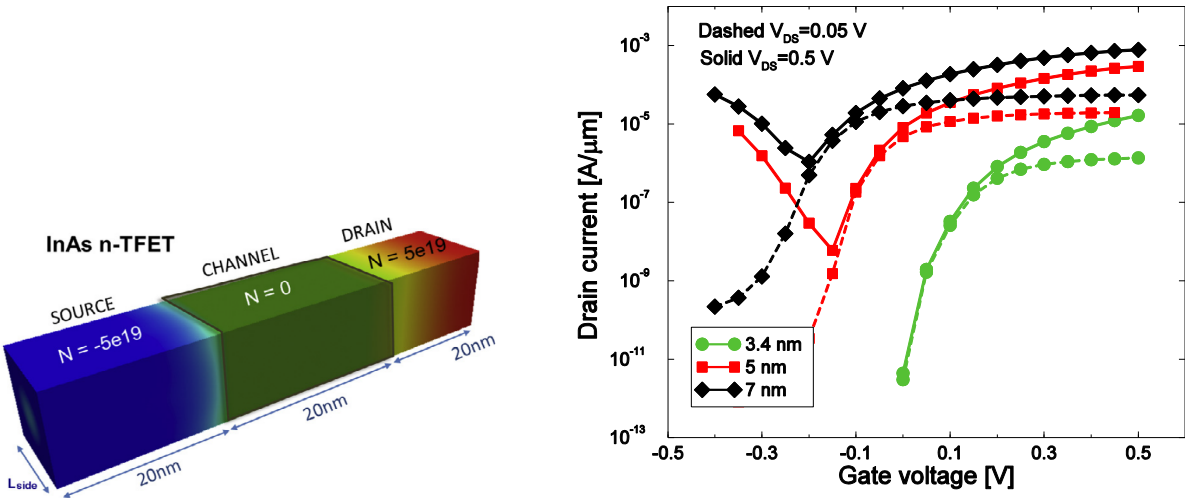


Figure 13: (Left) The nanowire TFET structure (Right) The transfer characteristics for different cross sections and different V_{DS} [5]. Note that the current is normalized with respect to the side of the cross section square.

As an affirmative way of checking that the devices are indeed 1D-1D tunneling devices, we plot the transmission rate per energy around the tunneling window. The transmission spectrum does not indicate any sudden increase in transmission, which is the typical sign of the contribution of a higher energy subband. Therefore, we conclude that the devices are indeed 1D.

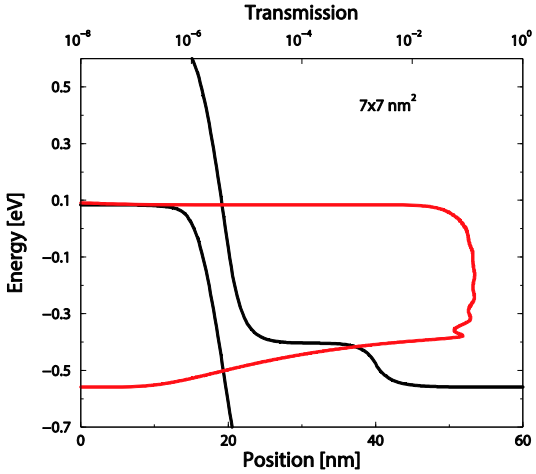


Figure 14: The current transmission spectrum at the tunneling junction around the tunneling energy window for the InAs $7\times7\text{nm}^2$ cross section nanowire. $V_{GS} = 0.3\text{V}, V_{DS} = 0.05\text{V}$.

Fig. 15 compares the case for homo- and hetero-junctions to investigate whether the dimensionality dependences change with respect to the junction type. The transfer characteristics indicate a striking improvement of the device switching slope when using hetero-junction, mainly due to OFF state reduction.

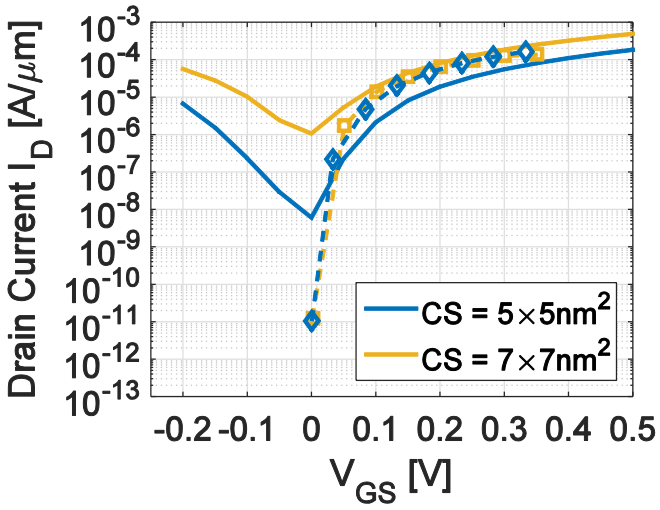


Figure 15: The transfer characteristics for the III-V nanowire TFETs with (solid, blue) 5x5nm^2 InAs homojunction $V_{DS} = 0.5V$ (solid, yellow) 7x7nm^2 InAs homojunction $V_{DS} = 0.5V$ (dashed w/symbols, blue) 5x5nm^2 InAs-GaSb heterojunction $V_{DS} = 0.3V$ (dashed w/symbols, yellow) 7x7nm^2 InAs-GaSb heterojunction $V_{DS} = 0.3V$.

4 Conclusions

An extensive comparison of different dimensionality cases of Tunnel FETs is performed by comparing the existing simulation data of obtained by WP3 and WP4 partners. It is seen that all the devices considered in D3.3 is 'subthermal' (i.e. SS<60mV/dec) for at least 3 decades of current.

1D and 2D EHBTFET simulations indicate that for all the considered channel materials, similar SS values are obtained (around 40mV/dec) although ON current levels vary greatly. Moreover, it is seen that the EHBTFET (a 2D-2D face tunneling device) is inherently more suitable for low supply voltage operation since the I-V transfer characteristics quickly saturate and increasing V_{DS} does not visibly increase the ON current.

The following dimensionality cases are compared:

- 2D-2D face vs 2D-2D edge tunneling
- 2D-2D face vs 1D-1D face tunneling
- 2D-2D edge vs 1D-1D edge tunneling
- 2D-2D face vs 3D-3D face tunneling

2D-2D edge and face tunneling devices are compared using the same channel thickness and EOT. It is seen that 2D-2D face tunneling can achieve much higher current levels and steeper switching compared to 2D-2D edge tunneling.

The impact of limiting the carrier dimensionality is studied by limiting the k-space along the transverse direction. Bearing in mind that the study neglects the electrostatic control improvements of the 1D-1D face tunneling device, it is seen that no visible performance improvement is gained by limiting the transverse k-space. One exception for that is the very effective suppression of the ambipolar leakage. Comparison between 1D-1D (transverse k-limited) and 2D-2D edge tunneling device indicates a shift of tunneling onset voltage and the reduction of the ON current due to bandgap increase due to transverse confinement.

2D-2D face tunneling and 3D-3D face tunneling devices are compared using 1D and atomistic simulations. 1D simulations show that 3D-3D tunneling devices are inherently more suitable for high supply voltage applications, whereas in 2D-2D tunneling a limit on the obtainable current is imposed due to the DOS reduction, which causes the saturation behavior. Atomistic simulations also partially confirm this idea since they indicate a tradeoff between 2D-2D tunneling and 3D-3D tunneling, where the former provides steeper switching but slightly lower current.

Comparison of homo and heterojunction nanowire TFETs reveal that using heterojunction (InAs-GaSb) is a very effective performance booster that improves both the switching slope and the ambipolarity. Nanowire TFET simulations indicate very promising steep slope switching behavior for the heterostructure nanowire TFETs. Similar to the k-limited 1D-1D edge tunneling simulations, decreasing the cross sections of the nanowires result in a similar voltage shift and a reduction in the ON current as well as reduction of the ambipolar leakage current.

Appendix 1: Transverse k-space Limited Simulation Framework

As stated in section 2.2, a modification to the existing EMA code was made to emulate transverse quantization. The procedure to calculate the BTBT in the presence of transverse quantization is given below, assuming the transverse length T_W and a constant potential along the transverse direction. The first modification is to rigidly add/subtract the quantization energy from the 'bulk' quantized energies. The second modification is to replace the 1-D joint density of states (JDOS) to a 0-D one. More specifically, the overall BTBT current is given by:

$$I_{dir,k-unlim} = 2\frac{eW}{\hbar}\sum_k \sum_{\alpha',k'\in v} |M_{cv}|^2 JDOS_{1D}(E_{k'\alpha'}, E_{k\Gamma})\Theta(E_{k'\alpha'} - E_{k\Gamma})\big(f_c(E_T) - f_v(E_T)\big)$$

where $JDOS_{1D}\left(E_{k'\alpha'}, E_{k\Gamma}\right) = \sqrt{\frac{\overline{m}}{\hbar^2\left(E_{k'\alpha'} - E_{k\Gamma}\right)}}$ using the parabolic approximation. $JDOS_{0D}(E_{k'\alpha'}, E_{k\Gamma})$, on the other hand is simply 1 (i.e. $JDOS_{0D}\left(E_{k'\alpha'}, E_{k\Gamma}\right) = 1$), since there's only one electron-hole pair that conserves the total energy. This is due to the fact that total energy needs to be conserved. The modified expression for current per transverse length is given by:

$$I_{dir,k-lim} = 2\frac{eW}{T_W\hbar}\sum_k \sum_{\alpha',k'\in v} |M_{cv}|^2 JDOS_{0D}(E_{k'\alpha'}, E_{k\Gamma})\delta(E_{k'\alpha'} - E_{k\Gamma})\big(f_c(E_T) - f_v(E_T)\big)$$

Note the replacement of the step function θ with the Dirac delta δ since we do not anymore have a continuous k-space along the transverse direction. The overall algorithm is given below.

1- Run the original EMA code (2D in k, 1D in space) to get the quantized energies for electrons and holes E_e^0, E_h^0 and wavefunctions ψ_e, ψ_h.
2- Calculate analytically the transverse quantization energies $E_e^{n,\perp}$ and $E_h^{n,\perp}$ using the analytical formula $E_{e,h}^{n,\perp} = \frac{\hbar^2\pi n^2}{2m_\perp^{e,h}T_W^2}$.
3- For all included transverse subbands 1…n…N:
    a. Calculate the total subband energies: $E_{e,h}^n = E_{e,h}^0 + E_{e,h}^{n,\perp}$.
    b. Use the modified BTBT tunneling formula.
    c. Sum all the contributions from all the subbands.

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