E2SWITCH

Energy Efficient Tunnel FET Switches and Circuits

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Energy Efficient Tunnel FET Switches and Circuits

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1 Introduction

In this report, design challenges with vertical TFET devices are reported. The industry standard software is adapted to accommodate for VTFET specific peculiarities. These developments allowed performing layout aware simulations. This was demonstrated in collaboration with IUNET on the ring oscillator level with 5nm-like ground rules and TCAD-calibrated compact models based on look-up tables. To demonstrate that all the tools work in sync and the developed analytical compact models do not cause convergence issues, and the layouts are correctly drawn, library characterization is performed with the imec analytical compact models calibrated on LUND device and corresponding ETHZ TCAD simulations.

2 Peculiarities of Vertical TFET Layouts

As source is not interchangeable with drain in TFETs, transistors become asymmetrical making series connection rather complex. If vertical architecture is used, designers may use different masks to indicate if a device should be made with source at the top or at the bottom. However, in practice, it is hardly possible due to both technological and economic constraints: this scheme implies that the technology would have to offer at least two flavours of nTFET and two flavours of pTFET each defined through a dedicated set of lithography masks. Therefore, the more realistic solution would be to fix source and drain orientations and to put an extra burden on local interconnects between the transistors.

A connection to a bottom electrode requires deep and narrow via which results in high access resistance to a bottom electrode. Thus, in order not to lose much of effective gate-source bias because of the *IR* drop, it is better to always place source of a VTFET on top and to keep drain on the bottom layer.

Layouts of VTFETs-based standard cells are difficult to interpret, because from the top-down view all the electrodes (top, gate, and bottom) overlap. It is natural to drive power rails above the top electrodes to ease contacting. This choice implies a need for extra routing tracks on the north and on the south resulting in taller standard cells with respect to lateral devices. Such an increase of the height of the VTFETs-based cells is possible as they do not require dummy gates at the edges of the cells. Lateral devices use them to separate fins between cells in the advanced technologies. Thus, although VTFET-based standard cells are taller than lateral cells, they are also narrower, which results in the overall similar cells area.

The discussion on cell height choice has already been presented in D6.3. Yet, the ground rules presented there were chosen to enable fair benchmarking with lateral FinFETs. Most of the work for this deliverable was done with scaled ground rules in mind, as the VTFETs were expected to be introduced for the ultimate digital logic scaling at 5nm technological node earliest.

3 VTFET Layouts

The chosen 5nm node ground rules are rather aggressive: contacted gate pitch is 32 nm and metal pitch is 24 nm as it was discussed in D3.5. With these ground rules, a set of standard cells was made including INV, NAND, XOR, D Flip-flop (DFF), Full adder (FA). XOR and FA were made in collaboration with IUNET visiting PhD student F. Settino. All the cells are 10 tracks tall with two outer tracks reserved for routing. For complex cells like DFF or FA this resulted in difficulties in local interconnect and larger utilization of M2 / M3 layers to finish the cell. The benchmarking exercise in D6.3 took this into account and INV layouts there had three tracks reserved for routing. Nevertheless, as all the designed cell were properly functional, we proceed with two tracks for routing. Figure 1 shows the layouts of the above-mentioned cells.

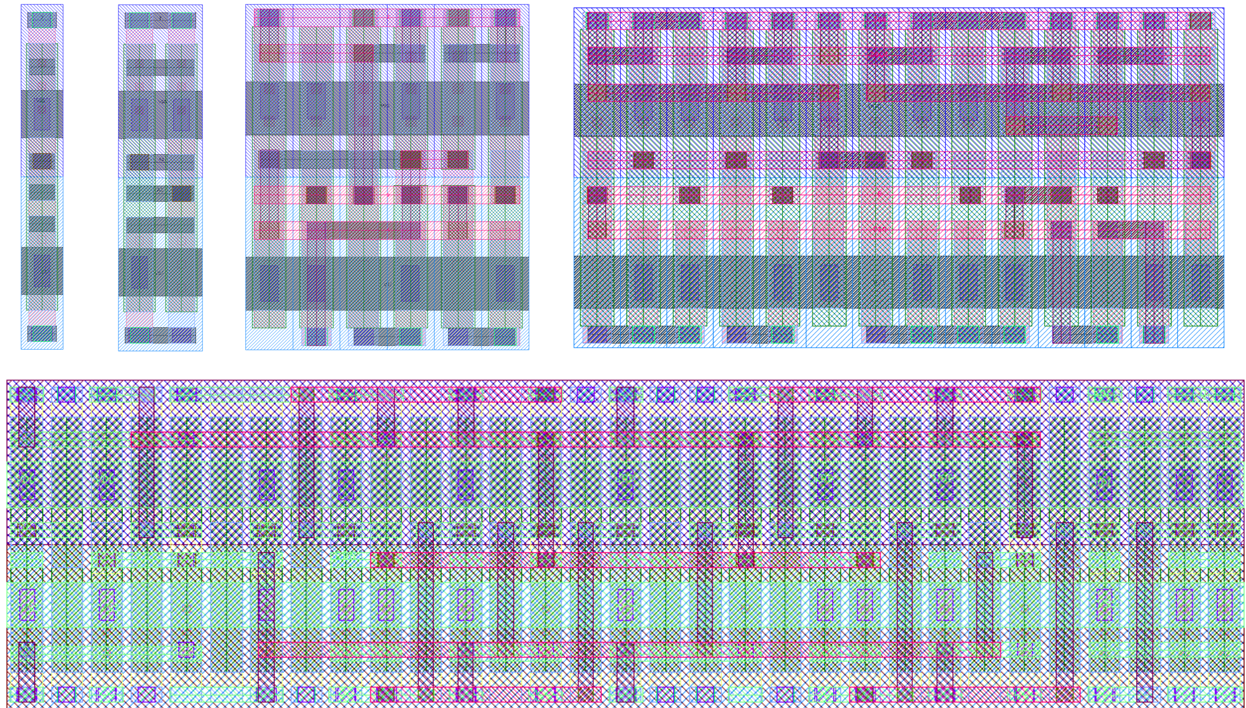

Figure 1: Layouts of various standard cells. Top row, left to right: INV, NAND, XOR, FA. XOR and Fa are made together with IUNET. Bottom row: DFF.

4 EDA Tools for Design with VTFET

To enable design with VTFETs, electronic design automation (EDA) tools had to adapted accordingly. To draw the layouts, no modifications were needed. It was enough to create the technology description with all the required layers. The enablement of PEX deck required some work, as the software had to a) recognize the drawn device and extract certain design features (like channel diameter); and b) correctly extract *RC* parasitics down to top electrode level. The parasitics from the top electrode level and below were handled by the scalable analytical macro model described D3.5. Device recognition was also important to enable layout versus schematic (LVS) verification step. The PEX deck was developed in the framework of Calibre® xACT™ software from Mentor Graphics. Once the cells were designed, they were fed into the library characterization tool (Cadence® Virtuoso® Liberate™). From this step onwards, the flow of the IC development does not differ from the conventional MOSFET techonlogies.

The impact of *RC* parasitics is mostly pronounced in the scaled technologies. In collaboration with IUNET, we looked at the impact of both macro model and cell parasitics on the ring oscillator performance made of inverters designed with 5nm ground rules. We used the IUNET look-up tables based compact model for the simulations (see D5.1 for details) and the INV layout shown in Figure 1. Figure 2 summarizes the findings.

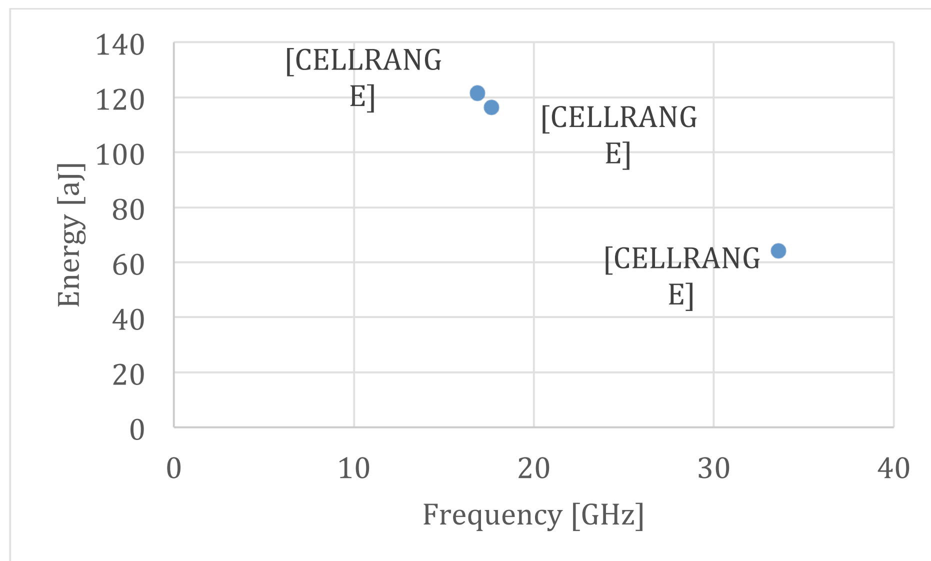

Figure 2: In collaboration with IUNET, the RO made with 5nm-like inverters was designed. The impact of FEOL parasitics was captured with the macro model. Extra cell parasitics were extracted from layouts with the developed PEX deck. In here, VDD = 250 mV.

As the compact models from D3.5 were based on the Lund device, which is relative large in size, we could not use directly the standard cell layouts presented in Figure 1. Nevertheless, to illustrate that the EDA tools can handle the VTFET' compact model along with the macro model, we created the standard cell library of netlists which were used for the library characterization.

The key parameters for the library characterization are the allowable delay transition time and the output capacitance. The minimum allowable delay transition time was set to 1 ps. This parameter is used to set the minimum output transition The maximum time should roughly be 10% of the clock period. As we do not know the target clock period, we assumed it to be 1 ns to mimic rather slow circuits. The minimum allowable output capacitance was set to 0.5 fF. The maximum output capacitance was computed automatically by the tool based on the maximum transition limitations. The tool generates look-up tables for various values of input slew and output loads which may be used afterwards for synthesis. Additionaly, the report is generated where key performance metrics and truth tables are automatically generated. Our library was characterized for a VTFET without traps at VDD = 0.3 V and having I_{OFF} = 10 pA. This regime was suggested to be optimal for VTFET based on the outcome of D6.3. The generated report is in Appendix A.

5 Conclusions

This deliverable presents:

- Challenges related to design with vertical TFET;
- Layouts of various logic standard cells;
- The design flow from layouts to library characterization.

Using the design rules of 5nm-like technological nodes, layouts for various standard cells made with vertical TFETs were presented. The EDA tools had to be adapted to enable design with VTFETs. As such, technology description file with relevant layers (bottom electrode, top electrode, etc.) was prepared, the PEX deck allowing device recognition and cell parasitics extraction was developed. These developments allowed to perform layout aware simulations. This was demonstrated in collaboration with IUNET on the ring oscillator level with 5nm-like ground rules and TCAD-calibrated compact models based on look-up tables. The analytical compact models based on Lund device and corresponding ETHZ TCAD simulations were used for the library characterization to highlight that the design flow works correctly up to this level. Next steps (synthesis, place and route) are not different from those for conventional MOSFETs.

Deliverable D5.4 - Design report on logic cell designs on vertical TFET technology

APPENDIX A

(Cadence® Virtuoso® Liberate™ library characterization report)

TFET Library

Cell Groups
DFF
FA
INV
NAND
XOR

DFF

TFET Cell Library: Process , Voltage 0.30, Temp 25.00

Truth Table

INPUT			OUTPUT
D	CDN	CP	Q
0	1	R	0
1	1	R	1
x	0	x	0
x	1	x	IQ

Pin Capacitance Information

Cell Name	Pin Cap(ff)			Max Cap(ff)
	D	CDN	CP	Q
DFF	1.42530	2.79188	1.40821	7.13790

Leakage Information

Cell Name	Leakage(pW)		
	Min.	Avg	Max.
DFF	13.37550	21.77400	27.25520

Delay Information

Delay(ns) to Q rising :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	**Avg**	**Max**
DFF	**CP->Q (RR)**	3.03532	3.47118	4.35548

Delay(ns) to Q falling :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	**Avg**	**Max**
DFF	**CP->Q (RF)**	2.52348	2.87729	3.64296
	CDN->Q (FF)	0.54225	0.90099	1.68880

Constraint Information

Constraints(ns) for D rising :

Cell Name	Timing Check	Ref Pin(trans)	Reference Slew Rate(ns)		
			min	avg	max
DFF	setup	CP (R)	1.27052	1.57181	1.82179
	hold	CP (R)	-0.79955	-0.65109	-0.53843

Constraints(ns) for D falling :

Cell Name	Timing Check	Ref Pin(trans)	Reference Slew Rate(ns)		
			min	avg	max
DFF	setup	CP (R)	0.55781	0.92771	1.20567
	hold	CP (R)	-0.34679	-0.10818	0.18687

Constraints(ns) for CDN rising :

Cell Name	Timing Check	Ref Pin(trans)	Reference Slew Rate(ns)		
			min	avg	max
DFF	recovery	CP (R)	-1.64098	-1.31759	-1.16037
	removal	CP (R)	1.57575	1.75030	2.13530

Min Pulse Width (ns) for CDN:

Cell Name	High	Low
DFF	-	1.4575

Min Pulse Width (ns) for CP:

Cell Name	High	Low
DFF	2.2632	1.7603

Power Information

Internal switching power(fJ) to Q rising :

Cell Name	Input	Power(fJ)		
		min	avg	max
DFF	**CP**	0.76326	0.78694	0.81238

Internal switching power(fJ) to Q falling :

Cell Name	Input	Power(fJ)		
		min	avg	max
DFF	**CP**	0.80110	0.80967	0.82336
	CDN	0.87601	0.88027	0.89041

Passive power(fJ) for D rising (conditional):

Cell Name	When	Power(fJ)		
		min	avg	max
DFF	**(CDN * CP) + (!(CDN) * CP * !(Q))**	0.01114	0.01303	0.01372
	(CDN * !(CP)) + (!(CDN) * !(CP) * !(Q))	0.19472	0.29976	0.32319

Passive power(fJ) for D falling (conditional):

Cell Name	When	Power(fJ)		
		min	avg	max
DFF	**(CDN * CP) + (!(CDN) * CP * !(Q))**	0.01013	0.01189	0.01274
	(CDN * !(CP)) + (!(CDN) * !(CP) * !(Q))	0.19700	0.32112	0.34720

Passive power(fJ) for CDN rising (conditional):

Cell Name	When	Power(fJ)		
		min	avg	max
DFF	**(CP * !(Q))**	0.01953	0.02335	0.02542
	(!(CP) * D * !(Q))	0.01637	0.02221	0.02469
	(!(CP) * !(D) * !(Q))	0.01129	0.01497	0.01695

Passive power(fJ) for CDN falling (conditional):

Cell Name	When	Power(fJ)		
		min	avg	max
DFF	(CP * !(Q))	0.02545	0.03061	0.03274
	(!(CP) * D * !(Q))	0.02750	0.03202	0.03345
	(!(CP) * !(D) * !(Q))	0.02604	0.03076	0.03236

Passive power(fJ) for CP rising (conditional):

Cell Name	When	Power(fJ)		
		min	avg	max
DFF	(CDN * D * Q)	0.27797	0.32933	0.33994
	(!(D) * !(Q))	0.28235	0.32698	0.33698
	(!(CDN) * D * !(Q))	0.33295	0.58024	0.63979

Passive power(fJ) for CP falling (conditional):

Cell Name	When	Power(fJ)		
		min	avg	max
DFF	(CDN * D * Q)	0.28959	0.34279	0.35443
	(!(D) * !(Q))	0.29372	0.34495	0.35839
	(!(CDN) * D * !(Q))	0.33877	0.54213	0.59022
	(CDN * D * !(Q))	0.31218	0.37666	0.39084
	(CDN * !(D) * Q)	0.31705	0.37790	0.39045

FA

TFET Cell Library: Process , Voltage 0.30, Temp 25.00

Truth Table

INPUT			OUTPUT	
A	B	CI	CO	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Pin Capacitance Information

Cell Name	Pin Cap(ff)			Max Cap(ff)	
	A	B	CI	CO	S
FA	5.26633	5.04983	3.63644	6.96971	5.82032

Leakage Information

Cell Name	Leakage(pW)		
	Min.	Avg	Max.
FA	15.85100	17.49200	18.24380

Delay Information

Delay(ns) to CO rising :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	Avg	Max
FA	A->CO (RR)	1.42745	1.88664	2.88093
	B->CO (RR)	1.58430	1.99714	2.76916
	CI->CO (RR)	1.45196	1.91614	2.93065

Delay(ns) to CO falling :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	Avg	Max
FA	A->CO (FF)	1.58648	2.00338	2.77582
	B->CO (FF)	1.43261	1.89574	2.90403
	CI->CO (FF)	1.46193	1.92723	2.94243

Delay(ns) to S rising :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	Avg	Max
FA	A->S (-R)	2.98972	3.26646	3.75825
	B->S (-R)	3.09365	3.40784	3.95856
	CI->S (-R)	3.00773	3.37991	4.21200

Delay(ns) to S falling :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	Avg	Max
FA	A->S (-F)	2.94995	3.31753	4.13571
	B->S (-F)	3.21791	3.53141	4.07148
	CI->S (-F)	3.10846	3.45972	4.24066

Power Information

Internal switching power(fJ) to CO rising :

Cell Name	Input	Power(fJ)		
		min	avg	max
FA	A	0.27914	0.29822	0.31737
	B	0.31007	0.33295	0.35151
	CI	0.30401	0.32357	0.34115

Internal switching power(fJ) to CO falling :

Cell Name	Input	Power(fJ)		
		min	avg	max
FA	A	0.32021	0.33737	0.35419
	B	0.27450	0.29627	0.31422
	CI	0.28011	0.30059	0.32024

Internal switching power(fJ) to S rising :

Cell Name	Input	Power(fJ)		
		min	avg	max
FA	A	0.32061	0.33900	0.35470
	B	0.36193	0.39419	0.42091
	CI	0.38406	0.41511	0.44250

Internal switching power(fJ) to S falling :

Cell Name	Input	Power(fJ)		
		min	avg	max
FA	A	0.39662	0.43112	0.45848
	B	0.33092	0.36751	0.39470
	CI	0.30758	0.32887	0.34578

INV

TFET Cell Library: Process , Voltage 0.30, Temp 25.00

Truth Table

INPUT	OUTPUT
I	ZN
0	1
1	0

Pin Capacitance Information

Cell Name	Pin Cap(ff)	Max Cap(ff)
	I	ZN
INV	1.45462	10.39704

Leakage Information

Cell Name	Leakage(pW)		
	Min.	Avg	Max.
INV	3.00034	3.00034	3.00034

Delay Information

Delay(ns) to ZN rising :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	**Avg**	**Max**
INV	**I->ZN (FR)**	0.10551	0.40202	1.30031

Delay(ns) to ZN falling :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	**Avg**	**Max**
INV	**I->ZN (RF)**	0.10498	0.40178	1.30036

Power Information

Internal switching power(fJ) to ZN rising :

Cell Name	Input	Power(fJ)		
		min	avg	max
INV	**I**	0.03359	0.03952	0.05764

Internal switching power(fJ) to ZN falling :

Cell Name	Input	Power(fJ)		
		min	avg	max
INV	**I**	0.03434	0.03934	0.05826

NAND

TFET Cell Library: Process , Voltage 0.30, Temp 25.00

Truth Table

INPUT		OUTPUT
A1	A2	ZN
0	x	1
1	0	1
1	1	0

Pin Capacitance Information

Cell Name	Pin Cap(ff)		Max Cap(ff)
	A1	A2	ZN
NAND	1.43333	1.28378	2.74426

Leakage Information

Cell Name	Leakage(pW)		
	Min.	Avg	Max.
NAND	0.34324	3.07416	6.00062

Delay Information

Delay(ns) to ZN rising :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	Avg	Max
NAND	A1->ZN (FR)	0.14806	0.28401	0.68778
	A2->ZN (FR)	0.12326	0.26376	0.67759

Delay(ns) to ZN falling :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	Avg	Max
NAND	A1->ZN (RF)	0.39148	0.62979	1.09016
	A2->ZN (RF)	0.37967	0.65867	1.35507

Power Information

Internal switching power(fJ) to ZN rising :

Cell Name	Input	Power(fJ)		
		min	avg	max
NAND	A1	0.10238	0.10524	0.11181
	A2	0.07654	0.07884	0.08387

Internal switching power(fJ) to ZN falling :

Cell Name	Input	Power(fJ)		
		min	avg	max
NAND	A1	0.07184	0.07367	0.07908
	A2	0.03916	0.04084	0.04504

Passive power(fJ) for A1 rising (conditional):

Cell Name	When	Power(fJ)		
		min	avg	max
NAND	(!(A2) * ZN)	0.00782	0.00920	0.00993

Passive power(fJ) for A1 falling (conditional):

Cell Name	When	Power(fJ)		
		min	avg	max
NAND	(!(A2) * ZN)	0.01862	0.01971	0.02012

Passive power(fJ) for A2 rising (conditional):

Cell Name	When	Power(fJ)		
		min	avg	max
NAND	(!(A1) * ZN)	-0.02164	-0.02127	-0.02083

Passive power(fJ) for A2 falling (conditional):

Cell Name	When	Power(fJ)		
		min	**avg**	**max**
NAND	**(!(A1) * ZN)**	0.03448	0.03481	0.03505

XOR

TFET Cell Library: Process , Voltage 0.30, Temp 25.00

Truth Table

INPUT		OUTPUT
A1	A2	Z
0	0	0
0	1	1
1	0	1
1	1	0

Pin Capacitance Information

Cell Name	Pin Cap(ff)		Max Cap(ff)
	A1	A2	Z
XOR	2.89683	2.70074	2.70123

Leakage Information

Cell Name	Leakage(pW)		
	Min.	Avg	Max.
XOR	12.25550	15.02510	18.01400

Delay Information

Delay(ns) to Z rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Avg	Max
XOR	A1->Z (RR)	!(A2)	0.94406	1.12591	1.46538
	A1->Z (FR)	A2	1.53896	1.75451	2.23534
	A2->Z (RR)	!(A1)	0.93562	1.11799	1.47461
	A2->Z (FR)	A1	1.47617	1.69533	2.18441

Delay(ns) to Z falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Avg	Max
XOR	A1->Z (FF)	!(A2)	0.76247	1.05469	1.60755
	A1->Z (RF)	A2	1.85666	2.13850	2.64669
	A2->Z (FF)	!(A1)	0.80186	1.09935	1.69253
	A2->Z (RF)	A1	1.90340	2.22712	2.95155

Power Information

Internal switching power(fJ) to Z rising (conditional):

Cell Name	Input	When	Power(fJ)		
			min	avg	max
XOR	A1	!(A2)	0.23784	0.24280	0.24905
	A1	A2	0.39906	0.40368	0.40990
	A2	!(A1)	0.22456	0.22852	0.23185
	A2	A1	0.35169	0.35711	0.36252

Internal switching power(fJ) to Z falling (conditional):

Cell Name	Input	When	Power(fJ)		
			min	avg	max
XOR	A1	!(A2)	0.24938	0.25297	0.25989
	A1	A2	0.53546	0.54276	0.55678
	A2	!(A1)	0.20328	0.20653	0.21418
	A2	A1	0.56864	0.58009	0.61900