

# E<sup>2</sup>SWITCH

## Energy Efficient Tunnel FET Switches and Circuits

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**Deliverable D7.10**

**Final public E2SWITCH workshop**

**Nature<sup>1</sup>:** R

**Dissemination level<sup>2</sup>:** PU

**Due date<sup>3</sup>:** M48

**Date of delivery:** M49

**Lead partner:** IUNET

**Contributing partners:** SCIPROM, imec, all

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<sup>1</sup> R = Report, P = Prototype, D = Demonstrator, O = Other

<sup>2</sup> PU = Public, PP = Restricted to other programme participants (including the Commission Services), RE = Restricted to a group specified by the consortium (including the Commission Services), CO = Confidential, only for the members of the consortium (including the Commission Services)

<sup>3</sup> Measured in months from the project start date (M01)

## Revision history

Version	Date	Authors	Comment
0.1	02.11.2017	Véronique Gobry	First version
0.2	17.11.2017	Véronique Gobry	Completions
1.0	29.11.2017	Véronique Gobry, Kirsten Leufgen, Lars-Erik Wernersson, Marie Garcia Bardon, Adrian Ionescu	Final deliverable version, approved by the coordinator

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<sup>4</sup> For up-to-date contact details, please refer to the contact page of the Members section:  
<http://www.OTOSTEM.org/members/contactdetails/index.php>.

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## Summary

The final E<sup>2</sup>SWITCH workshop entitled “Tunnel FET Workshop” was a one-day event organized on the occasion of the project closure. It was held on the 10<sup>th</sup> of November 2017, hosted by imec in Leuven, Belgium.

In this workshop the achievements of the E<sup>2</sup>SWITCH project have been presented and discussed, namely fabrication of lateral and vertical III-V and IV TFETs, TCAD simulations, analytical modelling and digital and analogue circuits benchmarks. The project presentations have been completed by presentations by invited speakers, opening the discussion of future prospects and challenges.

## **1. Overview**

This deliverables describes the final E<sup>2</sup>SWITCH workshop, namely

- The workshop preparation and advertisement,
- The workshop programme,
- The workshop proceedings incl. presentations and participants list,
- The workshop conclusions.

## 2. Workshop preparation

### 2.1 Workshop advertising

Before the workshop, a public webpage dedicated to the workshop has been created on the E<sup>2</sup>SWITCH website (Figure 1):

<http://www.e2switch.org/output/workshops/>.

The screenshot shows a web browser window with the URL [www.e2switch.org/output/workshops/index.html](http://www.e2switch.org/output/workshops/index.html). The page has a green header with the E<sup>2</sup>SWITCH logo and the text "Energy Efficient Tunnel FET Switches and Circuits". On the right side, there is a navigation menu with buttons for Home, The Project, Consortium, Output, Workshops, Publish. Summaries, Publications, and News. The main content area is titled "Workshops" and contains the following text:

In this page you will find information about past or future workshop co-organized by the E<sup>2</sup>SWITCH project. Click on the **i** sign to show more information.

**Final Workshop** **i**  
Energy Efficient Tunnel FET Switches and Circuits

10 November 2017  
IMEC, Belgium

This one-day workshop is organized for the closure of the E<sup>2</sup>SWITCH EU programme on Energy Efficient Tunnel FET Switches and Circuits and will highlight the results obtained within the program and complemented by external speakers. Steep transistors with subthreshold swings less than 60 mV/decade are attracting attention worldwide to continue the scaling roadmap and enable electronic systems operating at 300 mV and below. Transistors based on inter-band tunneling (TFETs) are promising and have seen important development in the last years, but there is still no consensus on materials or device architecture, on the mechanisms limiting current performance, on the exact field and conditions of application. In this workshop, the achievements of E<sup>2</sup>SWITCH project will be presented and discussed: fabrication of lateral and vertical III-V and IV TFETs, TCAD simulations, analytical modelling, and digital and analog circuits benchmarks. These focused presentations will be combined with presentations by invited speakers opening the discussion to future prospects and challenges.

Buttons on the page include: "Download the agenda", "Register for the workshop via the imec academy portal (registration required)", and "Practical Information".

**Organisers**  
E<sup>2</sup>SWITCH Project  
imec, Belgium

**Contact**  
Marie Garcia Bardon  
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The imec logo is shown at the bottom of the page.

**Figure 1:** The workshop webpage.

The workshop was also advertised on the public events calendar of the imec academy and promoted via imec internal channels (Figure 2).

< **November 2017** >

All Events  My Events

	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY
	30	31	1	2	3 NERF seminar: Encoding of three-dimensional head-displacement vectors for goal-oriented actions in the mouse 12:00 CET
	6 Beyond CMOS 09:00 CET	7 Beyond CMOS 09:00 CET	8 Beyond CMOS 09:00 CET	9 Beyond CMOS 09:00 CET	10 Beyond CMOS 09:00 CET Tunnel FET workshop 09:00 CET
	13 Nanoscale CMOS process technology 09:00 CET	14 Nanoscale CMOS process technology 10:00 CET	15 Upgrade to Custom ASIC 08:30 CET Nanoscale CMOS process technology 09:00 CET	16 Nanoscale CMOS process technology 09:00 CET	17 Nanoscale CMOS process technology 09:30 CET
	20	21	22	23	24

Figure 2: imec events calendar.

Moreover, the event was announced on the project News page (Figure 3).

The image is a screenshot of a web browser displaying a news announcement on the E2SWITCH website. The browser's address bar shows the URL 'e2switch.org/news/index.php'. The website's header features the E2SWITCH logo, which consists of a stylized 'E<sup>2</sup>' in green and 'SWITCH' in grey, with the full name 'Energy Efficient Tunnel FET Switches and Circuits' below it. The main content area has a white background with a green border. The announcement title is 'E2SWITCH final workshop: 10 Nov 2017, imec Leuven', dated '18 October 2017'. The text invites visitors to a workshop on 10 Nov 2017 at imec, Leuven. It describes the workshop as a one-day event for the closure of E2SWITCH - Energy Efficient Tunnel FET Switches and Circuits. The text discusses the importance of steep transistors with subthreshold swings less than 60 mV/decade and mentions that TFETs are promising but still lack consensus on materials and device architecture. A list of topics to be discussed includes fabrication of lateral and vertical III-V and IV TFETs, TCAD simulations, analytical modelling, and digital and analog circuit benchmarks. It also mentions that the workshop will include presentations by invited speakers. Finally, it directs visitors to a workshop webpage for more details and registration information.

**Figure 3:** News announcement.

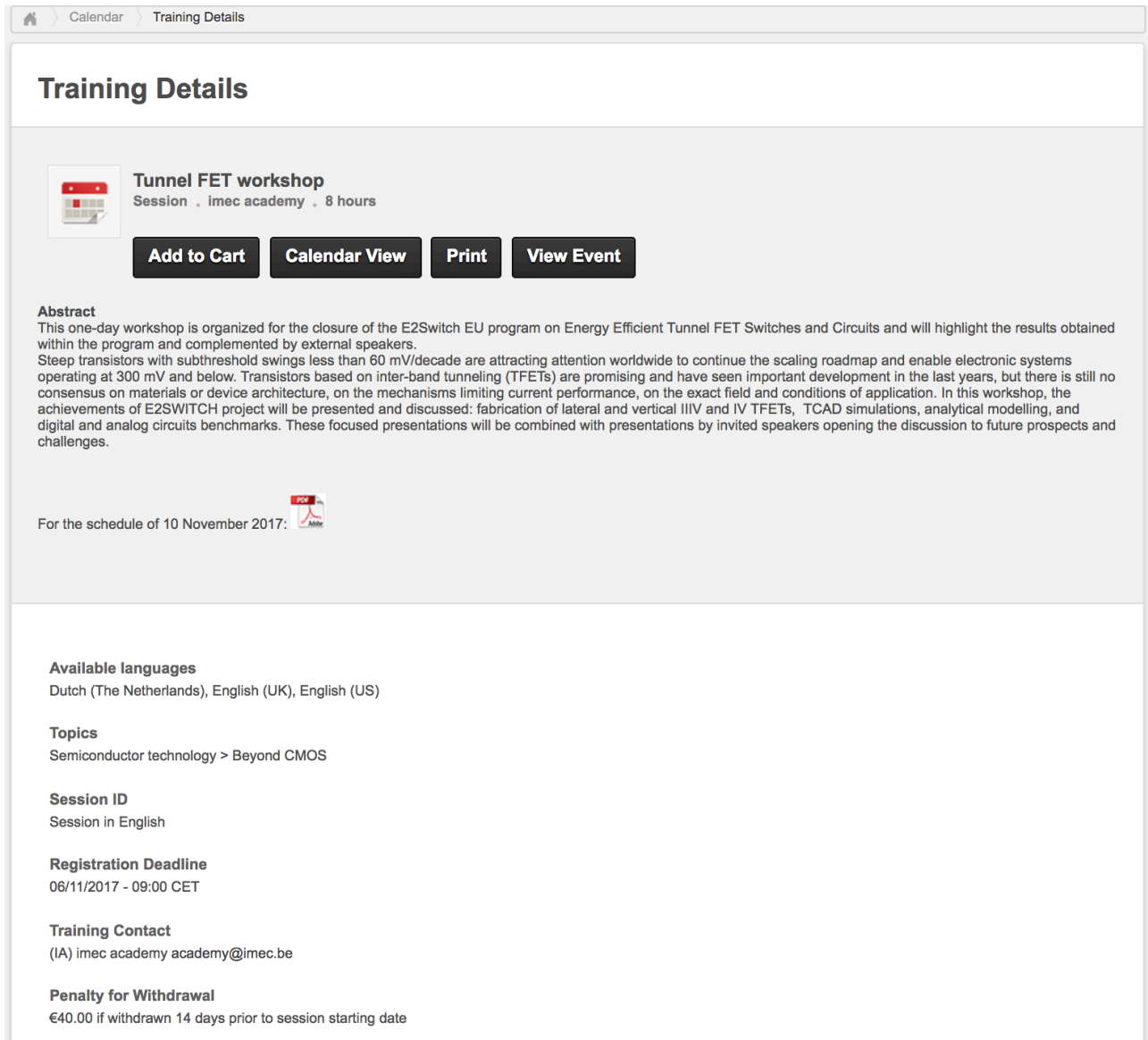
## 2.2 Workshop organisation

The workshop page presents the aim of the workshop and gives the visitor all the information needed to attend the event through three buttons.




## 2.2.1 Registration

The registration button redirects the visitor towards the imec academic portal where the registration can be completed (Figure 4).



The screenshot shows a web page titled "Training Details" with a breadcrumb trail "Calendar > Training Details". The main heading is "Training Details". Below this, there is a section for a "Tunnel FET workshop" session, which is part of the "imec academy" and lasts for "8 hours". There are four buttons: "Add to Cart", "Calendar View", "Print", and "View Event".

**Abstract**  
This one-day workshop is organized for the closure of the E2Switch EU program on Energy Efficient Tunnel FET Switches and Circuits and will highlight the results obtained within the program and complemented by external speakers. Steep transistors with subthreshold swings less than 60 mV/decade are attracting attention worldwide to continue the scaling roadmap and enable electronic systems operating at 300 mV and below. Transistors based on inter-band tunneling (TFETs) are promising and have seen important development in the last years, but there is still no consensus on materials or device architecture, on the mechanisms limiting current performance, on the exact field and conditions of application. In this workshop, the achievements of E2SWITCH project will be presented and discussed: fabrication of lateral and vertical IIIIV and IV TFETs, TCAD simulations, analytical modelling, and digital and analog circuits benchmarks. These focused presentations will be combined with presentations by invited speakers opening the discussion to future prospects and challenges.

For the schedule of 10 November 2017: 

**Available languages**  
Dutch (The Netherlands), English (UK), English (US)

**Topics**  
Semiconductor technology > Beyond CMOS

**Session ID**  
Session in English

**Registration Deadline**  
06/11/2017 - 09:00 CET

**Training Contact**  
(IA) imec academy academy@imec.be

**Penalty for Withdrawal**  
€40.00 if withdrawn 14 days prior to session starting date

**Figure 4:** Registration page on the imec website.

## 2.2.2 Agenda

The programme of the event along with details about the presentation format can be downloaded from the agenda button (Figure 5). The workshop was divided into different sections with speakers giving 30 min of focused talks on their respective topic of interest. Since the audience knows the field and most of the work at the different groups, no introductions were provided, allowing focus on the key innovative aspects.



### E<sup>2</sup>SWITCH Final Workshop 10 November 2017 — imec, Belgium

9h00	<b>Welcome and introduction to the workshop</b>	Adrian Ionescu » EPFL
9h10	<b>Physics an performance of III-V nanowire heterojunction TFETs including phonon and impurity band tails: An atomistic mode space NEGF quantum transport study</b>	Aryan Azfalian » Guest – TSMC
9h40	<b>III-V nanowire TFETs</b>	Lars-Erik Wernersson » Lund
10h10	<b>Energy filters and sub-unity body factors as boosters for better energy efficiency on advanced CMOS platforms'</b>	Adrian Ionescu » EPFL
10h40	<b>Break</b>	
11h00	<b>Tunnel-FET: bridging the gap between prediction and experiment through calibration</b>	Anne Verhulst » Guest – imec
11h30	<b>Complementary III-V heterojunction TFETs</b>	Kirsten Moselund » IBM
12h00	<b>Group IV semiconductor TFETs</b>	Qing-Tai Zhao » JUELICH
12h30	<b>Lunch</b>	
13h45	<b>Modeling the effect of non-idealities on III-V/Si and All-III-V TFETs</b>	Saurabh Sant » ETHZ
14h15	<b>Digital evaluation of TFETs in scaled nodes</b>	Dmitry Yakimets Marie Garcia Bardon » imec
14h45	<b>Full-quantum modeling of Si/SiGe/III-V Tunnel-FETs architectures</b>	Elena Gnani » IUNET
15h05	<b>Simulation of digital and analog/mixed-signal circuits employing Tunnel-FETs</b>	Pierpaolo Palestri » IUNET
15h25	<b>Break</b>	
15h45	<b>TFET based on 2-D semiconductors: a modeling perspective</b>	Mathieu Lusier » ETHZ
16h15	<b>Building transistors with 2D for back-end applications</b>	Iuliana Radu » imec

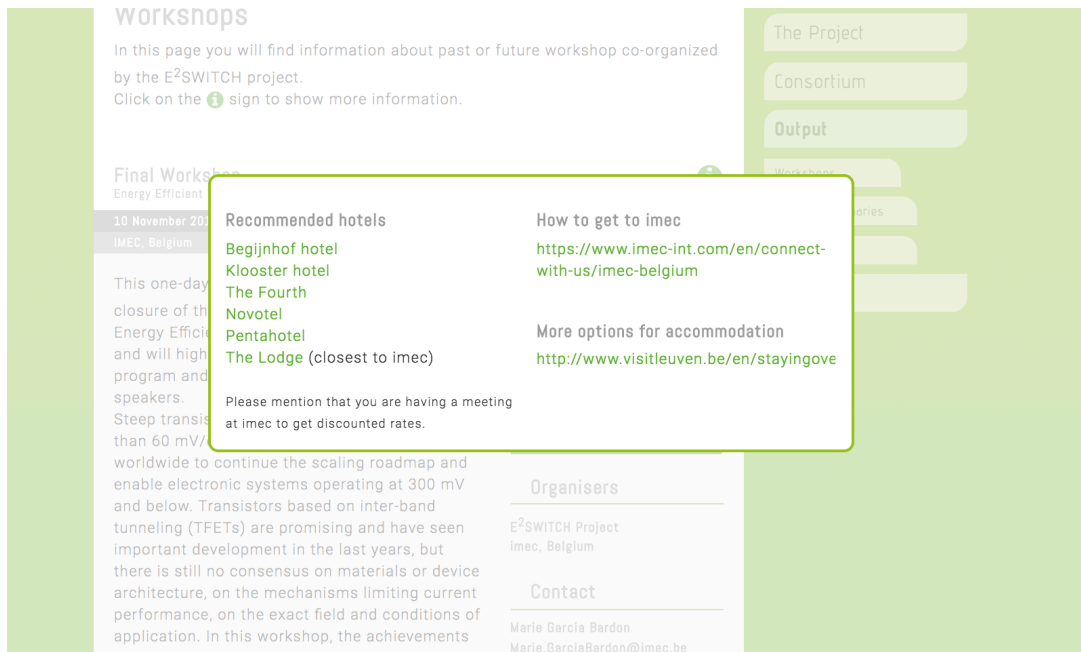


The research leading to these results has received funding from the European Community's Seventh Framework Programme under grant agreement No. 619509 (Project E<sup>2</sup>SWITCH).

**Figure 5:** Agenda of the workshop.

### 2.2.3 Practical information

Practical details including recommended hotels and travel directions were available through the practical information button (Figure 6).



**Figure 6:** Practical information pop-up window.

### 3. Workshop proceedings

#### 3.1 Participants

The interest in the E<sup>2</sup>SWITCH findings was substantial and the workshop with 46 participants well attended. Table 1 shows the list of participants with their affiliations (where available).

**Table 1:** List of participants.

Participant name	Affiliate
Adrian Ionescu	EPFL
Arayn Azfalian	imec
Lars-Erik Wernersson	LUND
Qing-Tai Zhao	JUELICH
Elena Gnani	IUNET
Pierpaolo Palestri	IUNET
Elme Gnomi	IUNET
BT Chan	imec
Marina Bangshni Lova	imec
Tarun Agamal	imec
Alexey Mileniu	imec
Jung Kyu Chae	imec
Doyoung Jang	imec
Ben Kaczer	imec
Veeresh Deshpande	imec
Patrick Verdonck	imec
Anne Verhulst	imec
Jasper Bizindavyi	imec
Dmitry Yakimets	imec
Tsvatan Ivanov	imec
Marie Garcia Bardon	imec
Vamsi Putcha	imec
Jacob Franco	imec
Jaber Derakhshandeh	imec
Negin Golshani	imec
Anabela Veloso	imec
Salim El <b>Kazzi</b>	imec
Dennis Lin	imec
Sergiu Clima	imec
Saurabh Sant	ETHZ
Mathieu Lusier	ETHZ
Kirsten Moselund	IBM

<b>Pierre Eyben</b>	imec
<b>Iuliana Radu</b>	imec
<b>Yashwanth Balaji</b>	KU Leuven
<b>Francky Catthoor</b>	KU Leuven
<b>Gabriel Khalil El Hajjam</b>	CEA
<b>Somya Gupta</b>	KU Leuven
<b>Doyoung Jang</b>	imec
<b>Clément Merckling</b>	imec
<b>Ramy Nashed Bassely Said</b>	Georgia Institute of Technology
<b>Peter Ramvall</b>	LUND
<b>Quentin Smets</b>	imec
<b>Vishal Tiwari</b>	IIT Madras, India
<b>Thomas Chouette</b>	IGEFI Lyon
<b>Eric Fribourg-Blanc</b>	European Commission

### 3.2 Presentations

Presentations were given by the following E<sup>2</sup>SWITCH partners:

- EPFL
- Lund
- IBM
- JUELICH
- ETHZ
- imec
- IUNET

Besides those presentations, 2 guest speaker presentations by Anne Verhulst from imec and Aryan Azfalian from TSMC were arranged.

The presentations given during this event can be downloaded from the public E<sup>2</sup>SWITCH workshop webpage: <http://www.e2switch.org/output/workshops/>.

## 4. Conclusions

The workshop was positively perceived with good attendance from within imec, from process, TCAD and circuit specialists. It led to very interesting exchanges and positive feedbacks. The public appreciated the mix of speakers covering TFETs from different angles: accurate physics, TCAD simulations, breaking edge fabricated devices, model calibration, and circuit level analysis, as well as opening the discussion towards 2D materials. The content was actually very dense for a one-day workshop and could have been split in two days.

The results of the E<sup>2</sup>SWITCH partner Lund University had the highest attendance and raised the most questions, as it is the best fabricated TFET published, a vertical III-V nanowire heterojunction TFET integrated on a Si substrate with lowest  $S_{min}$  and highest drive current.

In the invited speakers, the tenor was Aryan Azfalian presenting a simulation strategy based on an atomistic mode space NEGF quantum transport allowing to predict the performance of III-V nanowire heterojunction TFETs including phonon and impurity band tails. The work of Anne Verhulst on bridging the gap between prediction and experiments through calibration was also of highest value for the public. The presentations of Mathieu Lusier on 2-D semiconductors based TFETs, of Iuliana Radu on 2D back-end transistors and of Adrian Ionescu on innovative sub-60mV/dec devices were opening the discussion towards longer term future research.

Since sub-60mV/dec subthreshold slope TFETs are now demonstrated, interesting discussions followed on future research. The first points of attention are further scaling of the dimensions to comply the density requirements of advanced nodes, and further improvement of the electrostatics through the reduction of bulk traps, avoiding problematic processing steps that could lead to these defects. There is also an agreement on the need to work on higher drive current, pushed by the circuit level analysis showing the need for higher  $I_{on}$  current to make TFETs more competitive, and not only limited to niche application. This could be done by improving the contacts, as well as further EOT scaling. There is also agreement on the need to address variability, from device to circuit analysis. All these points could lead to future activities and collaborations between partners.