E2SWITCH
Energy Efficient Tunnel FET Switches and Circuits

Co-funded by the European Union

E²SWITCH

Energy Efficient Tunnel FET Switches and Circuits

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Deliverable D7.7	**First update of the Plan for Use and Dissemination of Foreground (PUDF)**

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[1] R = Report, P = Prototype, D = Demonstrator, O = Other

[2] PU = Public, PP = Restricted to other programme participants (including the Commission Services, RE = Restricted to a group specified by the consortium (including the Commission Services), CO = Confidential, only for the members of the consortium (including the Commission Services)

[3] Measured in months from the project start date (M01)

Revision history

Version	Date	Author	Comment
0.1	23-10-2015	V. Gobry	First draft
0.2	11-11-2015	L.-E. Wernersson	Completions dissemination
0.3	16-11-2015	F. Chowdbury	Completions exploitation
0.9	24-11-2015	V. Gobry, K. Leufgen, P. Ulrich	Review, completions, rearrangements
1.0	24-11-2015	K. Leufgen	Final version

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Summary

This document contains updates on the "**Plan for Use and Dissemination of Foreground (PUDF)**" as set in work package 7 (WP7) of the description of work defined for the E^{2}SWITCH project. All dissemination and exploitation activities, together with details of specific deliverables as outlined in WP7 are planned and recorded in this document.

As part of its primary impacts, E^{2}SWITCH aims to **enable ultra-low voltage/low power nanoelectronic solutions** through the **exploitation of Tunnel Field Effect Transistors (TFET).** Those new devices are anticipated to go beyond current industrial roadmaps in terms of energy efficiency by a factor or 10 to 100 times, with an operating voltage below 250mV with standby power reduction by more than 1000x.

With such potentials for energy efficient solutions, dissemination and exploitation tasks will promote the long-term impact on both the scientific and the technical fields.

The main cornerstones of this work are the following:

- Setup and maintenance of the project's website, publication of results in the scientific community, and dissemination to a wider public through academic, technology transfer and industrial channels.
- Development of a general exploitation strategy for E^{2}SWITCH results and definition of a concrete policy for the exploitation of the technical results of the project in industrial applications with two main paths: (i) digital and (ii) analog/RF.
- Networking with other EC funded research projects as well as with ENIAC and ITRS working groups and other possible players concerning publicly available project activities.
- Organisation of international workshops on the specific scientific and technical research addressed by the project: energy efficient devices and technologies and their applications in digital and non-digital applications.
- Contribution to the training of PhD students and senior staff through scientific seminars, summer schools, specific chapters in lectures and books.
- Encouragement of mobility of young researchers and PhDs between partners.

All partners involved with research will continuously and proactively evaluate opportunities for dissemination and exploitation of the project concept and its results. SCIPROM, responsible for E^{2}SWITCH management, takes care of the website. LUND, as dissemination manager, will coordinate all dissemination activities and leads the work. CCS, with the help of EPFL, will overlook the project's exploitation based on all E^{2}SWITCH findings as agreed by all partners. More details on the E^{2}SWITCH dissemination and exploitation strategies and related IPR considerations can be found in Section 3.2 of the DoW [1].

The first two years of the E^{2}SWITCH consortium have been very productive in terms of scientific results and the partners have been very active in the dissemination of the results to the various stakeholders including the scientific community, relevant industry, and the general audience. The complete list of dissemination activities is available on the web page of the consortium and within Section 4 of this document. In Table 1 some statistics of the activities during the first 24 months is given:

Table 1: Dissemination activities, status 23 Nov 2015.

Type of dissemination activity	
Film	1
Flyer	1
Scientific presentation	54
Poster presentation to a scientific event	1
Organisation of workshop	2
Press release	1
Publication	39
Web sites / Applications	1
Total	**100**

Highlights include 6 invited talks, 3 high-impact journal papers (Nature photonics, Nano letters) and 2 high-impact conference papers (IEDM 2015).

The full list of E^{2}SWITCH dissemination activities can be found in Section 4 of this document.

Workshops:

- In the Quest for Zero Energy Devices and Circuits Workshop at ESSDERC 2014, Venice, Italy
- Steep Slope Transistors International Workshop at Notre Dame, 2015, USA

1 Overview

The E²SWITCH WP7 comprises all dissemination and exploitation activities.

1.1 List of WP7 Deliverables

- D7.1 Website (first preliminary version) – M03
- D7.2 Press release at the project start – M01
- D7.3 Press release in the project end – M42
- D7.4 Video introduction to the project – M06
- D7.5 Project flyer – M06
- D7.6 First version of the Plan for Use and Dissemination of Foreground (PUDF) - M06
- D7.7 First update of the PUDF – M24
- D7.8 First public E²SWITCH workshop – M24
- D7.9 Roadmap for commercial use of E²SWITCH results – M42
- D7.10 Final public E²SWITCH workshop – M42

1.2 List of Milestones

- M7.1 Final PUDF ready for consortium approval – M41
- M7.2 Roadmap for commercial use of E²SWITCH results ready for consortium approval – M41

1.3 Dissemination and Exploitation Management Structure

The integration of the dissemination and exploitation activities within the management structure is described in detail in Sections 2.1 and 3.2 of the DoW [1].

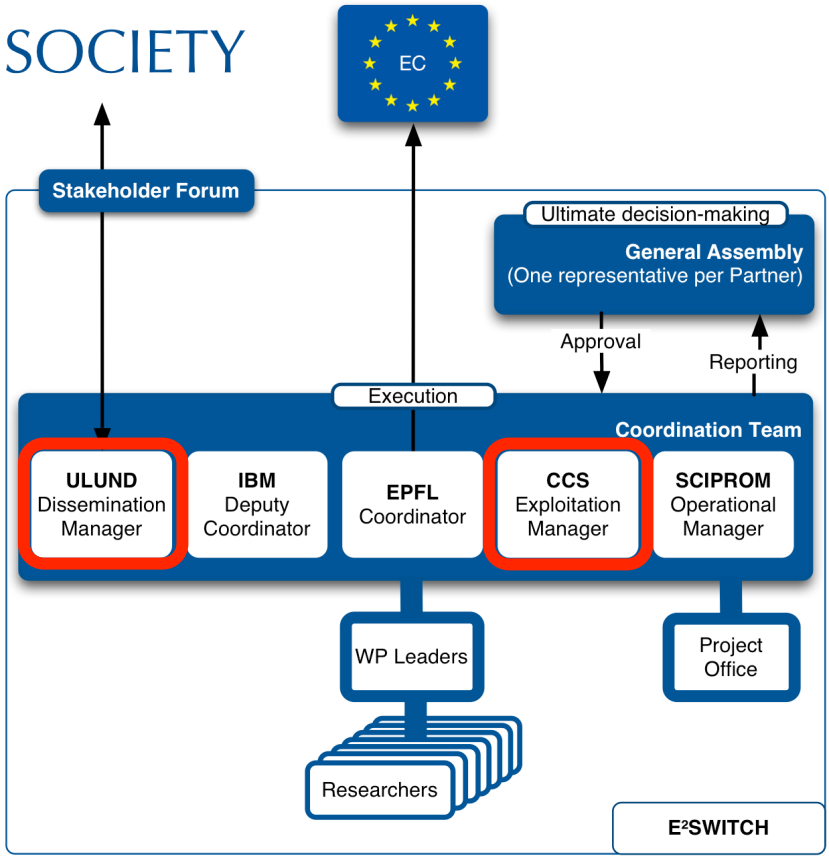


Fig. 1. Structure of the E²SWITCH management structure with the position of the Dissemination and Exploitation managers.

2 Dissemination of knowledge

This section describes the dissemination measures, including any scientific publications relating to foreground. The content of the corresponding section of the online PUDF on SESAM that is part of the final report **will be made available in the public domain,** thus demonstrating the added value and positive impact of the project on the European Community. However, the **present version contains additional information and has to be treated as confidential**.

This section includes a list of planned, ongoing and completed dissemination activities (publications, conferences, workshops, web, press releases, flyers, etc). Articles that have been published in the popular press will be listed as well.

The list of all published scientific (peer reviewed) publications relating to the foreground of the project is given in Table A.1 (see Section 4), respectively.

A list of all completed dissemination activities is given in Table A.2.

The impact of E^{2}SWITCH on the advancement of science and ultimately the benefit of citizens will be fundamentally linked to the presentation of its results in scientific conferences and especially publications in high-impact journals. In addition, the E^{2}SWITCH consortium considers dissemination to stakeholders and a wider public to also be of high importance to its success. The **Dissemination Manager (Lars-Erik Wernersson, LUND)** will liaise with the Exploitation Manager on approving all disclosures. They will develop and administer a procedure for the submission and approval of disclosures before publication. The partners have experience from previous and current collaborative research projects where such procedures have been successfully utilised to ensure widespread and beneficial dissemination whilst protecting valuable Intellectual Property.

The Dissemination Manager, together with SCIPROM, will support coherent and high quality dissemination by providing guidelines and templates for the production of documents, press releases and presentations. In addition, internal peer review of drafts will be supported to ensure articles generated for publication are of the highest quality and appropriate for their target audiences. This will be particularly important in the support and development of new researchers in the project team.

2.1 Main dissemination activities for the current period

2.1.1 Communication to the general public (M01 – M42)

Lead Partner SCIPROM; other partners: All

Communication to the general public has been achieved through a variety of communication means.

The E^{2}SWITCH website (D7.1, M03), has been set up, is hosted and maintained by SCIPROM. It contains a consortium-intern section for data exchange and management and a public section that serves as a dissemination gateway. For the latter, care will be taken to specifically address all stakeholders in energy efficient devices and technologies and their applications in digital and non-digital applications.

A press release has been issued in the first year of the project (D7.2). A project flyer (D7.5, M09) introducing the project has been prepared by SCIPROM in collaboration with all partners in the beginning of the project and updated in M14. An introductory video has also been released in the beginning of the second year (D7.4). It is conceived as a teaser directing the different stakeholders to the relevant part of the website.

2.1.2 Communication to the relevant scientific communities (M07 – M42)

Lead Partner: EPFL: other partners: All research partners

One of the major impacts of E^{2}SWITCH will be the promotion of European scientific leadership in the area of future electronic devices and low-power technologies. This will be achieved by:

- **Scientific publications** in high-ranked peer-reviewed scientific journals.
- Arrange partners of E^{2}SWITCH to regularly give presentations in international **scientific conferences**, including the presentation of **keynote speeches**.
- Organize dedicated dissemination events devoted to the project topics at the major **European PhD summer schools**, such as for instance: SINANO – Italy, MIGAS – France, Dresden Academy – Germany)

2.1.2.1 Publications

Table A.1 in Section 4.1 shows a list of all E^{2}SWITCH peer-reviewed articles published so far.

2.1.2.2 Participation in Scientific conferences

All E^{2}SWITCH presentations at scientific conferences and workshops are shown in Table A.2 (Section 4.1).

2.1.2.3 Workshops

Two public workshops have been organized during the period (D7.8, M24) Both workshops were performed in combination with a larger workshop, international conference or trade fair that attract a wide audience in the field. In addition, a final workshop will be organized at the end of the project. It will be combined with a presentation of the main scientific results obtained from the E^{2}SWITCH project including prototypes and devices.

The **1st workshop** of the E^{2}SWITCH project entitled "**In the Quest of Zero Power: Energy Efficient Computing Devices and Circuits**" was held on **September 26th, 2014** in **Venice** as satellite event to the international conference **ESSDERC/ESSCIRC 2014**. It was conducted as a scientific dissemination, networking and exploitation event of the E2SWITCH project at the end of the 1st year of work.

The workshop included a series of presentations dealing with state of the art advancements in Tunnel FETs as most promising energy efficient device candidates able to reduce the voltage supply of integrated circuits (ICs) below 0.25V and be hybridized with CMOS technology. It also served as a platform for the discussion of suitable exploitation tracks for the technique.

The programme featured focused reports on DC/AC benchmarking for complementary n- and p-type Tunnel FETs, compact models for digital and analog/RF, device scalability, operational reliability and ITRS metrics. The international keynote invited speakers from USA (prof. Alan Seabaugh) and France (Dr. Francis Balestra and Dr. Costin Anghel) provided vision and opinions from outside the E2-SWITCH Consortium.

The workshop was open to the whole ESSDERC/ESSCIRC audience and to other speakers who attended only the workshop day; the profile of the 25 registrants was very diverse, ranging from PhD students and researchers to industry representatives from both the consortium and the public.

Overall, the different presentations and interactions pointed out the importance and the significant advancement made by the Tunnel FET technology in the last year and its importance as one of the very few device candidates that can offer added value to the well established advanced silicon CMOS.

The 2nd workshop of the E^{2}SWITCH project entitled "**Steep Transistors Workshop**" was held at the **University of Notre Dame, Notre Dame, IN, October 5-6, 2015**.

As part of the dissemination activities of the E^{2}SWITCH consortium an International Workshop on Steep Slope Transistors was arranged on Oct 5-6, 2015, at University of Notre Dame, USA. The workshop was a co-arrangement between the European E^{2}SWITCH consortium and the US sister organization, LEAST (Low-Energy System Technology). The workshop was co-arranged by Prof. A. Seabaugh at University of Notre Dame and Prof. L.-E. Wernersson at Lund University, who also act as Dissemination Manager for E^{2}SWITCH. It was decided to host the workshop in the US to warrant a high participation from the US side as this increased the visibility in the US for the European effort. The workshop was by invitation only, whereas a few, mainly US, PhD-students also attended.

In total 95 participants attended estimated to be about 80% of all active professors in the field, demonstrating the great interest for the workshop. The major contributions were from the US LEAST center and the E^{2}SWITCH consortium, but the workshop was open for international contributions as well and in total 38 labs were represented. Industry participation was notable with participation from Intel, Toshiba, Texas Instruments, Taiwan Semiconductor Manufacturing Company (TSMC), Cambridge CMOS Sensors, IBM (US), IBM (Europe), and GlobalFoundries. Both Teledyne and Raytheon unfortunately had to cancel at the last minute, but showed strong interest.

The workshop was divided into different sections with speakers giving 10 min focussed talks on their respective topic of interest. Since the audience knows the field and most of the work at the different groups,

no introductions were needed, but we focussed on the key aspects. From the E²SWITCH consortium the following talks were given:

Table 2. Presentations at the 2nd E²SWITCH workshop entitled "Steep Transistors Workshop", University of Notre Dame, USA (October 5-6, 2015).

Speaker	Title of the talk
Prof. A. Ionescu	Functional diversification with TunnelFETs
Prof.. S. Mantl	TFETs for ultra low power
Prof. E. Gnani	Stress: performance booster or killer for III-V-based NW TFETs?
Prof. D. Esseni	Off-State behavior for MOSFETs and Tunnel FETs approaching 10nm gate length
Dr. H. Riel	Where are we with TFETs?
Prof. L.-E. Wernersson	Nanowire Tunnel FETs: Axial or Radial TFETs?
Dr. F. Chowdhury	Benchmarking of TFET Analog Circuits: The Sensor Applications Perspective

Besides the scientific and technical presentations, we arranged 5 discussion sessions were moderators were given questions that were addressed by two selected speakers from the participants. These moderators and speakers were selected to balance the efforts within the two host organisations that is the US and the European participants. The discussed topics included the Channel Materials, the Fundamental Understanding, Gate Geometry and Gate Stack, Alternative Mechanisms for Steep Transistors, and Accelerating the development of steep transistors. During these sessions we had a vivid discussion on the topics with the goals to pin-point the critical questions in the field of TunnelFETs. Looking at the device structure with many eyes with different backgrounds helped to get a clearer picture on the perspective on the field.

The workshop will be summarized in a short position document that is currently under writing. Generally we can conclude that there is a strong interest in realizing transistors that operate with high performance at 300 mV or below. The TunnelFET is generally believed to be the leading contender among the device structures. In the US, much effort is directed to implement TunnelFETs in Transition Metal Dichalcogenide (TMD) materials, whereas the European efforts are based on Si- and III-V devices, in line with efforts in Asia. The rationale for the US effort has been based on a strategy decision within the funding bodies (Semiconductor Research Corporation, SRC) where industry wanted to focus on TMDs. It appears that that this strategy now will change and it may open for efforts in Si and III-V materials also in the US again.

On the technical side there is still a gap between the performance predicted by simulations and the experimental results. It appears that the modelling is expected to quite well capture the essence of the device structure and the tunnelling mechanisms. However, the experimental implementations need further development both related to the geometrical sizes and the influence of the defects on the transistor properties. Many implementations are based on comparably thick body devices were the electrostatics are not ideal. The transistor is sensitive to the exact doping levels, for instance in the source region, as well as the presence of defects at the very local region of tunnelling. These are issues that the scientific community as well as the members of the E²SWITCH consortium will need to address in the future. They were well in line with the current project plan of E²SWITCH.

All the information about past or future workshop co-organized by the E²SWITCH project is available online on the project workshops webpage: http://e2switch.org/output/workshops/

The consortium will also maintain or establish links for fruitful exchanges and collaborations with other European and global initiatives with scientific relevance to E²SWITCH. Potential conflict with intellectual property protection and exploitation of project results will be carefully evaluated before publication of results. All scientific communications will be summarized in the present PUDF (D7.6, D7.7, final report).

2.2 PUDF page of the E²SWITCH website

In addition to the present PUDF that allows reporting the project's dissemination activities to the EC, all dissemination activities also have to be reported to the Consortium for approval.

As part of the project e-tools, the members section of the project website includes a PUDF page (http://www.e2switch.org/members/pudf/index.php) displaying the approval procedure for any dissemination activities as defined in the project consortium agreement [2] and reminding the acknowledgement of funding rules defined in the project management guidelines [3].

The PUDF page also provides the partners with an online tool to notify, request approval and report a dissemination activity within the consortium.

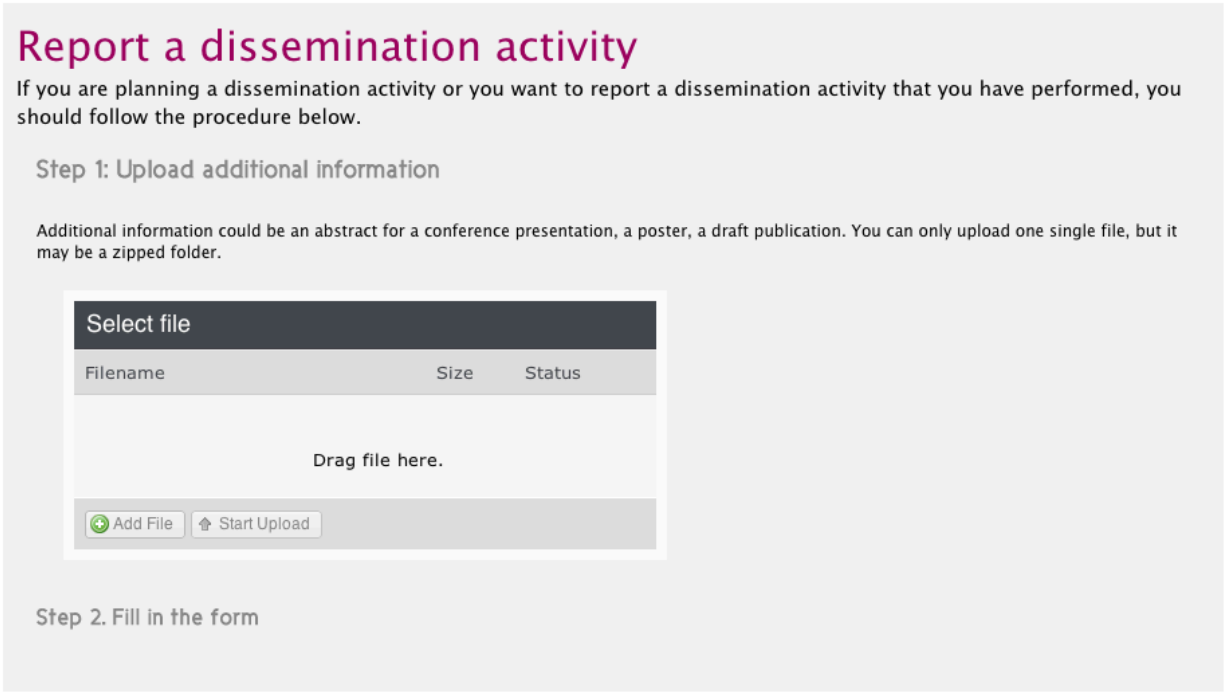
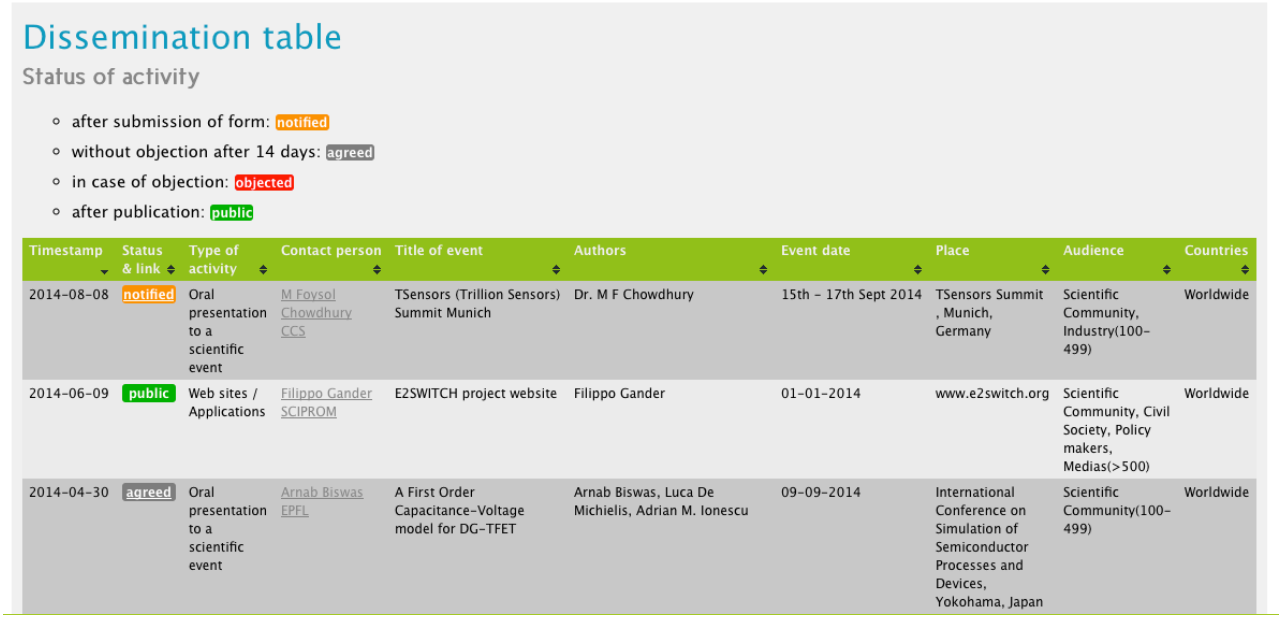


Fig. 2. Dissemination activity submission interface.

Finally, it gives an overview of the dissemination activities within the consortium along with their current status and a link to the corresponding file



Timestamp	Status & link	Type of activity	Contact person	Title of event	Authors	Event date	Place	Audience	Countries
2014-08-08	notified	Oral presentation to a scientific event	M Foysol Chowdhury CCS	TSensors (Trillion Sensors) Summit Munich	Dr. M F Chowdhury	15th - 17th Sept 2014	TSensors Summit , Munich, Germany	Scientific Community, Industry(100-499)	Worldwide
2014-06-09	public	Web sites / Applications	Filippo Gander SCIPROM	E2SWITCH project website	Filippo Gander	01-01-2014	www.e2switch.org	Scientific Community, Civil Society, Policy makers, Medias(>500)	Worldwide
2014-04-30	agreed	Oral presentation to a scientific event	Arnab Biswas EPFL	A First Order Capacitance-Voltage model for DG-TFET	Arnab Biswas, Luca De Michielis, Adrian M. Ionescu	09-09-2014	International Conference on Simulation of Semiconductor Processes and Devices, Yokohama, Japan	Scientific Community(100-499)	Worldwide

Fig. 3. Screenshot of partial dissemination table, showing the layout and colour coding of status as applied.

2.3 Update on the planned dissemination activities for the next period M25-M42

During the period of M25-M42 we plan to continue the dissemination activities according to the original plan described in Section 2.3. In particular, we intend to continue the effort to publish in leading journal and at key conferences following the track-record of the first two years and targeting the same journals and conferences listed in the DoW. We anticipate an even increasing publication effort as results typically are generated towards the end of a project. Currently, there are three upcoming presentations to scientific events (Table 3).

Table 3. List of planned presentations to scientific events (status: 23 November 2015).

No	Title	Main author(s)	Name and location of the event	Date
1	'Presentation of TFET work on InAs/Si TFETs '	K. Moselund, D. Cutaia, M. Borg, H. Schmid and H. Riel	QCom Workshop	31/11/2015
2	InAs-GaSb/Si Heterojunction Tunnel MOSFETs: An Alternative to TFETsas Energy-Efficient Switches?	Hamilton Carrillo-Nunez, Mathieu Luisier, Andreas Schenk	IEDM Washington	08/12/2015
3	International Electron Devices Meeting (IEDM)	J. Cao, D. Logoteta, S. Ozkaya, B. Biel, A. Cresti, M.G. Pala, and D. Esseni	IEDM in Washington D.C.	07/12/2015
4	Novel SiGe/Si line tunneling TFET with high Ion at low VDD and constant SS	S. Blaeser, S. Glass, C. Schulte-Braucks, K. Narimani, N. v. d. Driesch, S. Wirths, A. T. Tiedemann, S. Trellenkamp, D. Buca, Q. T. Zhao, S. Mantl	IEDM 2015 Washington	07/12/2015

We will continue to update and maintain the website with relevant news from the E^{2}SWITCH consortium and present scientific highlights as they develop within the project.

We intend to arrange at least one international workshop in the period of M25-M42. Based on the success of the International workshop on Steep Slope Transistors (described in Section 2.3) and the international interest in the field, we plan to arrange a follow up workshop in Europe during the period coordinated from LUND. We also aim for a final workshop at the end of the project aiming at presenting the general results of E^{2}SWITCH to a wider audience of stakeholders, including both academia and industry. It is at this stage not clear if these two events will be separate or if they will be combined. The consortium will discuss and decide in the period of M25-M32.

3 Exploitable knowledge and its use

Key exploitation will focus on energy efficient electronics for sensors in consumer and automotive industry to guarantee early awareness of the industrial potential originating from the technology and knowledge generated by the project. Furthermore, it will pursue the exploitation of project results by generating IP, device and technology know how.

This Section specifies the exploitable foreground and provides the plans for exploitation.

A summary of the expected exploitable results will be given in Table B.2.1. The template for the exploitation tables are presented in Section 4. The applications for patents, trademarks, registered designs, etc. will be listed in Table B.1.

Exploitable results will then be characterised in more detail in tables B2.2 of the final PUDF.

The **exploitation manager (Foysol Chowdhury, CCS) with the help of EPFL** will overlook the project's exploitation based on all E2SWITCH findings as agreed by all partners.

3.1 Planned exploitation activities

3.1.1 Outline Exploitation Plan

A plan for the exploitation strategy incorporating key deliverables and milestones is given below.

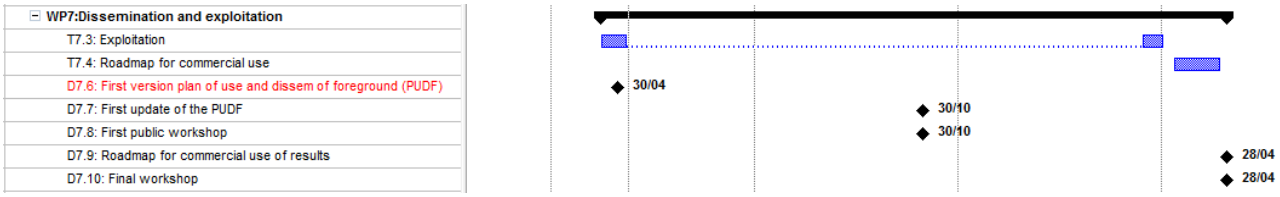


Fig. 4. Exploitation strategy correlation with WP7 deliverables and milestones

3.1.2 Outline Exploitation Roadmap

The first Consortium exploitation roadmap has been drafted by CCS and discussed with the E^{2}SWITCH members. The exploitation roadmap takes into account the R&D nature of this project and is divided into three phases; (1) R&D, (2) Engineering and (3) Production phase.

The exploitation starts from the novel models and device technologies that are currently developed in the project and is considering them as key circuit blocks allowing the achievement of digital and analog circuit functions. An engineering phase is planned after mid-2017, based on the validated IC blocks based on Tunnel FETs on the two platforms (SiGe and III-V) available in the Consortium. The engineering phase will also realistically consider implementation in two-die solutions, combining mature CMOS design with Tunnel FET circuits, according to the specifications for Internet-Of-Things (IoT) and automotive applications that can benefit from the low power consumption and reduced temperature drift of the new technology.

The Consortium will be proactive in producing patents when possible and seize opportunities on the markets, including partnerships with end-users beyond the lifetime of the project.

The risks associated with this exploitation roadmap are related to the achievements of the final figures of merit of Tunnel FET circuits but also, especially, to the reliability, robustness and cost of the IC implemented in the new technology.

The reliability will be partially addressed in the characterization workpackage, as an additional activity, supporting the potential exploitation. We will particularly try to apply and adapt traditional CMOS reliability test for digital circuit and study the behaviour of the devices and circuits over ranges of temperatures corresponding to industrial applications.

The cost risk is mitigated by the fact that the Consortium approach is to integrated Tunnel FETs on advanced CMOS platforms; therefore, at long term Tunnel FET should become just a design option into existing CMOS libraries. This is expected to reduce high additional costs.

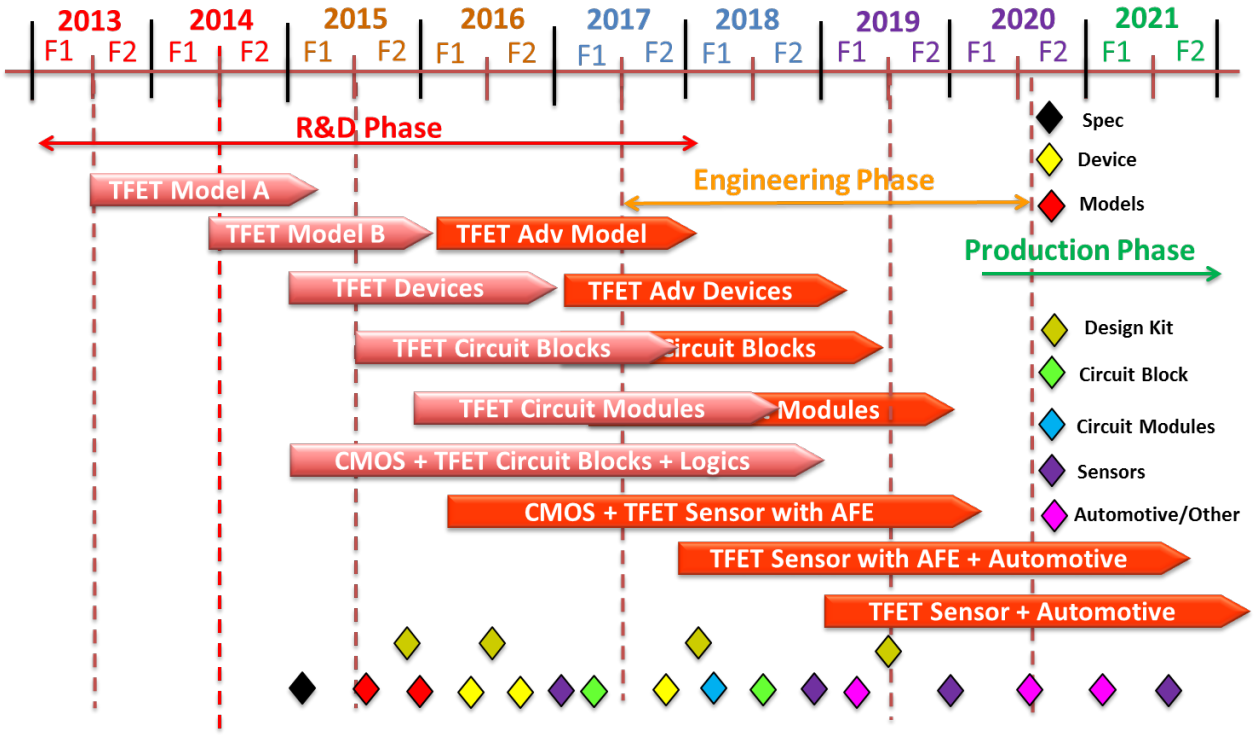


Fig. 5. Initial E[2]SWITCH exploitation roadmap.

The process and technology roadmap proposed in Figure 5, was considered to be highly optimistic and it was felt that TFET technology in terms of material selection and finalising the device structure will time to evolve and R&D phase could go beyond 2020. The engineering phase will then follow for at least 2 years, after 2022 production phase could begin as show in the revise roadmap in Figure 6.

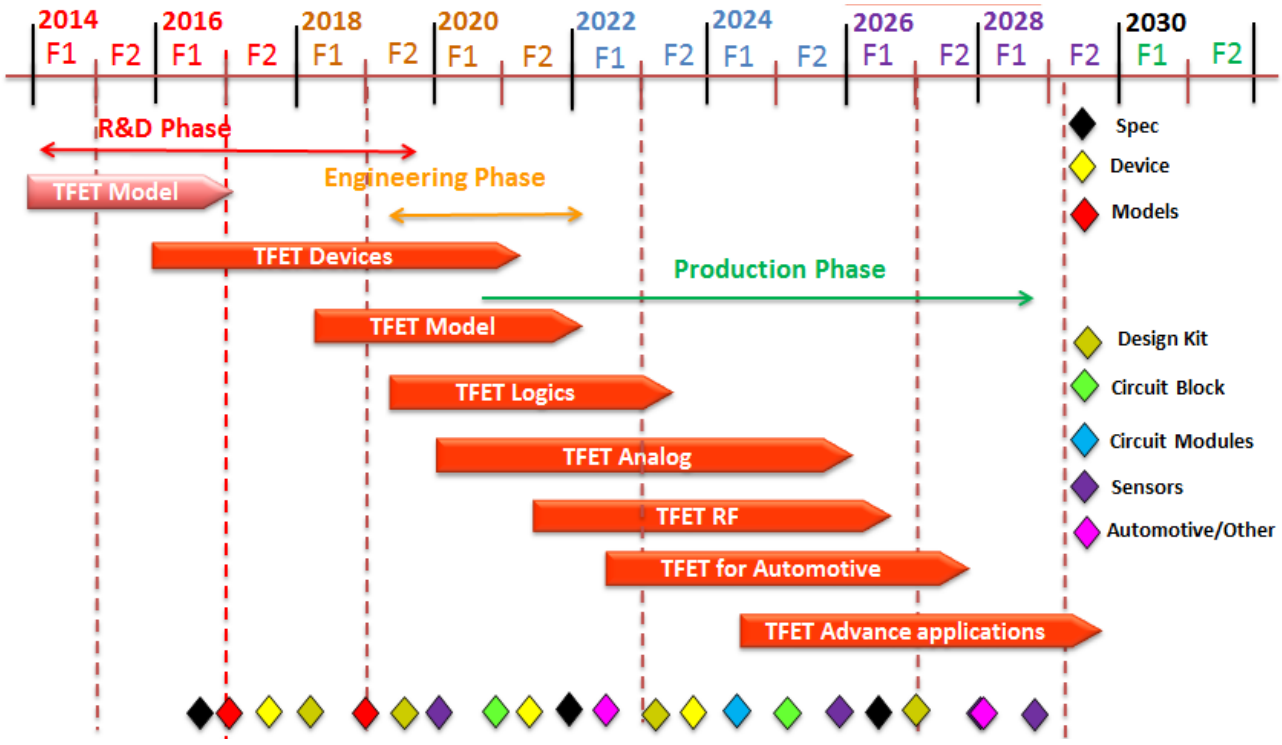


Fig. 6. E[2]SWITCH technology exploitation revised roadmap.

3.1.2.1 Device/Technology Roadmap

Figure 7, shows a possible device/technology roadmap. As can be seen, there are many options available and success will depend on how easily processes and appropriate tooling can be developed for high volume commercial manufacturing.

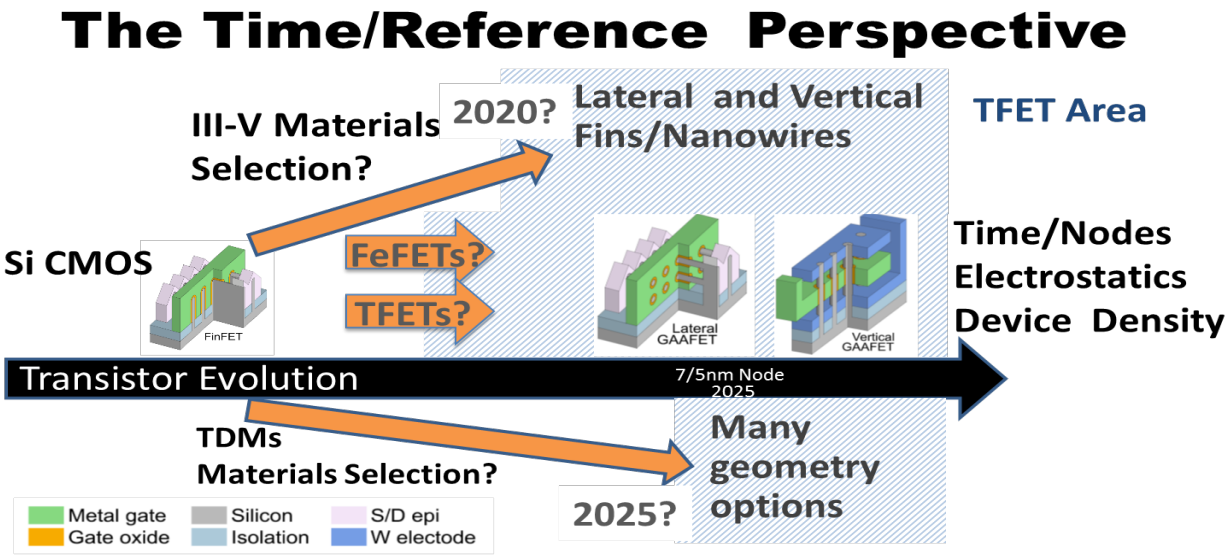


Fig. 7. E^{2}SWITCH Device and technology roadmap.

Gradual transition from FinFET device options to TFET is shown in Figure 8.

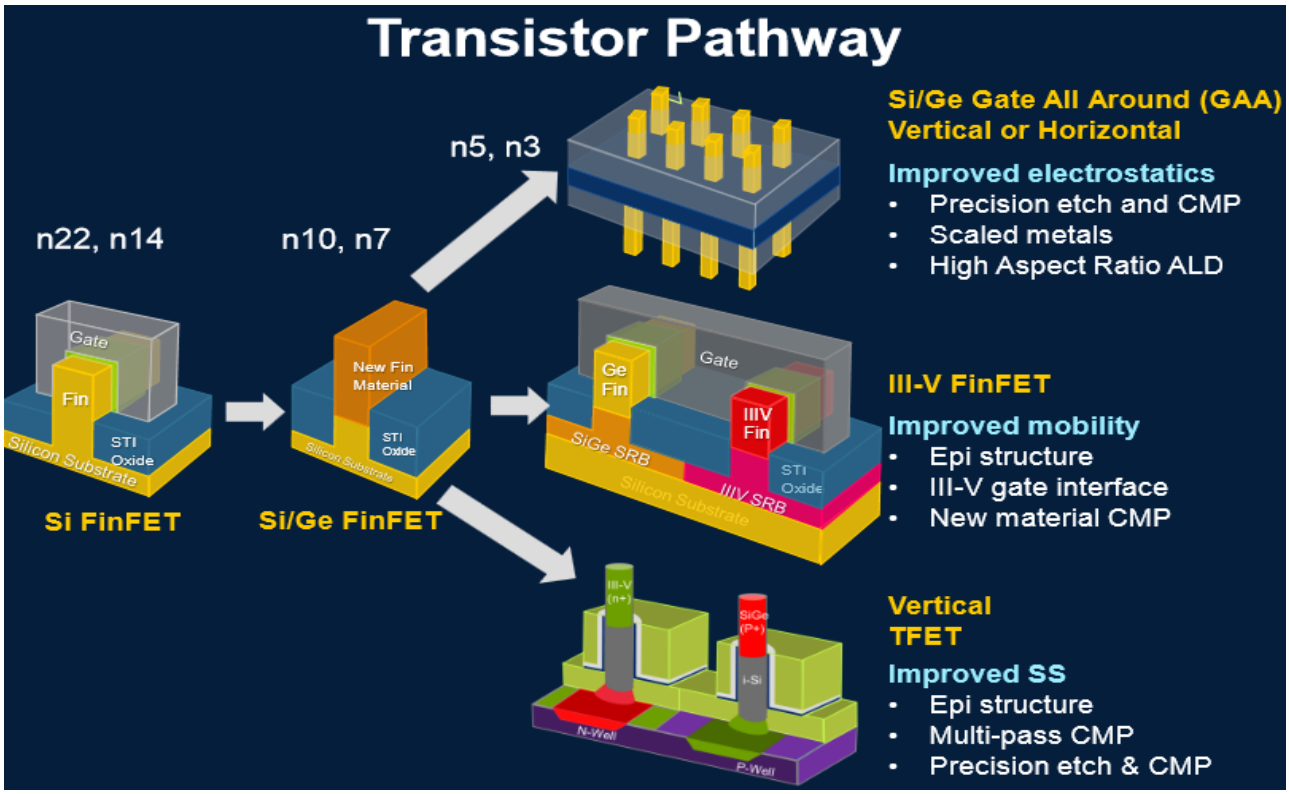


Fig. 8. E^{2}SWITCH Device and technology options.

3.1.2.2 *Application Roadmap*

Examples of Samsung's perception of technology and application areas are show in Figure 9, here the main driving factors are performance and low power consumption. Based in this, a similar roadmap can be determined, where key barrier is technology – this is what E2SWITCH project is aiming to contribute in finding solutions.

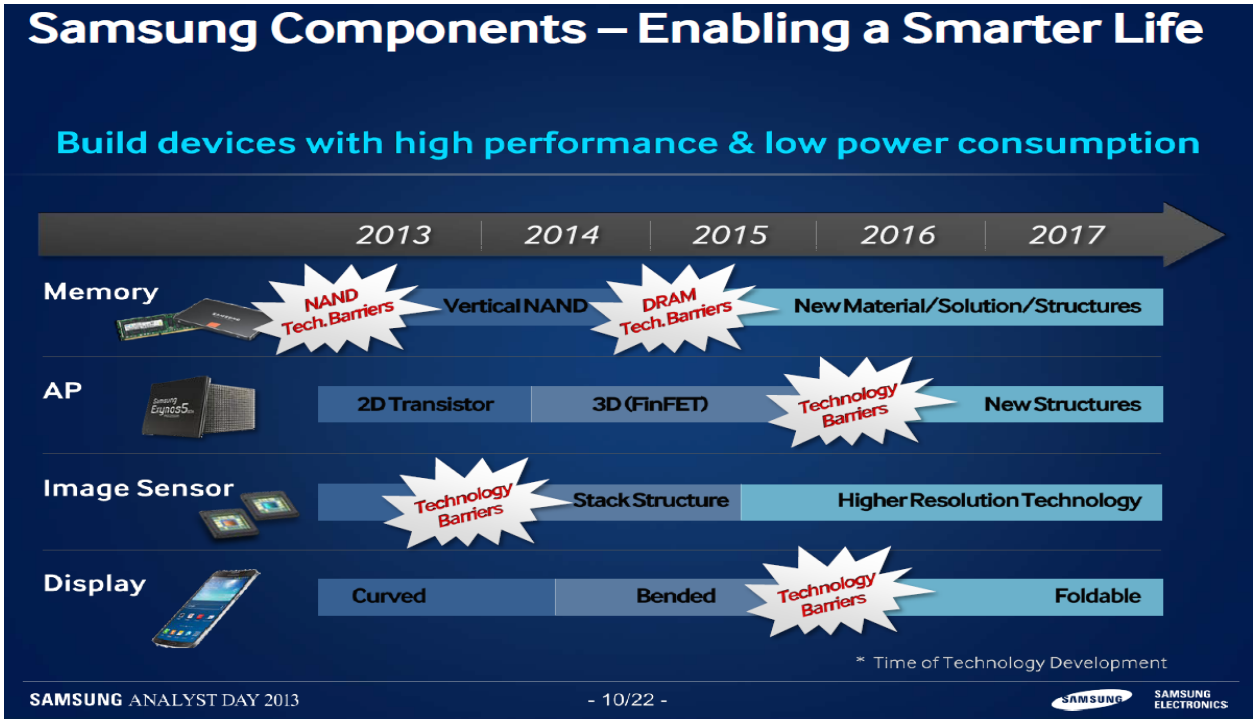


Fig. 9. Example of high volume application beyond CMOS technology and barriers

Figure 10, shows that 1st Gen, FinFET devices are in commercial production with 0.8V supply voltage, and 2nd generation will follow 0.7V. Beyond this point TFET devices operated below 0.7V, will help to push technology to overcome the barrier. At present there are 1 billion transistors per person!

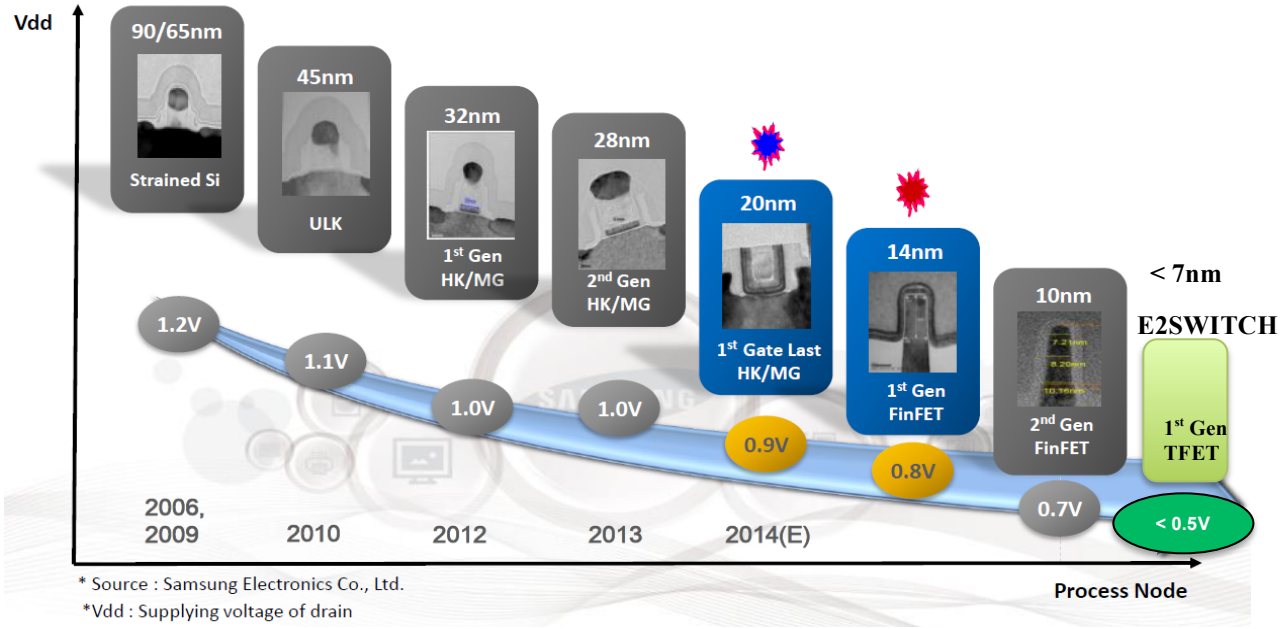


Fig. 10. Example of technology barriers E2SWITCH is aiming to solve

3.1.2.3 Low power sensor roadmap

One of the biggest areas where TFET solutions will benefit is the low power sensors for IoT applications, and based on this, nice summary of the power requirement roadmap is shown in Figure 11. With low power sensing solutions, it will also enable wider exploitation of energy-harvested sensing applications.

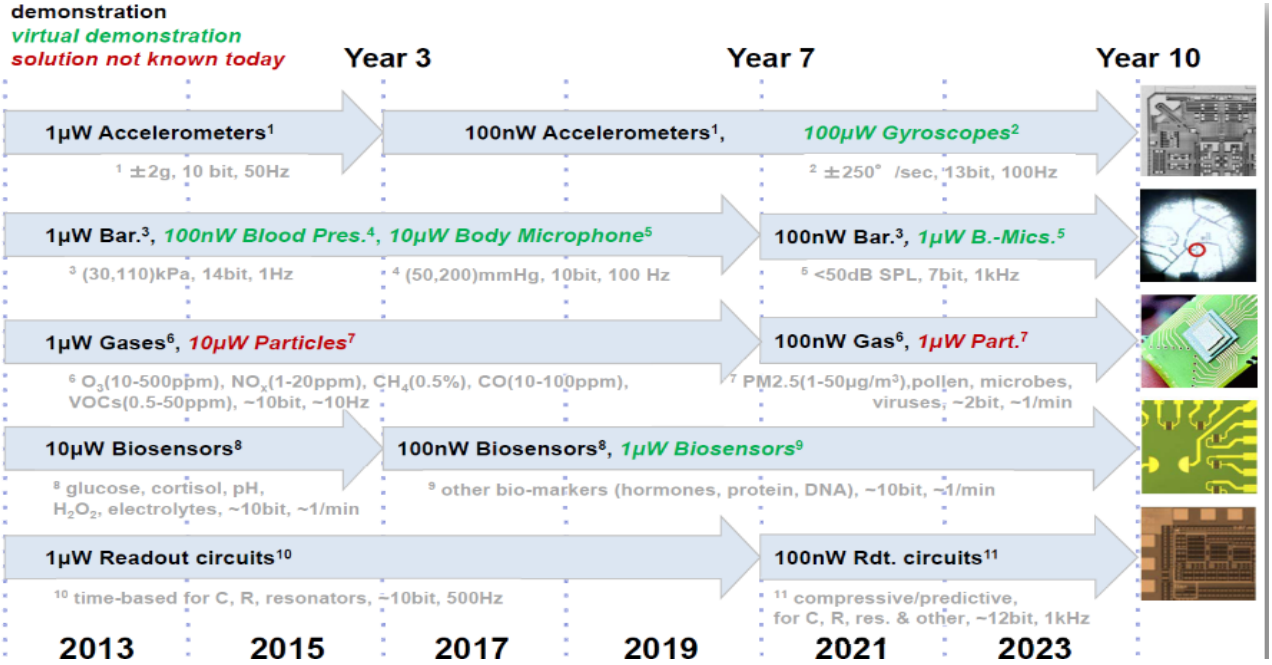
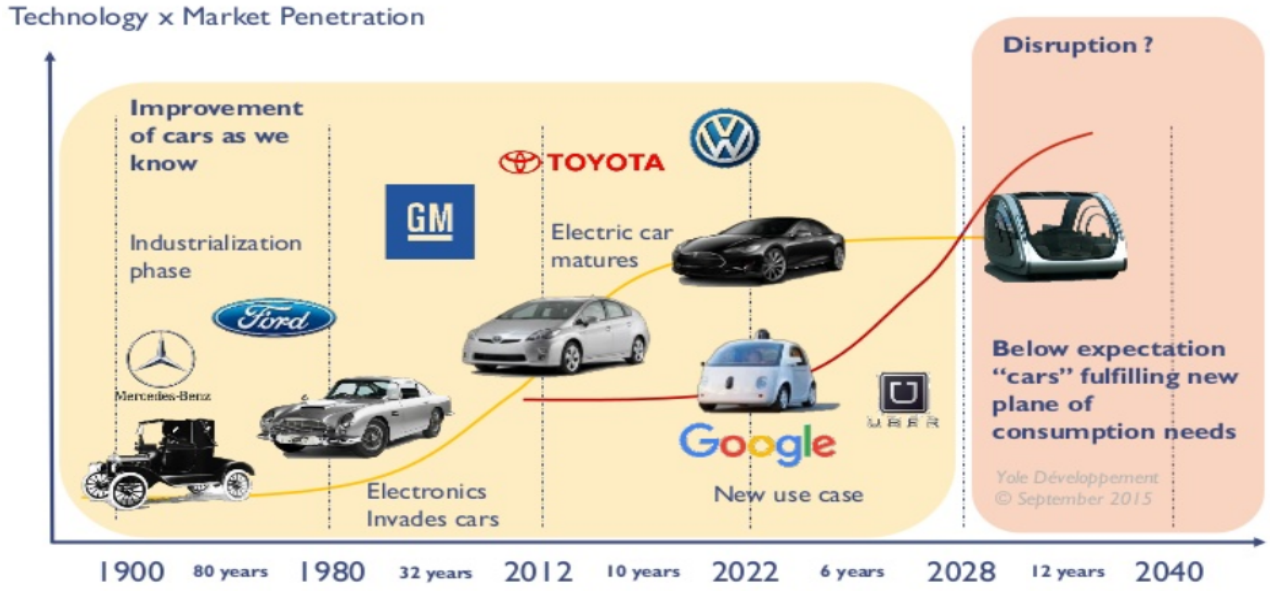


Fig. 11. Drive for low power sensors

3.1.2.4 Automotive application roadmap

It has been estimated that average car contains an average of $300 to $400 worth of electronic devices. With autonomous driver assisted vehicle, demand for low power, high performance electronics will grow. Figure 12a-c summarize some of the key players in this field and market size.

(a)



(b)

(c)

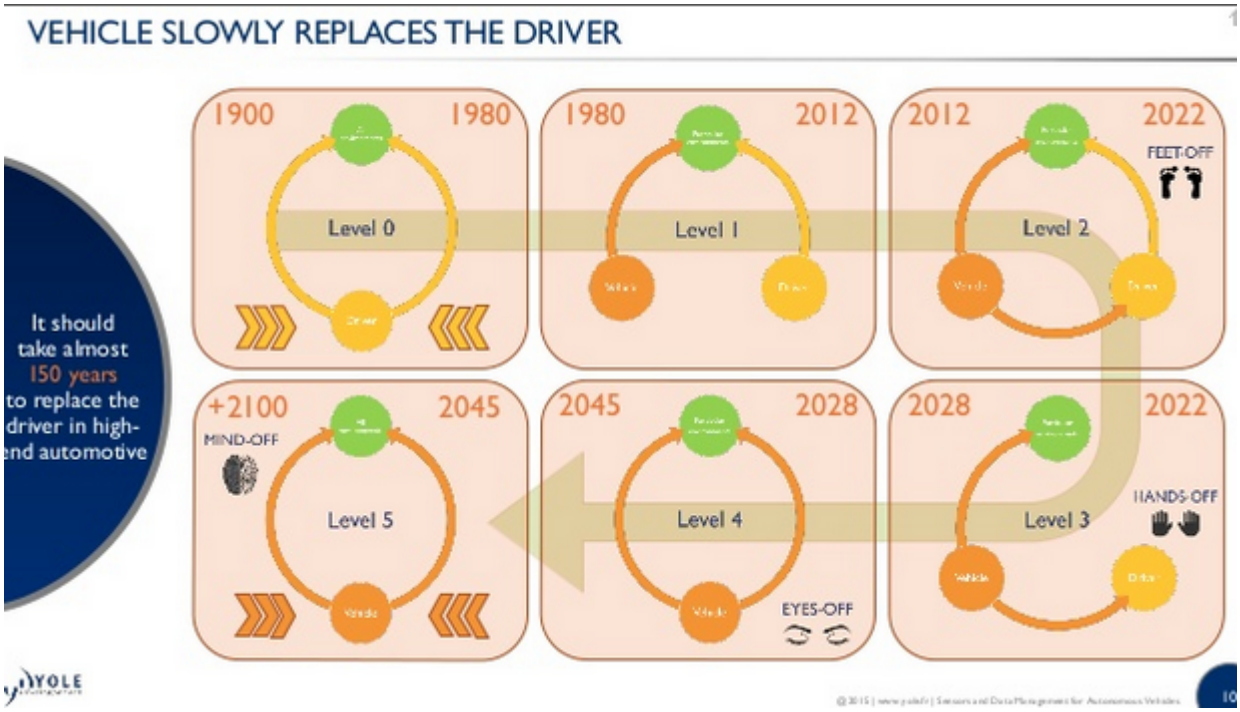


Fig. 12. Automotive applications

3.1.2.5 *Market facts and figures*

Some market facts and figures for semiconductor industry are shown in Figures 13-16.

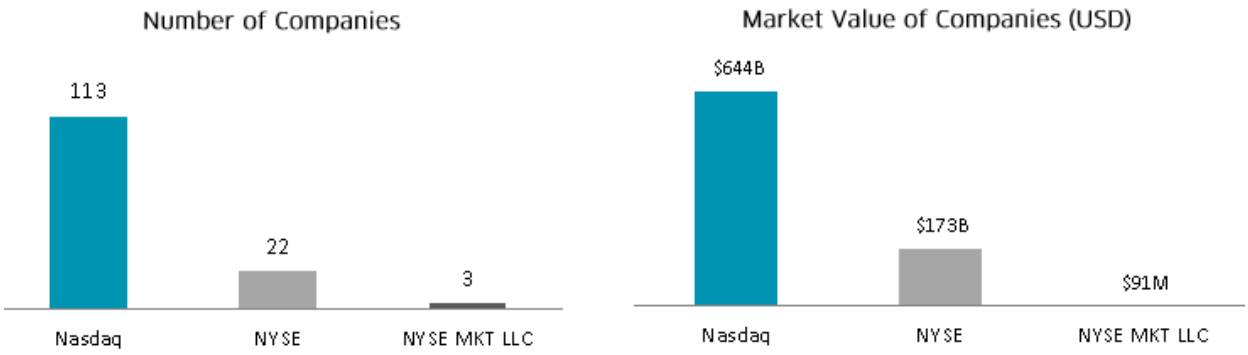


Fig. 13. Global Semiconductor companies and market values (Ref – NASDAQ)

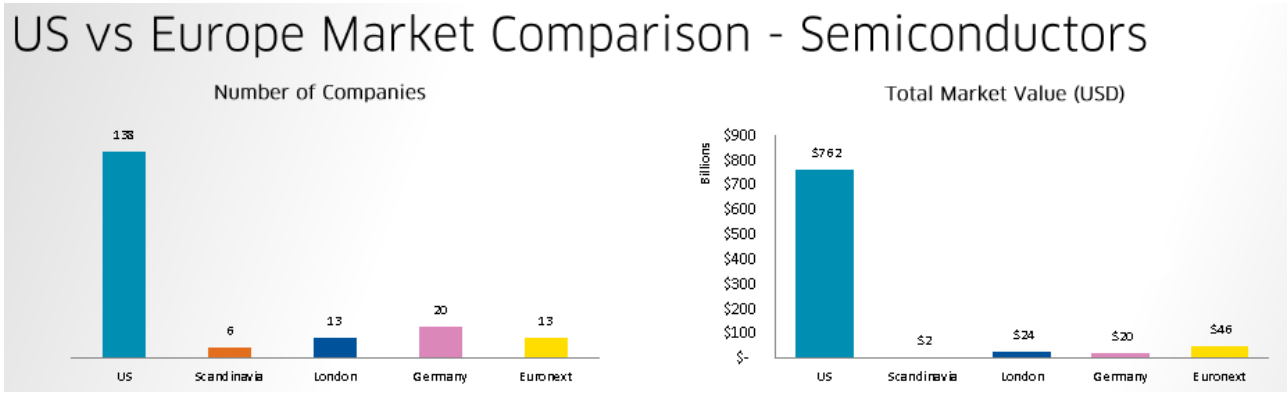


Fig. 14. US vs EU Semiconductor companies and market values (Ref – NASDAQ)

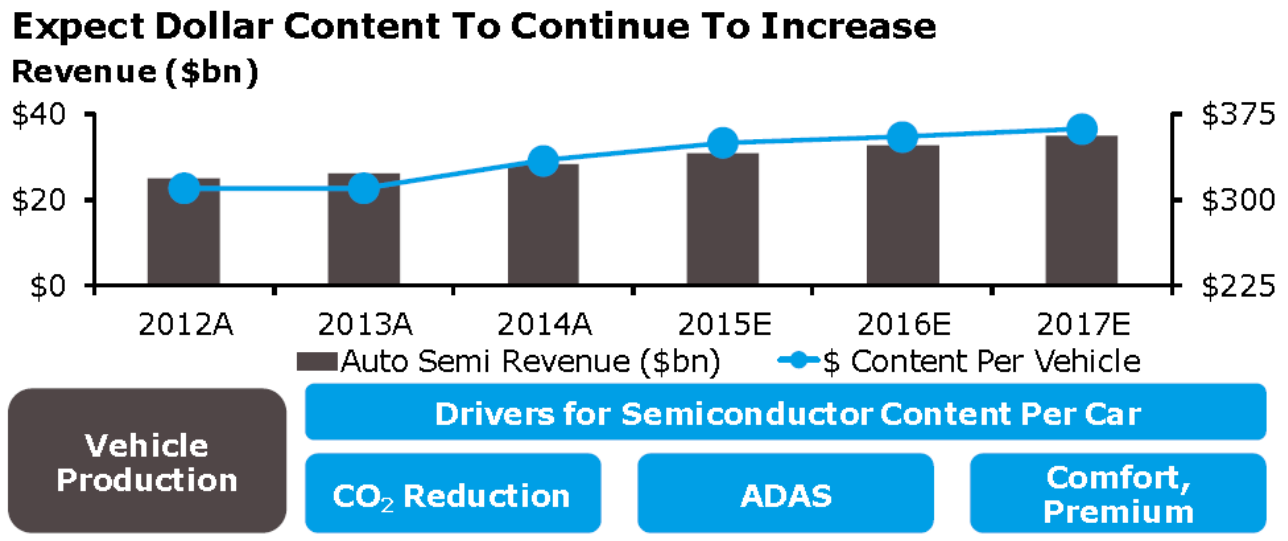
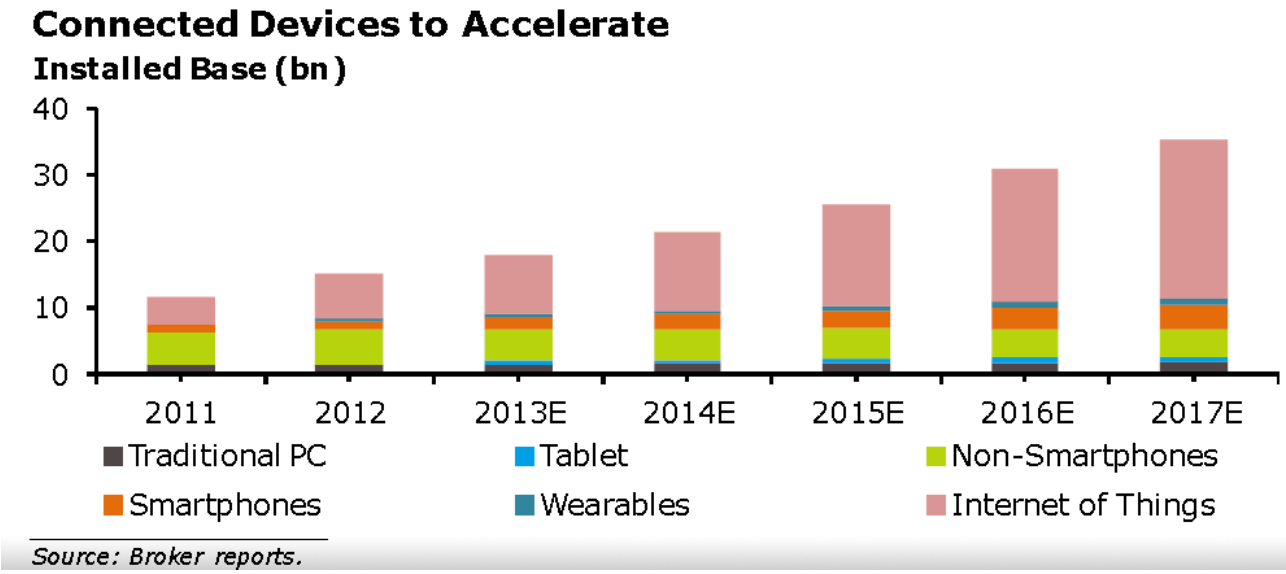


Fig. 15. Key driving factors for semiconductor market: Strong Growth in Automotive; Sector IoT – 50 Billion Connected Devices by 2020; Emergence of Big Data; China Inc. Interested In Semiconductors



Target	Acquirer	Transaction Value(1) ($m)
NXP	建广资产 JAC Capital	$1,800
ISSI	武岳峰资本 SUMMITVIEW CAPITAL	$736
STATSChipPAC	长电科技	$780
OmniVision	华创投资 HUA CAPITAL	$1,670
SPREADTRUM	PDSTI 上海浦东科技投资有限公司	$616
MONTAGE Technology	紫光集团有限公司 TSINGHUA UNIGROUP LTD.	$1,440
RDA	紫光集团有限公司 TSINGHUA UNIGROUP LTD.	$907

Fig. 16. China acquisition – 7 major transactions, more expected

3.1.3 Key Exploitation Areas

There are two areas of exploitations identified by the consortium:

3.1.3.1 Academic partners

- The knowledge and expertise acquired will underpin **further research** by the Universities.
- Strengthen their **competitiveness as higher education institutions** worldwide.
- Initiate **advanced graduate thesis projects** in very appealing and current topics such as “Emerging devices”, “TFET circuit design”.

- Promote students' awareness and their interest in energy efficient electronics and zero-power autonomous systems. The combination of **high-level universities with well-known research institutes and industry** depicts an excellent environment for students and postdoctoral researchers.
- Provide access to advanced technological and computational platforms and enable insight into the scientific and industrial environment.
- Encourage engineers and scientists in Europe to pursue a career in the **field of nanoelectronics**.
- Devise new **practical and theoretical methods and tools** to support **future capabilities.**
- Establish vehicle for **research funding** applications, studentships, doctoral theses, graduate dissertations and undergraduate projects and thus will help European universities to act strong on common performance metric in a competitive international environment.
- A key goal of E^{2}SWITCH is to strengthen the **competitiveness of Europe**.
- Initiate exploitation of the results by transferring technology to industrial partners to ensure rapid spread to European industrial companies.
- Propagate **interactions with international centres of competencies in the field of energy-efficient computing** to global **Stakeholder Forum.**
- Engage with licensing of know-how with industry to trigger further R&D co-operation with European and worldwide industry.

3.1.3.2 Industrial partners

- Identify potential for commercial exploitation in two potentially huge applications - ICT and sensors, incorporating consumer and automotive market sectors.
- Define **future device/technology roadmap** including the design process tools and methodology and **product portfolio**.
- Evaluate power consumption requirements for future Supercomputers to set a timescale for leading-edge power-efficient logic device technology deployment.
- Shortlist possible device technology such as FinFET architectures, nanowires. SiGe or SOI-CMOS channel materials for pFET and III-V for nFETs, leading to TFET as a stand-alone device.
- Identify the requirements for low power smart sensors for portable applications as well as for wireless sensor network applications.
- Investigate the feasibility of using TFET devices for **smart IR and gas sensors** with integrated circuits having extremely low power consumption and on-chip temperature sensing together with analogue readout.
- Establish state-of-the art, IPR protection strategies, the consortium exploitation strategy and including a *detailed market analysis for semiconductor companies*.
- Provide periodic report of the size of potential application markets for Tunnel FET based circuits in: (i) low power electronics for portable systems and (ii) low power smart systems for high temperature sensing, respectively.
- Produce exploitation roadmap and final exploitation plan, as a part of the final PUDF with feedback to consortium and advice from the members of the stakeholder forum.

Based on the above, outline plan for exploitation activities are summarised in Figure 17.

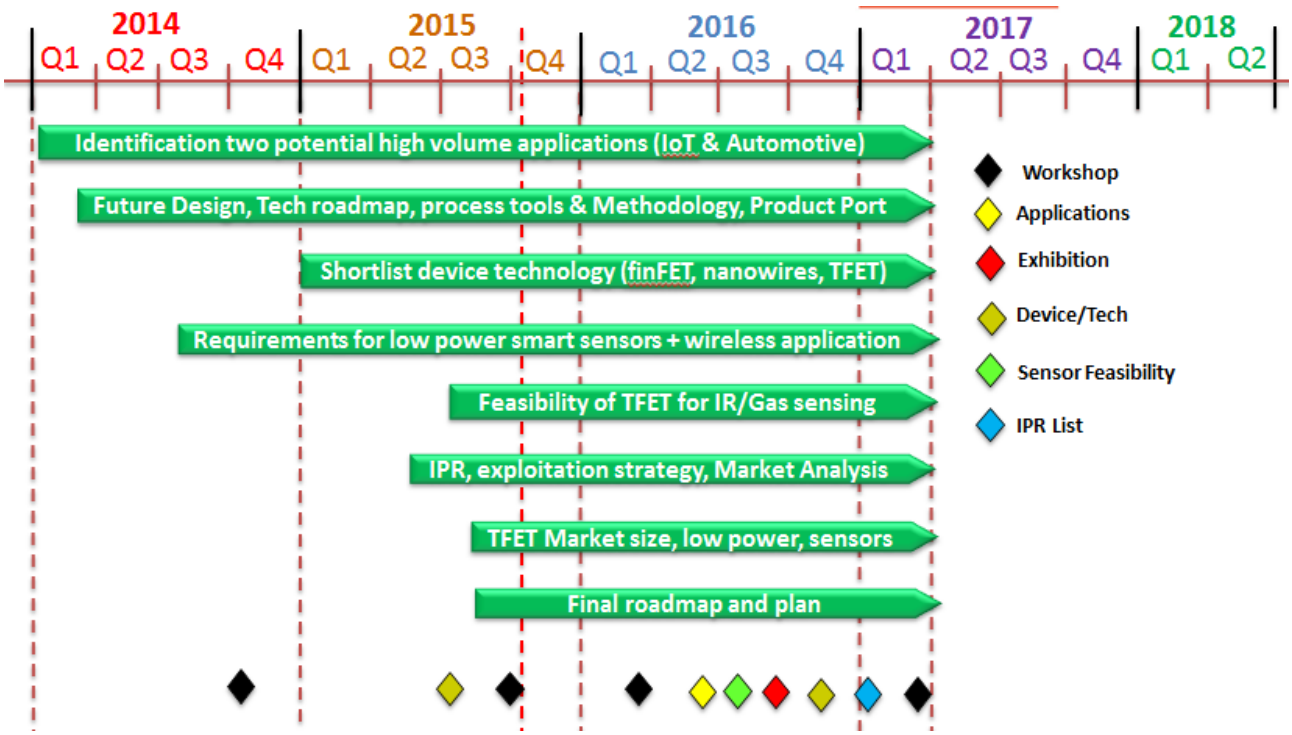


Fig. 17: Outline plan for exploitation activities

Trade fare/Exhibition:

Possible invited talk at: http://www.idtechex.com/energy-harvesting-europe/speakers.asp

This would give an opportunity to promote TFET technology for IoT applications.

3.1.4 Current steps towards successful exploitation of the E²SWITCH results

On 26 September 2014, a **first E²SWITCH workshop** was held in the frame of the ESSDERC conference 2014 in Venice. Involving speakers from the consortium and leading industry, the exploitation of expected E²SWITCH results will be a topic of discussions, centred on an exploitation-focussed keynote and further contributions from industry.

Moreover, details of the E²SWITCH exploitation activities have been discussed **within the consortium** on the basis of the **template table B.2.1** (see Section 4) and the "innovation radar" questionnaires of the first project review.

4 Dissemination and Exploitable knowledge in final PUDF format

In the following the tables used for the final format of the PUDF are shown.

The dissemination related tables A1 and A2 are completed based on the information available on the online PUDF page of the E²SWITCH member section (status 11 November 2015)

A. Dissemination of knowledge (confidential)

A.1 Scientific (peer reviewed) publications

Table A.1. List of scientific (peer reviewed) publications (public). Status 23 November 2015.

No	Title	Authors	Title of the periodical or the series	Volume, pages and year	Publisher	Permanent identifiers (D.O.I)	Open access
1	Vertical III-V Nanowire Device Integration on Si(100)	B. Mattias Borg, Heinz Schmid, Kirsten E. Moselund, Giorgio Signorello, Lynne Gignac, John Bruley, Chris Breslin, Pratyush das Kanungo, Peter Werner, Heike Riel	Nano Letters	14 (4), 1914-1920, 2014	ACS	10.1021/nl404743j	No
2	Electron-Hole Bilayer TFET: Experiments and Comments	A. Revelant, A. Villalon, Y. Wu, A. Zaslavsky, C. Le Royer, H. Iwai, S. Cristoloveanu	Transactions on Electron Devices	Vol.61, No. 8, 2674-2681, 2014	IEEE	10.1109/TED.2014.2329551	No
3	Challenges and opportunities in the design of Tunnel FETs: materials, device architectures, and defects	D. Esseni, M.G. Pala, A. Revelant, P. Palestri, L. Selmi, M.(Oscar) Li, G. Snider, D. Jena, H.G. Xing	ECS Transactions	Vol. 64, issue 6, 581-595, 2014	ECS	10.1149/06406.0581ecst	No
4	Pseudopotential calculations of strained-GeSn/SiGeSn hetero-structures	Saurabh Sant and Andreas Schenk	Appl. Phys. Lett.	105, 162101, , 2014	AIP	10.1063/1.4898676	No
5	Vertical InAs-Si Gate-All-Around Tunnel FETs Integrated on Si Using Selective Epitaxy in Nanotube Templates	D.Cutaia, K.E.Moselund, M.Borg, H.Schmid, L.Gignac, C.M.Breslin, S.Karg, E.Uccelli, H.Riel	Journal of Electron Device Society (J-EDS)	Vol. 3, Issue 3, 176 - 183, 2015	IEEE	10.1109/JEDS.2015.2388793	No
6	Impact of TFET Unidirectionality and Ambipolarity on the Performance of 6T SRAM Cells	S. Strangio, P. Palestri, D. Esseni, L. Selmi, F. Crupi, S. Richter, Q. T. Zhao and S. Mantl	Journal of Electron Device Society (J-EDS)	Vol. 3, Issue 3, 223-232, 2015	IEEE	10.1109/JEDS.2015.2392793	No
7	Strained Si and SiGe Nanowire Tunnel FETs for Logic and Analog Applications	Q. T. Zhao, S. Richter, C. Schulte-Braucks, L. Knoll, S. Blaeser, G.V. Luong, S. Trellenkamp, A. Schäfer, A. Tiedemann, K. K. Bourdelle, S. Mantl	J. Electronic Devices Society	Vol. 3, Issue 3, 103-114, 2014	IEEE	10.1109/JEDS.2015.2400371	No
8	Lasing in direct bandgap GeSn alloy grown on Si	S. Wirths, S. Mantl, D.Buca, et al.	Nature Photonics	Vol 9, 88-92, 2015	Nature	10.1038/nphoton.2014.321	No
9	Experimental demonstration of planar SiGe on Si TFETs with counter doped pocket	S. Blaeser, S.Richter, S. Wirths, S. Trellenkamp, D. Buca, Q. T. Zhao, S. Mantl	EUROSOI-ULIS 2015	297-300, 2015	IEEE	10.1109/ULIS.2015.7063832	No
10	Strained Si nanowire GAA n-TFETs for low supply voltages	G.V.Luobg, S. Trellenkamp, K.K. Bourdelle, Q. T. Zhao, S. Mantl	EUROSOI-ULIS 2015	65-68, 2015	IEEE	10.1109/ULIS.2015.7063774	No
11	III-V Nanowire CMOS Monolithically Integrated on Si	Johannes Svensson, Anil Dey, Daniel Jacobson, Lars-Erik Wernersson	Nano research	Vol 7 Issue 12, 1769-1776, 2015	Tsinghua University Press	10.1007/s12274-014-0536-6	No
12	Analysis of InAs-Si Heterojunction Nanowire Tunnel FETs: Extreme	Hamilton Carrillo-Nunez, Mathieu Luisier, Andreas Schenk	Solid State Device Research	2014 44th, 118-119, 2015	IEEE	10.1109/ESSDERC.2014.6948772	No

No	Title	Authors	Title of the periodical or the series	Volume, pages and year	Publisher	Permanent identifiers (D.O.I)	Open access
	Confinement vs. Bulk		Conference (ESSDERC), European				
13	Modeling direct band-to-band tunneling: from bulk to quantum-confined semiconductor devices	Hamilton Carrillo-Nunez, Anne Ziegler, Mathieu Luisier, Andreas Schenk	Journal of Applied Physics	117, 234501_1-10, 2015	AIP	10.1063/1.4922427	No
14	Negative differential resistance in direct bandgap GeSn p-i-n structures	C. Schulte-Braucks, et al.,	Journal of Applied Physics	117, 2015	AIP	10.1063/1.4927622	No
15	Ternary and quaternary Ni(Si)Ge(Sn) contact formation for highly strained Ge p- and n- MOSFETs	S. Wirths et al.,	Semiconductor Science and technology	Vol 30 Issue 5, , 2015	IOP		No
16	High-k Gate Stacks on Low Bandgap Tensile Strained Ge and GeSn Alloys for Field-E□ect Transistors	S. Wirths et al.,	Applied Materials & Interfaces	Vol 7 Issue 1, 62-67, 2014	ACS	10.1021/am5075248	No
17	Vertical InAs-Si Gate-All-Around Tunnel FETs Integrated on Si Using Selective Epitaxy in Nanotube Templates	D.Cutaia, K.E.Moselund, M.Borg, H.Schmid, L.Gignac, C.M.Breslin, S.Karg, E.Uccelli, H.Riel	Journal of Electron Device Society, 2015	Vol 3 Issue 3, 176-183, 2015	IEEE	10.1109/JEDS.2015.2388793	No
18	Efficient quantum mechanical simulation of band-to-band tunneling	Cem Alper, Pierpaolo Palestri, Jose L Padilla, Antonio Gnudi, Roberto Grassi, Elena Gnani, Mathieu Luisier, Adrian M Ionescu,	EUROSOI-ULIS 2015	141-144, 2015	IEEE	10.1109/ULIS.2015.7063793	No
19	Modeling the Imaginary Branch in III-V Tunneling Devices: Effective Mass vs k · p	Cem Alper , Michele Visciarelli, Pierpaolo Palestri, Jose L. Padilla , Antonio Gnudi, Elena Gnani, Adrian M. Ionescu	SISPAD 2015, Washington D.C.	273-276, 2015	IEEE	10.1109/SISPAD.2015.7292312	No
20	Impact of TFET Unidirectionality and Ambipolarity on the Performance of 6T SRAM Cells	Sebastiano Strangio, Pierpaolo Palestri, David Esseni, Luca Selmi, Felice Crupi, Simon Richter, Qing-Tai Zhao, Siegfried Mantl	Journal of the Electron Devices Society	Vol 3 Issue 3, 223-232, 2015	IEEE	10.1109/JEDS.2015.2392793	No
21	Two dimensional quantum mechanical simulation of lowdimensional tunneling devices	C. Alper, P. Palestri, L. Lattanzio, J.L. Padilla, A.M. Ionescu	Solid-State Electronics	Vol 113, 167-172, 2015	Elsevier	10.1016/j.sse.2015.05.030	No
22	Capacitance estimation for InAs Tunnel FETs by means of full-quantum k·p simulation. Solid-State Electronics.	Baravelli E., Gnani E., Gnudi A., Reggiani S., Baccarani, G.	ULIS Conference Paper	Vol 108, 104-109, 2015	Elsevier	10.1016/j.sse.2014.12.005	No
23	Essential Physics of the OFF-State Current in Nanoscale MOSFETs and Tunnel FETs	Esseni, D.; Pala, M.G.; Rollo, T.,	IEEE Transactions on Electron Devices	Vol. 62, n. 9, 3084-3091, 2015	IEEE	10.1109/TED.2015.2458171	No
24	Mixed Tunnel-FET/MOSFET Level Shifters: a new proposal to extend the Tunnel-FET application domain	M. Lanuzza, S. Strangio, F. Crupi, P. Palestri, D. Esseni	IEEE Transactions on Electron Devices	vol.62, no.12, pp.3973-3979, 2015	IEEE	10.1109/TED.2015.2494845	No
25	III–V device integration on Si using template-assisted selective epitaxy	Schmid, H.; Borg, M.; Moselund, K.; Gignac, L.; Breslin, C.; Bruley, J.; Cutaia, D.; Riel, H.	Device Research Conference	vol., no., pp.255-256, 21-24 June	IEEE	10.1109/DRC.2015.7175666	No

No	Title	Authors	Title of the periodical or the series	Volume, pages and year	Publisher	Permanent identifiers (D.O.I)	Open access
			(DRC), 2015 73rd Annual	2015			
26	Band-Offset Engineering for GeSn-SiGeSn Hetero Tunnel FETs and the Role of Strain	Sant, S.; Schenk, A.	Electron Devices Society, IEEE Journal of the	vol.3, no.3, pp.164-175, May 2015	IEEE	10.1109/JEDS.2015.2390971	No
27	A quasi 2D semianalytical model for the potential profile in hetero and homojunction tunnel FETs	Villani, F.; Gnani, E.; Gnudi, A.; Reggiani, S.; Baccarani, G.	Solid State Device Research Conference (ESSDERC), 2014 44th European	pp.262-265, 22-26 Sept. 2014	IEEE	10.1109/ESSDERC.2014.6948810	No
28	Improved Tunnel-FET Inverter Performance with SiGe/Si Heterostructure Nanowire TFETs by Reduction of Ambipolarity	S. Richter, S. Trellenkamp, A. Schäfer, J. M. Hartmann, K. K. Bourdelle, Q. T. Zhao, S. Mantl	Solid-State Electronics	Volume 108, , Pages 97–103, June 2015	Elsevier	doi:10.1016/j.sse.2015.02.018	No
29	Mechanisms of Template-Assisted Selective Epitaxy of InAs nanowires on Si	M. Borg, H. Schmid, K.E. Moselund, D. Cutaia, H. Riel	J. Appl. Phys.	117, 144303 (2015)	AIP Publishing	10.1063/1.4916984	No
30	Template-assisted selective epitaxy of III–V nanoscale devices for co-planar heterogeneous integration with Si	D. Cutaia, K. E. Moselund, M. Borg, H. Schmid, L. Gignac, C.M. Breslin, S. Karg, E. Uccelli, P. Nirmalraj, H. Riel	Appl. Phys. Lett	106, 233101 (2015)	AIP Publishing	10.1063/1.4921962	No
31	Mixed device-circuit simulations of 6T/8T SRAM cells employing tunnel-FETs	S. Strangio, P. Palestri, D. Esseni, L. Selmi, F. Crupi	Gruppo Italiano di Elettronica 47th Annual Meeting, Proceedings of the (GE 2015)	pp. 81-82			Yes
32	Simulation analysis of III-V n-MOSFETs: channel materials, Fermi level pinning and biaxial strain	Enrico Caruso, Daniel Lizzit, Patrik Osgnach, David Esseni, Pierpaolo Palestri, Luca Selmi	Electron Devices Meeting (IEDM), 2014 IEEE International	pp.7.6.1-7.6.4, 15-17 Dec. 2014	IEEE	10.1109/IEDM.2014.7047006	No
33	State-of-the-art semi-classical Monte Carlo method for carrier transport in nanoscale transistors	P. Palestri, E. Caruso, F. Driussi, D. Esseni, D. Lizzit, P. Osgnach, S. Venica, L. Selmi	Information and Communication Technology, Electronics and Microelectronics (MIPRO), 2015 38th International Convention on	pp.1-8, 25-29 May 2015	IEEE	10.1109/MIPRO.2015.7160227	No
34	Modeling the Imaginary Branch in III-V Tunneling Devices: Effective Mass vs k · p	Cem Alper , Michele Visciarelli, Pierpaolo Palestri, Jose L. Padilla , Antonio Gnudi, Elena Gnani, Adrian M. Ionescu	Simulation of Semiconductor Processes and Devices (SISPAD), 2015	pp.273-276, 9-11 Sept. 2015	IEEE	10.1109/SISPAD.2015.7292312	No

No	Title	Authors	Title of the periodical or the series	Volume, pages and year	Publisher	Permanent identifiers (D.O.I)	Open access
			International Conference on				
35	III-V Heterostructure Nanowire Tunnel FETs	Lind, E.; Memisevic, E.; Dey, A.W.; Wernersson, L.-E.	Electron Devices Society, IEEE Journal of the	vol.3, no.3, pp.96-102, May 2015	IEEE	10.1109/JEDS.2015.2388811	Yes
36	Impact of TFET Unidirectionality and Ambipolarity on the Performance of 6T SRAM Cells	Strangio S., Palestri P., Esseni D., Selmi L., Crupi F., Richter S., Zhao Q., Mantl, S., ",	Journal of the Electron Devices Society	n. 3, vol. 3, pag. 223-232, May 2015	IEEE	10.1109/JEDS.2015.2392793	No
37	Thin electron beam defined hydrogen silsesquioxane spacers for vertical nanowire transistors	E. Memisevic, É. Lind, L.-E. Wernersson	J. Vac. Sci. Technol. B	32, 051211 (2014);	AIP Publishing	10.1116/1.4895112	No
38	Narrow Gap Semiconductors: From Nanotechnology to RF-Circuits on Si	Lars-Erik Wernersson	J. Appl. Phys.	117, 112810 (2015);	AIP Publishing	10.1063/1.4913836	No
39	III-V compound semiconductor transistors – from planar to nanowire structures	H. Riel, L.-E. Wernersson, M. Hong. J. del Alamo	MRS Bulletin	Vol. 39, Iss. 08, pp 668-677, 2014	Cambridge University Press	10.1557/mrs.2014.137	No

Table A.2. List of Dissemination activities (public). Status 23 November 2015.

LIST OF DISSEMINATION ACTIVITIES								
No	Type of activities	Main leader	Title	Start date	Place	Type of audience	Size of audience	Countries addressed
1	Web sites / Applications	SCIPROM	E2SWITCH project website	01/01/14	www.e2switch.org	Academic, Public, Policy makers, Medias	>500	World
2	Scientific presentation	IBM	The futur of nanoelectronics	24/02/14	5th International Workshop on Advanced Scanning Probe Microscopy Techniques, Karlsruhe, Germany	Academic	0-99	World
3	Scientific presentation	IBM	III-V Semiconductor Nanowires for Future Devices	27/03/14	Design, Automation and Test in Europe 2014, Dresden, Germany	Academic	0-99	Europe
4	Flyer	SCIPROM	Project flyer	01/04/14		Academic	100-499	World
5	Scientific presentation	IUNET	15th International Conference on Ultimate Integration on Silicon, ULIS 2014	07/04/14	Stockholm; Sweden	Academic	0-99	World
6	Scientific presentation	IBM	Semiconducting Nanowires - From Materials to Devices	21/05/14	Swiss NanoConvention. Windisch, Switzerland	Academic	0-99	Switzerland
7	Scientific presentation	IBM	In Quest of a New Nanoelectronic Low Power Switch	10/06/14	International Summer School on Physics at Nanoscale, Devet Skal, Czech Republic	Academic	0-99	World

LIST OF DISSEMINATION ACTIVITIES								
No	Type of activities	Main leader	Title	Start date	Place	Type of audience	Size of audience	Countries addressed
8	Scientific presentation	JUELICH	Experimental Demonstration of Inverter and NAND Operation in p-TFET logic at Ultra-low Supply Voltages down to VDD = 0.15 V	22/06/14	72nd Device Research Conference (DRC), UC Santa Barbara, USA	Academic	100-499	World
9	Scientific presentation	IBM	Semiconducting Nanowires – From Materials to Devices	07/07/14	CMOS Emerging Technologies Research 2014, Grenoble, France	Academic	0-99	Europe
10	Scientific presentation	IBM	Dynamics of III-V MOVPE inside nanotube templates on Si	13/07/14	ICMOVPE XVII Lausanne	Academic	100-499	World
11	Scientific presentation	IBM	The Future of Nanoelectronics: New Material, Architectures and Mechanisms	13/07/14	ICMOVPE XVII, Lausanne, Switzerland	Academic	0-99	CH
12	Scientific presentation	IBM	Dynamics of III-V MOVPE inside Nanotube Templates on Si	16/07/14	ICMOVPE XVII, Lausanne, Switzerland	Academic	0-99	CH
13	Scientific presentation	IBM	Semiconducting Nanowires - From Materials to Devices	18/07/14	Gordon Research Conference, Biddeford, ME, USA	Academic	0-99	World
14	Scientific presentation	IBM	Semiconducting Nanowires – Growth, Characterization & Devices	07/08/14	International Conference on Superlattices, Nanostructures and Nanodevices, Savannah, GA, USA	Academic	100-499	World
15	Scientific presentation	LUND	Invited talk at ICPS (International Conference of Physics of Semiconductors)	10/08/14	ICPS, Austin, USA	Academic	>500	
16	Scientific presentation	IBM	Inducing a Direct-to-Pseudodirect Bandgap Transition in Wurtzite GaAs Nanowires with Uniaxial Stress	29/08/14	Nanowire Conference 2014, Eindhoven, The Netherlands	Academic	0-99	World
17	Scientific presentation	ETHZ	Analysis of GeSn-SiGeSn Hetero-Tunnel FETs	09/09/14	2014 International Conference on Simulation of Semiconductor Processes and Devices, Yokohama, Japan	Academic	100-499	World
18	Scientific presentation	EPFL	A First Order Capacitance-Voltage model for DG-TFET	09/09/14	International Conference on Simulation of Semiconductor Processes and Devices, Yokohama, Japan	Academic	100-499	World
19	Scientific presentation	EPFL	Two Dimensional Quantum Mechanical Simulation of Low Dimensional Tunneling Devices	22/09/14	2014 44th European Solid-State Device Conference	Academic	100-499	World
20	Scientific presentation	ETHZ	Analysis of InAs-Si Heterojunction Nanowire Tunnel FETs: Extreme Confinement versus Bulk	22/09/14	2014 44th European Solid-State Device Conference (ESSDERC), Venice, Italy	Academic	100-499	World
21	Scientific presentation	IUNET	A quasi 2D semianalytical model for the potential profile in hetero and homojunction tunnel FETs	22/09/14	European Solid-State Device Research Conference (ESSDERC), Venice, Italy	Academic	>500	World
22	Scientific presentation	IUNET	Advanced Modeling and Simulation Approaches for Nanoscale FETs	22/09/14	"CMOS Technology at the nm Scale Era" tutorial, ESSDERC, Venice, Italy	Academic	0-99	World
23	Scientific presentation	JUELICH	Experimental demonstration of improved analog device performance in GAA-NW-TFETs	22/09/14	2014 44th European Solid-State Device Conference (ESSDERC), Venice	Academic	100-499	World

LIST OF DISSEMINATION ACTIVITIES								
No	Type of activities	Main leader	Title	Start date	Place	Type of audience	Size of audience	Countries addressed
24	Scientific presentation	IUNET	Two Dimensional Quantum Mechanical Simulation of Low Dimensional Tunneling Devices	24/09/14	European Solid-State Device Research Conference (ESSDERC), Venice, Italy, 2014, pp. 186-189	Academic		World
25	Press release	EPFL	EPFL Press Release: September 25, 2014	25/09/14		Academic, Industry, Public, Policy makers, Medias, Other	100-499	
26	Scientific presentation	IUNET	Analysis of TFET based 6T SRAM cells implemented with state of the art silicon nanowires	25/09/14	European Solid-State Device Research Conference (ESSDERC), Venice, Italy, pp. 282-285	Academic	>500	World
27	Scientific presentation	IBM	The futur of nanoelectronics	25/09/14	Kompetenznetz Funktionelle Nanostrukturen, Bad Herrenalb, Germany	Academic	0-99	DE
28	Scientific presentation	IUNET	Simulation of Tunnel FETs for accurate performance prediction at device and circuit level	26/09/14	Workshop "In the Quest of Zero Power: Energy Efficient Computing Devices and Circuits", ESSDERC, Venice, Italy	Academic	0-99	World
29	Workshop organisation	EPFL	In the Quest of Zero Power: Energy Efficient Computing Devices and Circuits	26/09/14	European Solid-State Device Research Conference (ESSDERC), Venice, Italy	Academic	0-99	World
30	Scientific presentation	JUELICH	SiGe strained nanowire tunnel FETs: integration and performance	26/09/14	Workshop "In the Quest of Zero Power: Energy Efficient Computing Devices and Circuits", ESSDERC, Venice, Italy	Academic	0-99	World
31	Scientific presentation	IMEC	Low power Tunnel FET circuits: challenges and opportunities	26/09/14	Workshop "In the Quest of Zero Power: Energy Efficient Computing Devices and Circuits", ESSDERC, Venice, Italy	Academic	0-99	World
32	Scientific presentation	LUND	Tunnel FETs for digital and analog/RF applications	26/09/14	Workshop "In the Quest of Zero Power: Energy Efficient Computing Devices and Circuits", ESSDERC, Venice, Italy	Academic	0-99	World
33	Scientific presentation	EPFL	Computing and sensing with steep-slope devices	26/09/14	Workshop "In the Quest of Zero Power: Energy Efficient Computing Devices and Circuits", ESSDERC, Venice, Italy	Academic, Industry	0-99	World
34	Scientific presentation	IBM	III-V heterostructure TFETs integrated on silicon for low-power electronics	26/09/14	Workshop "In the Quest of Zero Power: Energy Efficient Computing Devices and Circuits", ESSDERC, Venice, Italy	Academic, Industry	0-99	World
35	Scientific presentation	IUNET	2014 Si, SiGe, and Related Compounds: Materials, Processing, and Devices Symposium	08/10/14	Moon Palace Resort, Cancun, Mexico	Academic, Industry	0-99	
36	Scientific presentation	IBM	Materials and Devices for Next Generation Electronics at IBM Research - Zurich	10/10/14	IBM - Notre Dame Workshop, Notre Dame University, IN, USA	Academic	0-99	World

LIST OF DISSEMINATION ACTIVITIES								
No	Type of activities	Main leader	Title	Start date	Place	Type of audience	Size of audience	Countries addressed
37	Scientific presentation	JUELICH	Strained Silicon nanowire Tunnel FETs and NAND logic	29/10/14	Invited paper at ICSICT, Guilin, China	Academic	100-499	World
38	Film	SCIPROM	E2SWITCH movie	19/11/14		Academic	>500	World
39	Scientific presentation	IBM	Enhancement of Seebeck Coefficient and Thermoelectric Power Factor in One-Dimensional InAs Nanowires	30/11/14	MRS Fall Meeting, Boston, MA, USA	Academic, Industry	100-499	World
40	Scientific presentation	IBM	EuroSOI-Ulis 2015	26/01/15	EuroSOI-Ulis 2015, Bologna	Academic	>500	World
41	Scientific presentation	IUNET	NATO Advanced Research Workshop “Functional Nanomaterials and Devices for Electronics, Sensors, Energy Harvesting"	13/04/15	Lviv	Academic	0-99	
42	Scientific presentation	IUNET	Challenges and opportunities related to innovative material systems in CMOS transistors and Tunnel FETs.	11/05/15	European Materials Research Society Spring Meeting 2015; Symposium Z: Nanomaterials and processes for advanced semiconductor CMOS devices	Academic	don't know	
43	Scientific presentation	JUELICH	Si Nanowire Tunnel FETs for energy efficient nanoelectronics (invited)	25/05/15	ECS symposium	Academic	100-499	World
44	Scientific presentation	ETHZ	(Invited) Comparative Simulation Study of InAs/Si and All-III-V Hetero Tunnel FETs	27/05/15	ECS, Symposium Device Physics, Chicago	Academic, Industry	100-499	World
45	Poster	EPFL	Silicon Nanoelectronic Workshop 2015	14/06/15	Kyoto, Japan	Academic	0-99	World
46	Scientific presentation	LUND	CSW2015	28/06/15	CSW, UCSB	Academic	100-499	World
47	Scientific presentation	IUNET	Modeling and simulations for the design of nanoscale transistors	29/06/15	Tutorial of the INFOS Conference	Academic, Industry	100-499	
48	Scientific presentation	CCS	TSensors (Trillion Sensors) Summit Munich	15/09/15	TSensors Summit , Munich, Germany	Academic, Industry	100-499	World
49	Scientific presentation	ETHZ	Analysis of InAs-Si Heterojunction Double-Gate Tunnel FETs with Vertical Tunneling Paths	16/09/15	ESSDERC 2015, Graz	Academic	0-99	World
50	Scientific presentation	IUNET	ESSDERC 2015	16/09/15	Graz	Academic	100-499	
51	Scientific presentation	EPFL	Compact modeling of DG-Tunnel FET for Verilog-A Implementation	16/09/15	ESSDERC 2015	Academic	0-99	World
52	Scientific presentation	IUNET	4th Berkeley Symposium on Energy Efficient Electronic Systems	01/10/15	Berkeley University	Academic, Industry	0-99	International Workshop
53	Scientific presentation	CCS	Benchmarking of TFET Analogue Circuits: Sensors applications perspective	05/10/15	Steep Transistors Workshop, Notre-Dame, USA	Academic	0-99	world
54	Scientific presentation	IUNET	Experimentally reported sub-60mV/dec swing in Tunnel FETs	05/10/15	Steep Transistors Workshop, Notre-Dame, USA	Academic	0-99	world
55	Scientific presentation	EPFL	E2SWITCH Project Functional diversification with Tunnel FETs	05/10/15	Steep Transistors Workshop, Notre-Dame, USA	Academic	0-99	world

LIST OF DISSEMINATION ACTIVITIES								
No	Type of activities	Main leader	Title	Start date	Place	Type of audience	Size of audience	Countries addressed
56	Scientific presentation	JUELICH	sere Ziele Das Forschungszentrum Jülich im Fokus Mitglied der Helmholtz-Gemeinschaft TFETs for ultra low power	05/10/15	Steep Transistors Workshop, Notre-Dame, USA	Academic	0-99	world
57	Scientific presentation	LUND	Nanowire Tunnel FETs: Axial or Radial TFETs?	05/10/15	Steep Transistors Workshop, Notre-Dame, USA	Academic	0-99	world
58	Scientific presentation	IBM	Where are we with TFETs?	05/10/15	Steep Transistors Workshop, Notre-Dame, USA	Academic	0-99	world
59	Workshop organisation	LUND	Steep Transistors Workshop	05/10/15	Notre-Dame University, Notre-Dame, USA	Academic	0-99	world
60	Scientific presentation	IBM	Beyond CMOS Workshop	16/10/15	IMEC, Leuven, Belgium	Academic, Industry	100-499	
61	Scientific presentation	IBM	Template-Assisted Selective Epitaxy: Highly controlled III-V nanowire integration on Si	26/10/15	Nanowires 2015, Barcelona	Academic	100-499	World

B. Exploitable knowledge and its use (confidential)

B.1 Applications for patents, trademarks, registered designs, etc.

Key industrial personnel have been trained in patenting and patent search techniques. A general patent search concerning the use of the described novel technologies in the field of TFET has been conducted, and is reported in Figure 18 and Table B.1b. In addition to this, during and afterwards, all partners will be required to make a patent search in the field of their respective technologies, and then to strive to develop new patents in the field.

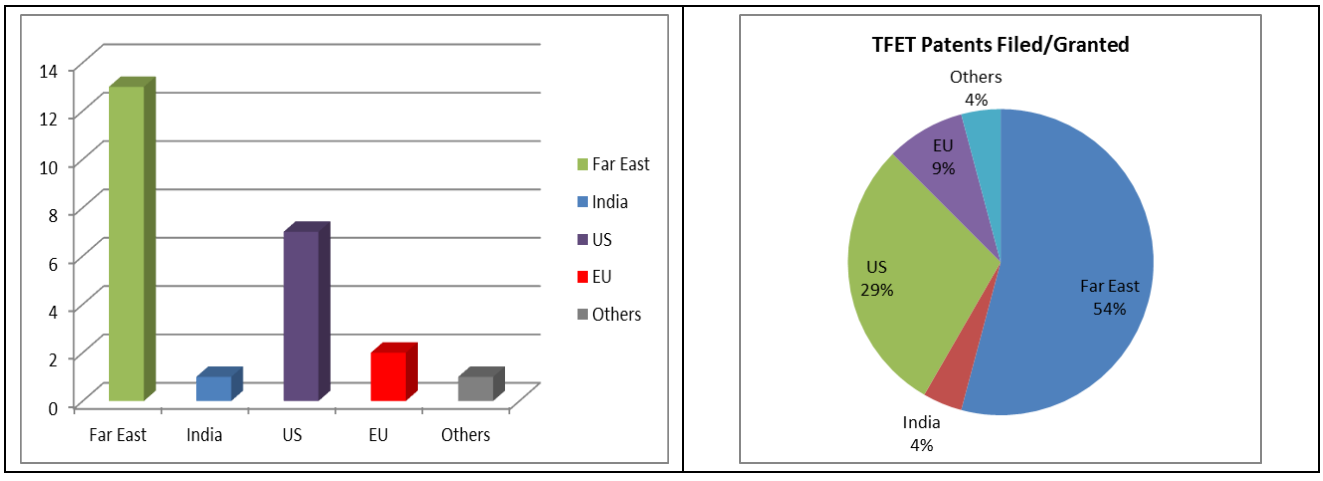


Fig. 18. Summary of patents sited: number of patents (left); region-based share of patents (right)

It should be noted that the only two EU patents are from E2SWITCH beneficiary IMEC. The Consortium is aware that one needs to actively raise the European profile in scientific innovation to the global community.

Table B.1a. Patent search

Topic	Inventor	Applicant	CPC	IPC	Publication info	Priority date

Tunneling Field Effect Transistor (TFET) Formed By Asymmetric Ion Implantation and Method of Making Same	ZHANG YING [TW]	TAIWAN SEMICONDUCTOR MFG [TW]	H01L21/266 H01L21/31138 H01L21/31155 (+4)	H01L21/266 H01L29/66	US2015187584 (A1) 2015-07-02	2012-12-18
TFET (Tunneling Field Effect Transistor) and forming method thereof	HUANG XINYUN ZENG YIZHI (+1)	SEMICONDUCTOR MFG INT SHANGHAI		H01L21/336 H01L29/08 H01L29/78	CN104425606 (A) 2015-03-18	2013-09-04
Complementary TFET and manufacturing method thereof	XIAO DEYUAN	SEMICONDUCTOR MFG INT CORP	H01L21/02381 H01L21/02466 H01L21/02549 (+7)	H01L21/8238 H01L27/092	CN104465657 (A) 2015-03-25	2013-09-22
Deep-N-well technology based production method capable of isolating tunneling field effect transistor (TFET)	HUANG RU HUANG QIANQIAN (+5)	UNIV BEIJING		H01L21/336 H01L21/761	CN104332409 (A) 2015-02-04	2014-11-05
Deep-energy-level impurity tunneling field-effect transistor (TFET) and preparation method thereof	HUANG RU WU CHUNLEI (+3)	UNIV BEIJING		H01L21/336 H01L29/06 H01L29/10 (+1)	CN104241374 (A) 2014-12-24	2014-08-29
Anti-staggered-layer heterojunction resonance tunneling field-effect transistor (TFET) and preparation method thereof	HUANG RU WU CHUNLEI (+3)	UNIV BEIJING		H01L21/336 H01L29/41 H01L29/78	CN104241373 (A) 2014-12-24	2014-08-29
TUNNEL FIELD-EFFECT TRANSISTOR (TFET) WITH SUPERSTEEP SUB-THRESHOLD SWING	MALLIK ABHIJIT [IN]	UNIV CALCUTTA [IN]	H01L29/0657 H01L29/0843 H01L29/1025 (+2)	H01L29/08	WO2015001399 (A1) 2015-01-08	2013-07-03
TFET with Nanowire Source	BANGSARUNTIP SARUNYA [US] LAUER ISAAC [US] (+2)	BANGSARUNTIP SARUNYA [US] LAUER ISAAC [US] (+3)	B82Y10/00 H01L29/0665 H01L29/0669 (+15)	H01L29/06 H01L29/08 H01L29/78	US2014239258 (A1) 2014-08-28 US8946680 (B2) 2015-02-03	2010-05-11
Tunneling Field Effect Transistor (TFET) With Ultra Shallow Pockets Formed By Asymmetric Ion Implantation and Method of Making Same	ZHANG YING [TW]	TAIWAN SEMICONDUCTOR MFG CO LTD [US] TAIWAN SEMICONDUCTOR MFG [TW]	H01L29/1045 H01L29/66356 H01L29/7311 (+1)	H01L29/66	US2014158990 (A1) 2014-06-12	2012-12-12
Source-grid-drain common-controlled single-doped type TFET (tunneling field effect transistor)	LIU XI JIN XIAOSHI (+1)	UNIV SHENYANG TECHNOLOGY	H01L29/0603 H01L29/16 H01L29/1608 (+1)	H01L29/06 H01L29/78	CN103531636 (A) 2014-01-22	2013-10-25
TUNNEL FIELD EFFECT TRANSISTOR (TFET) WITH LATERAL	LEE JACK C [US] ZHAO HAN [US]	LEE JACK C [US] ZHAO HAN [US] (+1)	H01L29/0653 H01L29/0895 H01L29/78609 (+3)	H01L21/336 H01L29/78 H03K17/74	US2013093497 (A1) 2013-04-18	2011-10-14

OXIDATION						
LINE-TUNNELING TUNNEL FIELD-EFFECT TRANSISTOR (TFET) AND MANUFACTURING METHOD OF THE SAME	IMEC	IMEC KATHOLIEKE UNIV LEUVEN KU LEUVEN R & D	B82Y10/00 H01L29/0665 H01L29/7391	H01L29/06 H01L29/66 H01L29/786	JP2013012723 (A) 2013-01-17	2011-05-23
STRUCTURE FOR USE IN FABRICATION OF PIN HETEROJUNCTION TFET	BANGSARUNTIP SARUNYA [US] KOESTER STEVEN [US] (+2)	BANGSARUNTIP SARUNYA [US] KOESTER STEVEN [US] (+3)	H01L21/2007 H01L21/76254 H01L29/66227 (+1)	H01L29/772	US2012298963 (A1) 2012-11-29	2010-01-08
Self-adaptive composite mechanism tunneling field effect transistor (TFET) and preparation method thereof	RU HUANG QIANQIAN HUANG (+3)	UNIV BEIJING	H01L21/823807 H01L21/823814 H01L29/7391	H01L21/336 H01L29/08 H01L29/78	CN102664192 (A) 2012-09-12	2012-05-08
Method for manufacturing complementary tunneling field effect transistor (TFET) based on standard complementary metal oxide semiconductor integrated circuit (CMOS IC) process	RU HUANG QIANQIAN HUANG (+3)	UNIV BEIJING	H01L21/823807 H01L21/823814 H01L21/823892 (+2)	H01L21/8238	CN102664165 (A) 2012-09-12 CN102664165 (B) 2014-06-04	2012-05-18
High-voltage-resistant tunneling field effect transistor (TFET) and preparation method thereof	NING CUI RENRONG LIANG (+2)	UNIV TSINGHUA	H01L29/66356 H01L29/7391	H01L21/336 H01L29/06 H01L29/10 (+1)	CN102569363 (A) 2012-07-11	2012-02-15
TFET BASED 6T SRAM CELL	SINGH JAWAR [US] KRISHNAN RAMAKRISHNAN [TW] (+3)	SINGH JAWAR [US] KRISHNAN RAMAKRISHNAN [TW] (+4)	G11C11/412	G11C11/419	US2012106236 (A1) 2012-05-03 US8369134 (B2) 2013-02-05	2010-10-27
Tunneling field effect transistor (TFET) and manufacturing method thereof	RU HUANG QIANQIAN HUANG (+2)	UNIV BEIJING		H01L21/336 H01L29/08 H01L29/78	CN102364690 (A) 2012-02-29 CN102364690 (B) 2013-11-06	2011-11-02
LOW VOLTAGE TUNNEL FIELD-EFFECT TRANSISTOR (TFET) AND METHOD OF MAKING SAME	SEABAUGH ALAN C [US] FAY PATRICK [US] (+5)	SEABAUGH ALAN C [US] FAY PATRICK [US] (+6)	H01L29/7391	H01L21/336 H01L29/78	US2012032227 (A1) 2012-02-09 US8796733 (B2) 2014-08-05	2010-08-09
VERTICAL TUNNEL FIELD-EFFECT TRANSISTOR (TFET) MANUFACTURING METHOD		IMEC UNIV LEUVEN KATH	B82Y10/00 H01L29/0665 H01L29/165 (+3)	H01L21/336 H01L21/8238 H01L27/092 (+3)	JP2011238909 (A) 2011-11-24 JP5542728 (B2) 2014-07-09	2010-04-19
TFET BASED 4T MEMORY DEVICES	SARIPALLI VINAY [US] MOHATA DHEERAJ [US]	STATE RES FOUND [US] SARIPALLI VINAY [US]	G11C11/412 G11C11/413 H01L27/11	G11C11/34 G11C11/412	WO2011153451 (A2) 2011-12-08 WO2011153451 (A3) 2012-03-29	2010-06-04

	(+3)					
Low-power consumption tunneling field effect transistor (TFET) of fork-structure grid structure	ZHAN ZHAN QIANQIAN HUANG (+2)	UNIV BEIJING	H01L29/4238 H01L29/7391	H01L29/423 H01L29/78	CN102157559 (A) 2011-08-17 CN102157559 (B) 2012-05-02	2011-03-01
METHOD OF FABRICATING A SILICON TUNNELING FIELD EFFECT TRANSISTOR (TFET) WITH HIGH DRIVE CURRENT		GLOBALFOUNDRIES SG PTE LTD	1 B82Y10/00 H01L21/26586 H01L29/0895 (+3)		SG170670 (A1) 2011-05-30	2009-10-08
TFET USING ASYMMETRIC SCHOTTKY BARRIER AND FABRICATION METHOD OF THE SAME	PARK BYUNG GOOK [KR] KIM JONG PIL [KR]	SNU R&DB FOUNDATION [KR]		H01L21/338 H01L29/812	KR20110005185 (A) 2011-01-17 KR101030983 (B1) 2011-04-28	2009-07-09

Table B.1b. List of applications for patents, trademarks, registered designs, etc.

LIST OF APPLICATIONS FOR PATENTS, TRADEMARKS, REGISTERED DESIGNS,UTILITY MODELS, ETC.							
Type of IP Rights: Patents, Trademarks, Registered designs, Utility models, etc.	Application reference(s) (e.g. EP123456)	Intellectual Property Organization	Subject or title of application	Confidential (yes/no)	Foreseen embargo date	Applicant (s) (as on the application)	URL of application (mandatory for patents)

B.2 Exploitable foreground

The exploitation strategies outlined at the start of the project are described in the DoW. Table B2.1 will summarise the exploitable foreground as identified by the consortium. Progress along each exploitation track will be monitored by the Exploitation Manager and will be reported in the end of the project in the final PUDF.

Table B.2a. Overview table with exploitable foreground

OVERVIEW TABLE WITH EXPLOITABLE FOREGROUND							
Type of exploitable foreground	Description of exploitable foreground	Confidential	Exploitable product(s) or measure(s)	Sector(s) of application	Timetable, commercial or any other use	Patents or other IPR exploitation (licences)	Owner & other beneficiary(s) involved
e.g. General advancement of knowledge							
e.g. Commercial exploitation of R&D results							

TableB.2b. Exploitation activities of the consortium: template table

EXPLANATION OF THE EXPLOITABLE FOREGROUND	
Lead partner name	
Describe the innovation content of the result to be exploited.	
Who will be the customer?	
What benefit will it bring to the customers?	
When is the expected date of achievement in the project?	
What is the time to market?	
What are the costs to be incurred after the project and before exploitation?	
What is the approximate price range of this result / price of licences?	
What is the market size in Million € for this result? What is the trend?	
How will this result rank against competing products in terms of price / performance?	
Who are the competitors for this result?	
How fast and in what ways will the competition respond to this result?	
Who are the project partners involved in the result?	
Who are the industrial partners interested in the result (partners, sponsors, etc…)?	
Have you protected or will you protect this result? How? When?	

References

[1] Grant Agreement Annex I (DoW): available in the E2SWITCH document repository: http://www.e2switch.eu/members/repository/legal/DOW_E2SWITCH_2013-09-13_final_bookmarks.pdf

[2] Consortium Agreement: http://www.e2switch.eu/members/repository/legal/E2SWITCH_CA_signed.pdf

[3] Management guidelines: http://www.e2switch.org/members/repository/deliverables/E2SWITCH_D8.1_v1.pdf