E2SWITCH
Energy Efficient Tunnel FET Switches and Circuits

Co-funded by the European Union

E²SWITCH

Energy Efficient Tunnel FET Switches and Circuits

Grant Agreement No.: 619509

Funding Scheme: Collaborative project

Thematic Area: Energy efficient switch, tunnel FET, nanotechnology III-V, SiGe and Ge, low power integrated circuits, digital and analog/RF circuits, CMOS, simulation and modeling of nano-electronic devices & circuits

Project start date: 01-11-2013

Deliverable D7.9 — Roadmap for commercial use of E2SWITCH results

Nature[1]: R

Dissemination level[2]: PU

Due date[3]: M48

Date of delivery: M49

Lead partner: IBM

Contributing partners: CCS, EPFL

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[1] R = Report, P = Prototype, D = Demonstrator, O = Other

[2] PU = Public, PP = Restricted to other programme participants (including the Commission Services, RE = Restricted to a group specified by the consortium (including the Commission Services), CO = Confidential, only for the members of the consortium (including the Commission Services)

[3] Measured in months from the project start date (M01)

Revision history

Version	Date	Author	Comment
0.1	24 October 2017	K. Moselund	First draft
0.3	16 Nov 2017	M Foysol Chowdhury	Final draft
1.0	28 Nov 2017	A. Ionescu, K. Leufgen	Final version, approved by the consortium

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Summary

This document contains task and work conducted by IBM together with EPFL, CCS and the other industrial partners on a roadmap for commercial evaluation and market research. The aim of this task is to carry out a market survey during the project phase. This work was done by visited workshops and conferences in order to get feedback from the community. From this we have been able to define a more precise projection of the road mapping of future products, and able to get a better understanding of the market volumes requirement of TFET technology. We have used the results horizontally in related application areas in order to deduce our findings.

1 TFET Technology roadmap

Whether Moore's law is alive and kicking or whether it is slowly dying is up for debate. As Fig. 1 shows though transistor count continues to increase and scaling is still pursued for the next couple of nodes, while frequency and performance is saturating or slowing down. Power dissipation continues to be the main limitation in modern microelectronics, whether this is for small form factor mobile devices, where battery lifetime is a limitation or for large scale super-computers, where overall power consumption is a key limitation towards exascale computing.

Also, as a result of the increasing penetration of electronic and online applications, data center power consumption is on an exponential increase. Therefore, low-power devices have never been a more pertinent topic than at the present. The most efficient lever to reduce power consumption of micro-processors containing billions of field effect transistors (FETs) is reduction of the supply voltage. For low performance

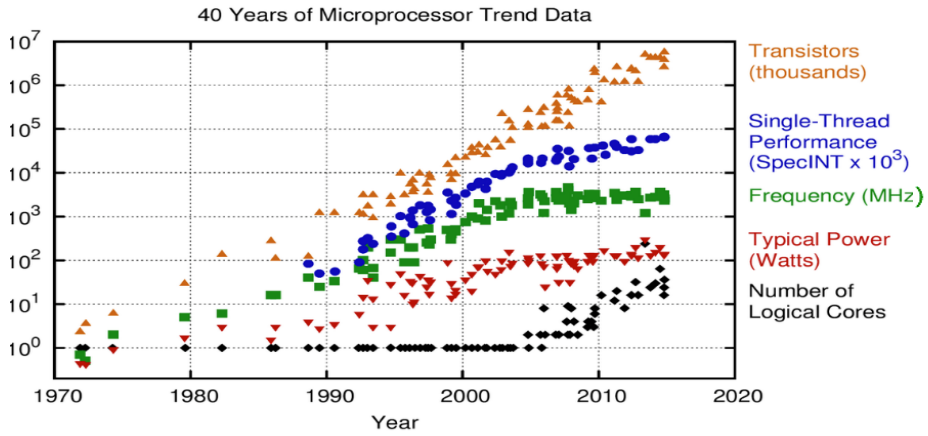

Figure 1: 40 years of microprocessor trend data [1]**.**

processors, this can be achieved by a dedicated architecture optimized for sub-threshold device operation. For high performance, the voltage scaling is fundamentally limited by the turn-on characteristics of the transistor, which can only be overcome by employing novel devices like tunnel FETs.

The tunnel FET continues to be one of the best options for ultra-low power devices. Other alternatives to logic devices are the ferro-electric gate FETs, phase-change devices and device concepts based on non-charge based transport such as magnetic or nuclear spins. However, all these devices they would likely have a lower threshold of insertion, compared to tunnel FETs. Moreover, TFETs structure resembles that of a MOSFET, and they can implement most of the logic gates currently using FETs.

Within E^{2}SWITCH some of the best tunnel-FETs worldwide have been demonstrated – finally the barrier to sub-thermionic slopes seems to have been broken.

The simulation and modelling teams within E2SWITCH have contributed to an in-depth understanding of the limitations of TFETs and how to scale the device in order to achieve best performance. Notably, as we move forward, a great challenge for TFETs is to achieve channel scaling and gate alignment and to limit the role of traps which is detrimental for TFETs performances.

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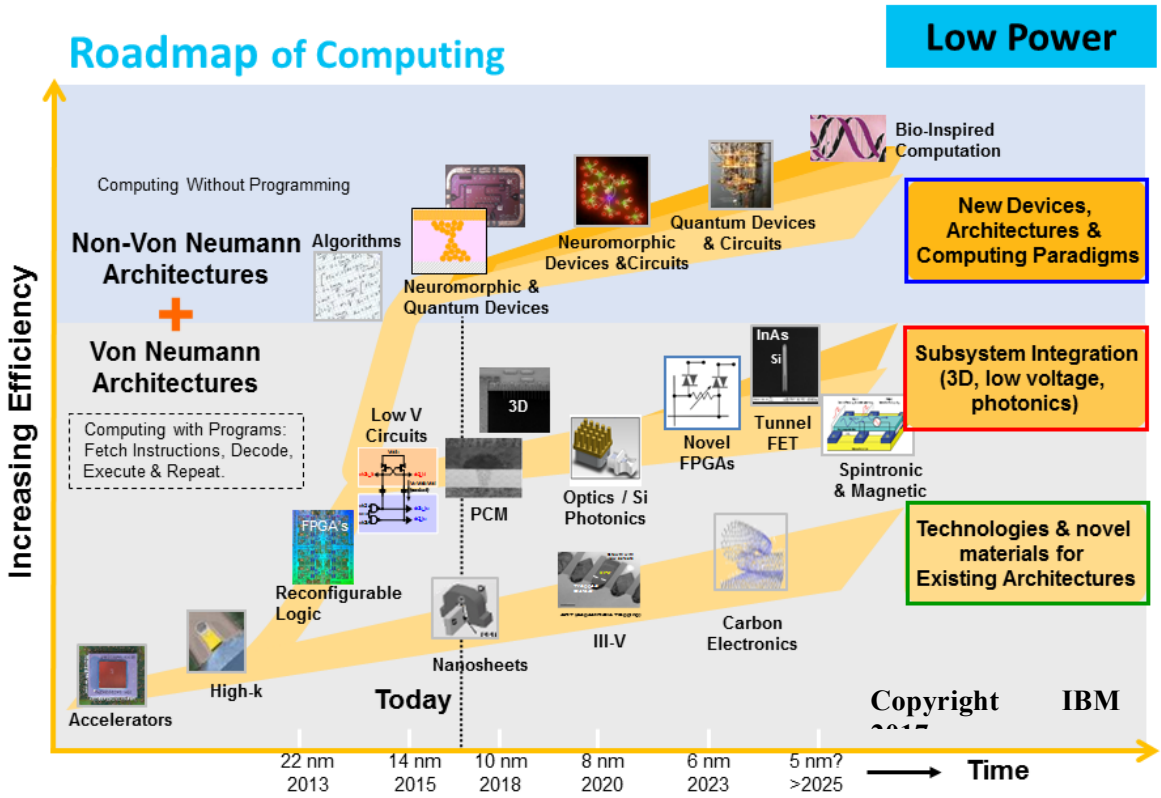

Figure 2: Roadmap of computing representing IBMs vision for the future. Copyright IBM 2017.

Figure 2 represents IBMs vision for a future roadmap of computing, where a diversification in terms of both materials, devices, and system architectures is foreseen. The first path represents the developments we foreseen in terms of continued scaling and the introduction of novel materials. In June 2017 at the VLSI symposium, IBM demonstrated the world's first 5nm node test chip. The transistors here are nanosheets, this 3D geometry both exploits the improved electrostatics of a gate-all-around architecture, combined with vertical stacking to boost current level. III-V materials are known to present higher electron mobilities, hence they are attractive for n-FET channels, but there is a lot of technological challenges related to their integration on silicon.

The second path represents novel devices both for logic and memory, we currently do not foresee a replacement of Si CMOS, but rather that these devices may each find their application space. One important point is that many of these device developments are intrinsically tied to the technology platform, for example both active photonic devices as well as tunnel FETs will require III-V materials. Hence maintaining technological expertise and potential for innovation is essential. In particular if Europe wishes to play an active role in the development and exploitation of these systems, then it is essential to also foster an ecosystem of technological innovation and to continue to support the entire technology foodchain.

E2SWITCH demonstrated that performance superior of tunnel FETs to that of MOSFETs can be achieved, however this is only the first step on the path. It has been shown that heterojunctions will provide the best performance trade-offs, and within E2SWITCH we developed a III-V integration method which allows to densely integrate multiple III-V materials locally in-plane on silicon. However, complementary tunnel FET logic requires the presence of at least two different materials for each device type – *within the channel itself*, hence mastering multiple materials in terms of contacting and gate stacks on the same wafer or even the same devices is a large technological challenge.

The third path represents system architectures beyond Von-Neuman, such as neuro-morphic or quantum computing. These may or may not exploit the novel devices and materials, and most likely we will see two waves, like for present day advances in cognitive computing. Presently most systems are based on conventional Si CMOS with the main innovation being in the system design and algorithms, but eventually this will likely be complemented by true native devices with embedded neuromorphic function.

As already mentioned, excellent TFET device performance has been demonstrated, hence it is possible to achieve good performance once electrostatics are optimized, and probably the largest issue in terms of individual devices performance is mastering the impact of traps. In order, to be implemented as a technology the main issues are now related to the practical implementation of complementary heterojunction tunnel FETs in a CMOS compatible process flow. Here, following topics remain to be addressed in detail: variability, transient performance, scaling, reliability and yield which all must be comparable to that of MOSFETs.

2 TFET Applications roadmap

Some aspects of the potential TFET technology application was already reported in D7.7. In this deliverable, we looked at specific areas through market trends to define a more precise roadmap for future TFET device applications.

Based on the technology development roadmap as shown in Figure 2, as the market applications evidence suggested that by 2025 when TFET is in commercial production, it will still remain in the era of "More than Moore" law (see Figure 3).

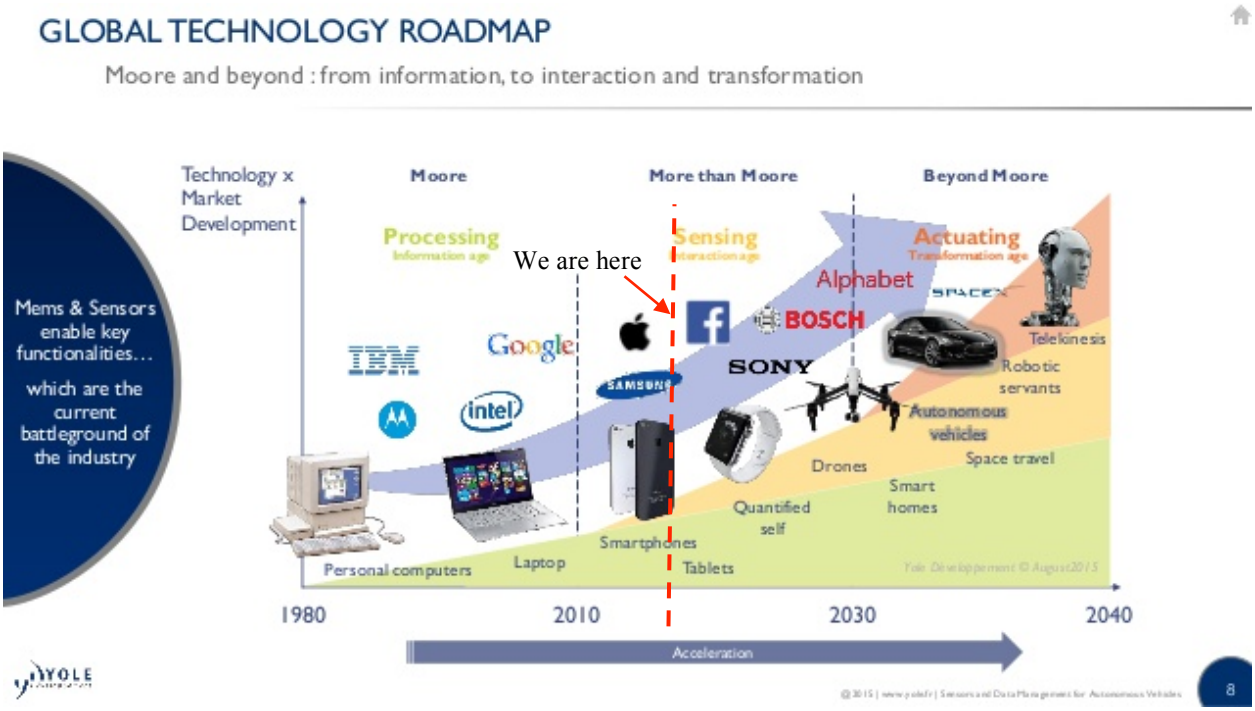

Figure 3: Roadmap for Moore and beyond.

According to Yole report[2] May 20, 2016: "Driven by a full applications range, drones and robots market is expected to grow at CAGR1 of 9.4% between 2015 and 2021, reaching a total revenue of US$ 46 billion by 2021.

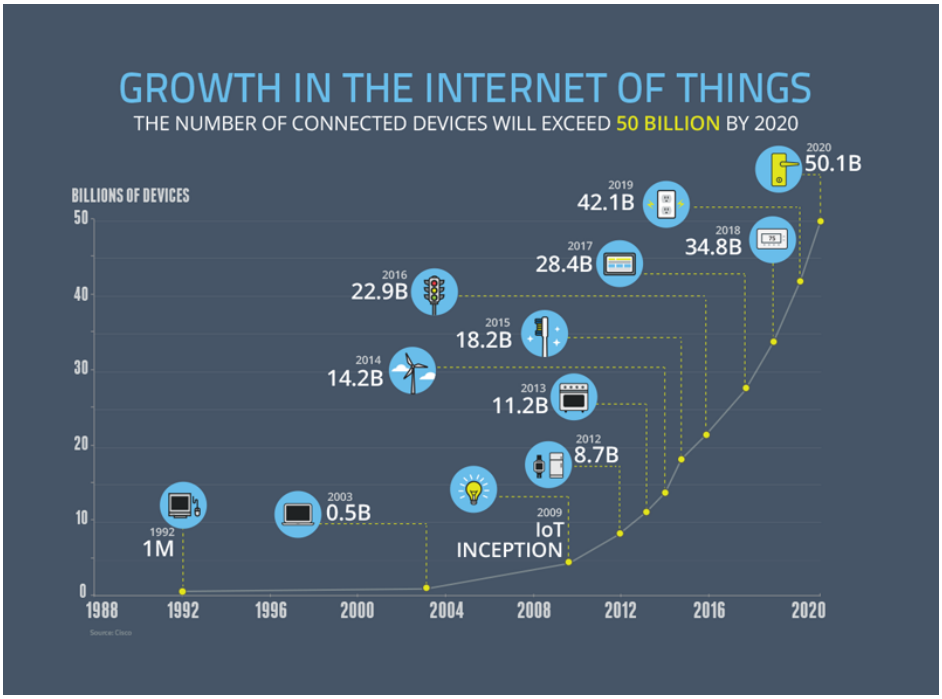

Figure 4: Roadmap for IoT demand.

The market will see step by step integration those technologies within robots and drones systems." Acoustic, optical, position, touch, electromagnetic and environmental sensors are part of the drones and robots revolution (see Figure 5).

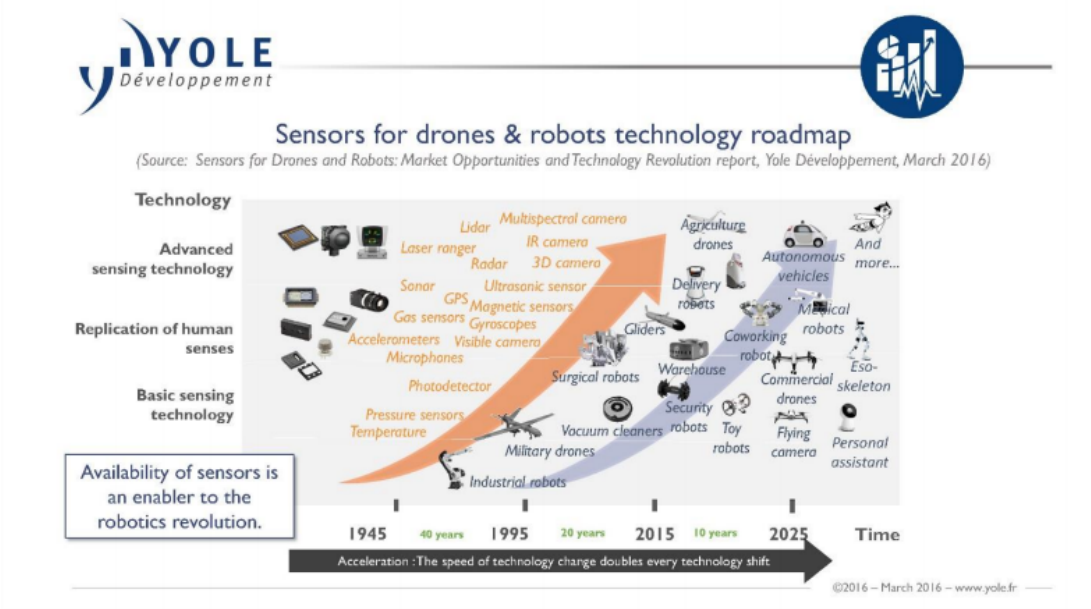

Figure 5: Roadmap for sensor, drones and robot technology.

During this phase (between 2015 to 2025) we are seeing a huge growth in sensor devices that are largely dominated by smart homes, factories, security and drones. Furthermore, by 2025, it is predicted that autonomous vehicles and commercial drones will make its presence which will ultimately lead to increase in demand for ultra-low power and energy harvested sensors and micro-processors (see Figure 6).

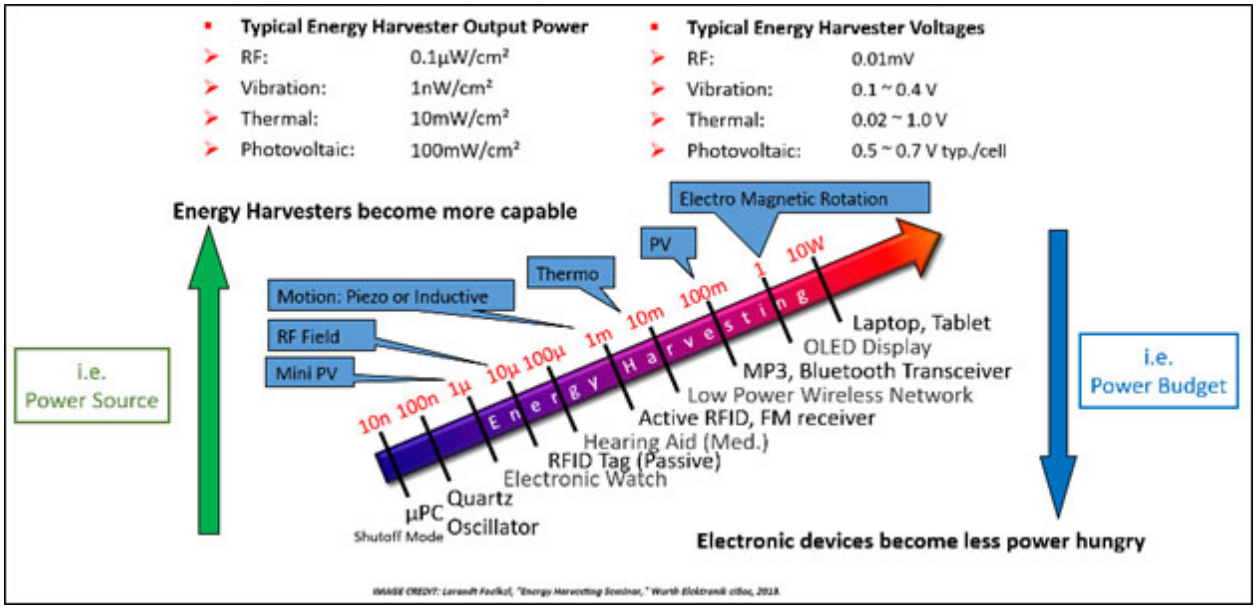

Figure 6: Roadmap for ultra-low power energy harvested devices [3].

In terms of energy harvesting, there are typically photovoltaic, vibration and thermoelectric. Two such examples of the roadmap is shown in Figure 7.

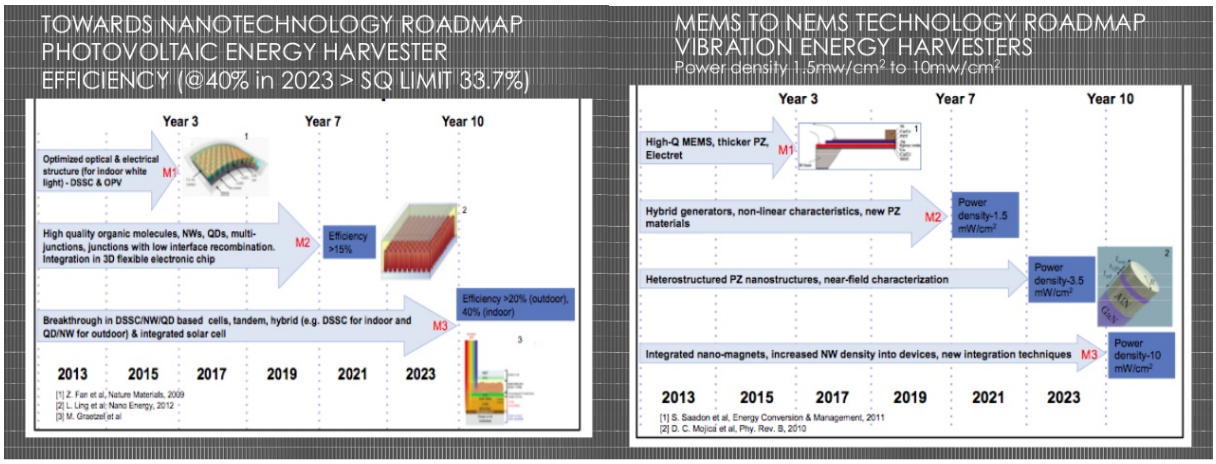

Figure 7: Roadmap for ultra-low power energy harvested technology [4].

Consequently, to make best use of energy harvest technology, low voltage and low power devices will be required and this is where it is believed that TFET technology developed from E^{2}SWITCH will be exploited and make wider impacts in other areas.

References

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