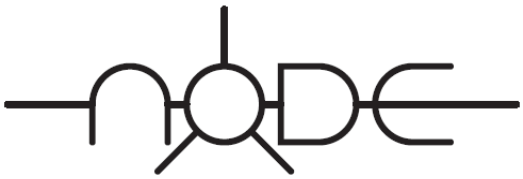

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NODE

Nanowire-based One-Dimensional Electronics

Integrated Project

Information Society Technologies

Publishable Executive Summary

Period covered: from 2005-09-01 to 2009-08-31 Date of preparation: 2009-10-10

Start date of project: 2005-09-01 Duration: 48 months

Project coordinator name: Lars Samuelson
Project coordinator organisation name: Lunds universitet Revision: Final

Nanowire-based One-Dimensional Electronics (NODE)

The integrated project "NODE" is developing and evaluating technologies for growth and processing of semiconductor nanowire devices for their possible impact as key add-on technologies to standard semiconductor fabrication. The partners in NODE work on generating a deepened understanding of the physics phenomena of one-dimensional semiconductor materials and nanowire-based devices, and on developing new functionalities not found in traditional higher-dimensional device structures.

A set of key device families based on semiconductor nanowires are studied in detail; such as tunneling devices, and field-effect transistors. Also unique opportunities that may be offered by nanowires in different areas are explored, e.g. memory applications. NODE is making a dedicated effort to evaluate the potential for integration of nanowire-specific processing methods and to assess the compatibility with requirements from conventional semiconductor processing, as well as evaluating novel architectural device concepts and their implementation scenarios.

Participants	Acronym	Country
Lunds universitet	LU	Sweden
Philips Electronics Nederland B.V.	PRE	Netherlands
Technische Universiteit Delft	TUD	Netherlands
Max Planck Gesellschaft zur Foerderung der Wissenschaften	MPI	Germany
Bayerische Julius – Maximilians Universität Würzburg	WU	Germany
Scuola Normale Superiore	SNS	Italy
IBM Research GmbH	IBM	Switzerland
Interuniversitair Micro-Elektronica Centrum vzw	IMEC	Belgium
Qumat Technologies AB	QM	Sweden
Commissariat á l'Energie Atomique	CEA	France
NXP Semiconductors Belgium NV	NXP	Belgium
Namlab gGmbH	NL	Germany

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Project webpage: www.node-project.com

Project objectives and major achievements

Overview of the general project objectives

Materials growth and processing technologies of semiconductor nanowire devices will be developed and evaluated for their possible impact as key add-on technologies to standard semiconductor fabrication. The goal is also to reach a deepened understanding of the physics of one-dimensional semiconductor materials and nanowire-based devices, and to develop new functionalities not found in traditional higher-dimensional device structures.

NODE will study in detail a set of key device families based on semiconductor nanowires, such as tunneling devices, and field-effect transistors, as well as explore unique opportunities that may be offered by nanowires in areas for storage applications. NODE will also make a dedicated effort to evaluate the potential for integration of nanowire-specific processing methods and to assess the compatibility with requirements from conventional semiconductor processing, as well as evaluate novel architectural device concepts and their implementation scenarios. More specifically the main objectives of NODE are:

- to build and evaluate electronic devices based on semiconductor nanowires:
    - NW-based transistors with increased frequency response and decreased power consumption
    - Nanowire logic elements
    - Explore potential for novel device designs using nanowires
- to assess nanowire growth and related nanostructuring in terms of up-scalability and Si-integration potential

Achievements

The research in NODE in many cases represents the state-of-the art in its field. The NODE partners are currently in the research forefront in areas such as (i) understanding of nanowire growth mechanisms, (ii) control of nanowire growth and nanowire doping (iii) characterization of the structural properties of nanowires (iv) processing of vertical nanowires structures (v) device research and development along the two tracks: InAs nanowire wrap-gate FETs and Si nanowire tunnel FETs, using both etched (fully-CMOS compatible) and bottom-up grown nanowires.

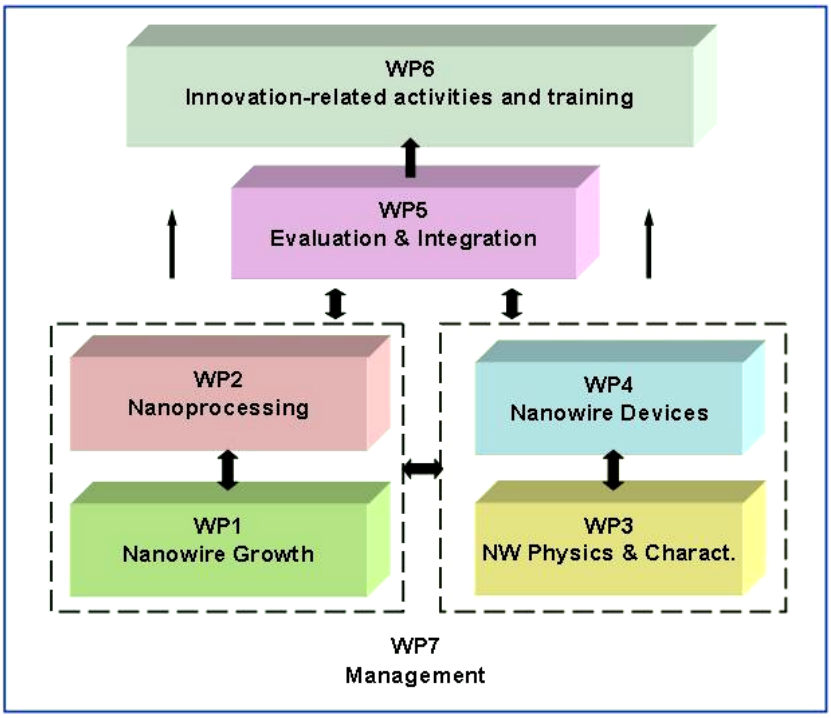
Since the project includes partners with strong background in research related to CMOS-integration, NODE had a strong focus on finding CMOS-compatible growth methods and processing conditions. Important sub-projects have therefore been to develop growth methods where gold is not required, and catalyst-free techniques have been developed for both InAs- and Si-nanowires, and Al, Pd, Ag seeding of Si nanowires has been demonstrated. A particular effort was also made on investigating the effect of gold on Si nanowires during growth and processing.

Design, fabrication and characterization of the first reported vertical RF-compatible nanowire transistors were carried out, demonstrated with InAs wrap-gate nanowires. Steep slope devices based on Si-nanowires were implemented, where also the first functional Si nanowire tunnel-FETs processed on 200mm wafers on a CMOS platform were demonstrated. Finally, multi-gated Si nanowire Schottky barrier FETs were realized, where an inverter function was demonstrated.

The NODE project has had a very high output in publications, and in total over 100 articles has been published at the end of the project. This clearly shows that considerable progress was made in the project and that the research was competitive on an international level. The NODE partners have applied for at least 48 patents related to nanowire research

and development, not including patent applications submitted within the last 18 months that are not yet publicly posted.

Diagram illustrating the work of the project



Nanowire growth is developed in WP1 and the grown material is characterized in WP3. Post-processing of nanowires is developed in WP2, and the technology is used in WP4 for building, evaluating and modelling devices. The nanowire growth, processing and device performance are finally evaluated in WP5 from an up-scaling perspective. WP6 collects the research results and takes care of the external presentation, and also training of young scientists in the project. The management of the project is conducted and overseen by WP7.

Work-package 1: Nanowire growth

The objectives of WP 1 stretched over the whole project duration. The main goal was to gain control of for NODE relevant NW formation. Better understanding of the different growth mechanisms and optimizing growth of NWs was developed, where the main materials research was focused towards InAs and Si nanowires. A strong focus was put on aspects of NW doping and on the Si integration of NW growth. This knowledge was then adapted to grow more technology relevant NW assemblies.

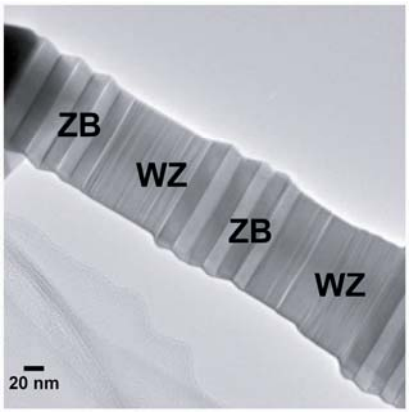
The over-all objectives of this work-package were divided into four categories:

- **General growth control**
  - Develop understanding of the nanowire growth mechanisms.
  - Investigate limits for the control of nanowire length, diameter, location, and growth direction
- **Heterostructures**
  - Develop and optimize growth of axial and radial heterostructures in nanowires.
- **Doping**
  - Develop understanding of the doping mechanism in nanowires and its limitations.
  - Find dopant precursors and growth conditions that lead to desired nanowire electrical properties.
- **Si integration**
  - Find growth and processing techniques where nanowires can be grown on Si.
  - Avoid use of CMOS incompatible materials such as gold.

Main results and conclusions:

General growth control

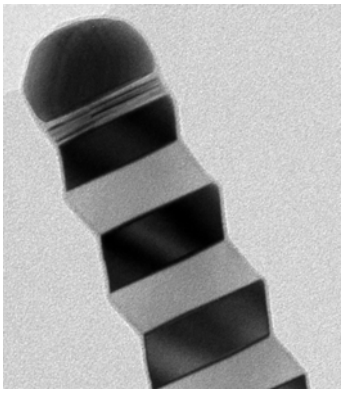
Controlling the crystal structure of InAs nanowires (LU) Gold-particle seeded nanowires fabricated in materials with zinc blende as the bulk crystal structure are often observed to have wurtzite crystal structure. The general trend is that thin wires are wurtzite and thick wires are zinc blende. That is, there is a cross-over diameter for the preferential polytype. This cross-over diameter is temperature dependent. By carefully varying the temperature during growth we were able to fabricate superlattices with alternating zinc blende and wurtzite structure.[1]



The figure shows a polytypic superlattice, with alternating zinc blende and wurtzite structure, along an InAs nanowire.

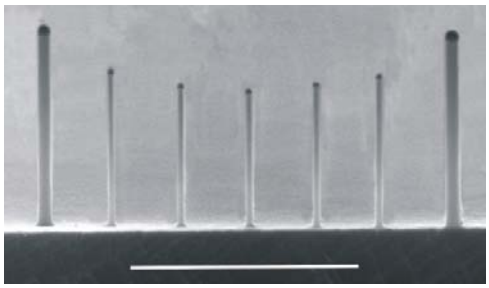
[1] P. Caroff *et al.* Nature Nanotech. **4**, 50 (2009)

Crystal phase and twin superlattices (PRE). The crystal phase of III-Vs NWs can be determined by the dopant precursor flows during growth. In InP the use of Zn-precursor favors the ZB phase, whereas the use of S-precursor favors the Wz phase. Moreover, highly regular twin superlattices can be induced in the ZB phase by tuning the Zn concentration, wire diameter and supersaturation. The effect was explained in a model based on surface energy arguments.[2]



The figure shows a TEM image of the top part of an InP NW, closely below the Au catalyst particle, showing the highly regular twin superlattice structure .

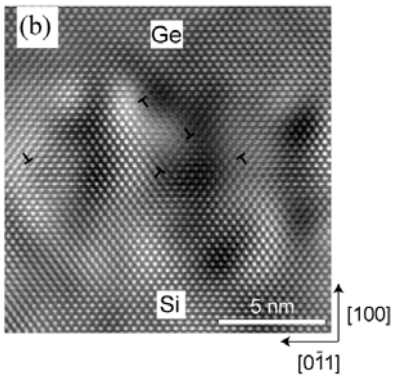
Synergetic growth (PRE). A counter-intuitive effect controlling the influence of wire spacing on growth rate was uncovered, synergetic growth, which implies that at smaller spacing the competition for available material, reducing the growth rate, is counteracted by the increase in surface density of catalyst metal particles on neighboring nanowires, providing more decomposed material.[3]



The figure shows that GaP wires next to a thick wire are taller than the second-nearest wires, which are taller than those in the middle of the field (furthest from the thick wire), showing that the growth rate of one wire is enhanced by the presence of another one and dependent on the catalytic alloy amount.

Heterostructures

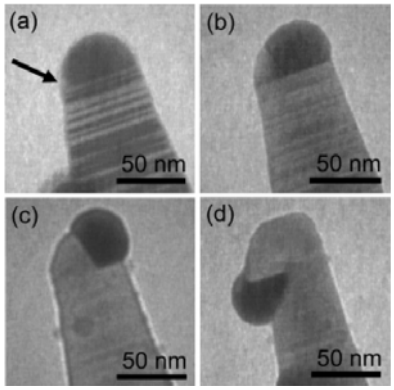
Epitaxial Ge/Si nanowires (MPI). Epitaxial Ge/Si hetero-structure nanowires on Si (100) substrates were prepared in AAO templates. Usually, the Si atoms dissolved in the Au/Si eutectic catalyst act as a reservoir for Si, and the interface to Ge is smeared out. Our new approach of the growth inside the AAO templates, allowed to produce a sharp interface of Ge/Si without changing the diameter of the nanowire.[4]



The figure shows a cross-section TEM image of the Ge-Si interface.

[2]R.E. Algra, *et al.*, Nature **456**, 369 (2008)
[3]M.T. Borgström *et al.*, Nature Nanotech. **2**, 541 (2007)
[4]T. Shimizu *et al.*, *Nano Lett.* **9**, 1523 (2009)

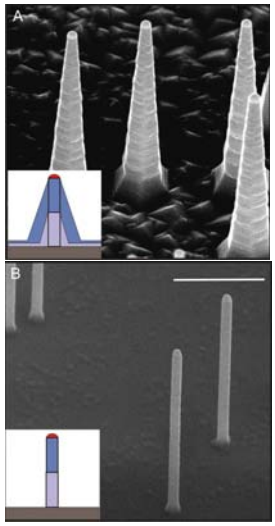
Morphology of axial heterostructures (LU). We have carried out an extensive investigation of the epitaxial growth of Au-assisted axial heterostructure nanowires composed of group IV and III−V materials and derived a model to explain the overall morphology of such wires. [5] By analogy with 2D epitaxial growth, this model relates the wire morphology (i.e., whether it is kinked or straight) to the relationship of the interface energies between the two materials and the particle. This model suggests that, for any pair of materials, it should be easier to form a straight wire with one interface direction than the other, and we demonstrate this for the material combinations presented here.



The figure shows images recorded during the growth of Ge on GaP nanowires by UHV-CVD.

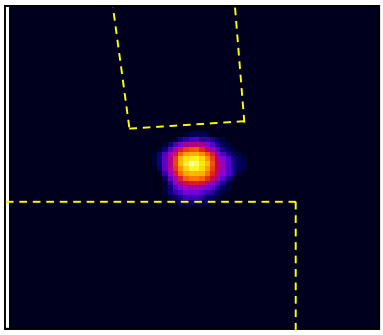
Doping

Decoupling the radial from the axial growth rate by in situ etching (LU)
We showed that *in-situ* etching can be used to decouple the axial from the radial nanowire growth mechanism, independent of other growth parameters. Thereby a wide range of growth parameters can be explored to improve the nanowire properties without concern of tapering or excess structural defects formed during radial growth. We used HCl as the etching agent during InP nanowire growth, and etched nanowires show improved crystal quality as compared to non etched and tapered NWs. These results will make way for devices relying on doping in axial structures, where any radial overgrowth would lead to short circuiting of a device.



The figure shows a) tapered reference InP nanowires grown at a temperature of 450ºC b) non tapered nanowires grown with HCl in the gas phase under otherwise identical growth conditions to a).

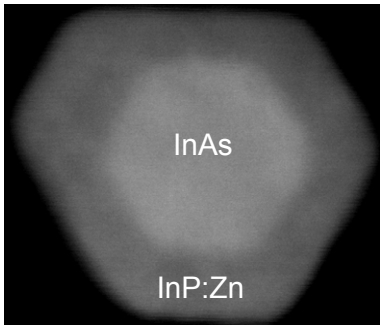
p-type doping and p-n junctions in InP NWs (PRE). Sulphur was identified as a suitable candidate for n-type doping of InP in MOVPE using H_2S as a precursor. It was further established that Zn-doping can be effectively used to achieve p-type doping in InP, using trimethylzinc as a precursor. The combination of S and Zn permits realization of *p-n junctions* in InP, showing good electrical diode characteristics in thin (20 nm-diameter) nanowires. The diodes exhibit LED behavior, testifying the high quality of the p-n junctions.[6]



The figure shows the optical microscope image of electroluminescent light coming from an InP NW LED, as collected by a CCD camera (the dashed lines show the positions of the electrodes).

[5]K.A. Dick *et al.* Nano Lett. **7**, 1817 (2007)
[6]E.D. Minot *et al.* Nano Lett. **7**, 367 (2007)

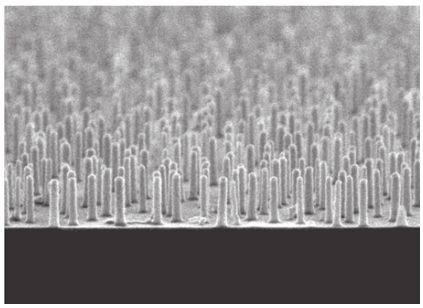
Remote p-type doping of InAs NWs (PRE). Obtaining quantitative control of doping levels in nanowires grown by the vapor-liquid-solid (VLS) mechanism is especially challenging for the case of p-type doping of InAs wires because of the Fermi level pinning around 0.1 eV above the conduction band. It was shown that growing a Zn-doped shell of InP epitaxially on a core InAs NW yields remote p-type doping: shielding with a p-doped InP shell compensates for the built-in potential and donates free holes to the InAs core. The effect of shielding critically depends on the thickness of the InP capping layer and the dopant concentration in the shell.[7]



The figure shows a dark-field TEM image of the InAs(core)/InP:Zn(shell) NW.

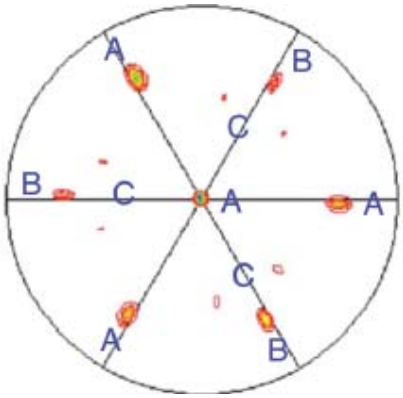
Si integration

Al as catalyst for Si nanowires (MPI). Replacement of Au by other catalysts was one of the main efforts of our work. The metal Al was successfully used as a catalyst at low growth temperature in the VSS mode for growth of freestanding Si nanowires. The template-assisted growth using AAO and Al catalyst allowed to grow (100) oriented Si nanowires.[8]



The figure shows Si nanowires grown by use of a Al catalyst

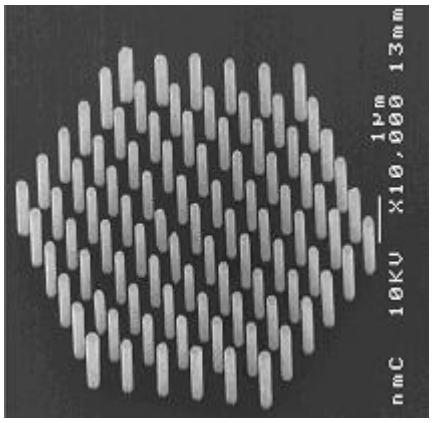
Epitaxial growth of III-V NWs on Si and Ge (PRE). The growth of GaAs, GaP, InAs, and InP nanowires on Si and Ge substrates was investigated extensively , and high-quality epitaxial growth was demonstrated for these materials systems. It was shown that the orientation of the epitaxial nanowires depends on the substrate-wire lattice mismatch.[9]



The figure shows X-ray diffraction pole measurements on InP wires grown on Si(111), showing the presence of InP(111) reflections originating from the wires.

[7]H.-Y. Li *et al,*. Nano Lett. **7**, 1144 (2007)
[8]Y.W. Wang *et al.*, *Nature Nanotech.*, **1,** 186 (2006); Z. Zhang et al., Adv. Mater.
[9]E.P.A.M. Bakkers *et al.,* MRS Bulletin **32**, 117 (2007).

Au-free InAs nanowires on silicon (LU) Narrow bandgap materials, such as InAs, could have great impact on future nano-electronics if integrated with Si, but integration has so far been hard to realize. We have shown that InAs nanowires can be grown directly on silicon substrates using a method employing self-assembled organic coatings to create oxide-based growth templates.[10] The method was subsequently modified to also allow for position-control, which is required for vertical device implementation.



The figure shows epitaxial InAs nanowires grown on a Si(111) substrate from holes etched in a SiO_2 film.

[10]T. Mårtensson *et al.* Adv. Mat. **19**, 1801, (2007)

Work-package 2: Nanoprocessing

The overall objective of this workpackage was to provide a technological basis for the fabrication of nanowires devices. WP2 provided samples with patterned seeds or templates for the nanowire growth in WP1. Nanowires grown by the groups in WP1 were used to fabricate nanowire devices, which were passed on to WP3 for basic physics characterization or to WP4 and WP5 for device characterization.

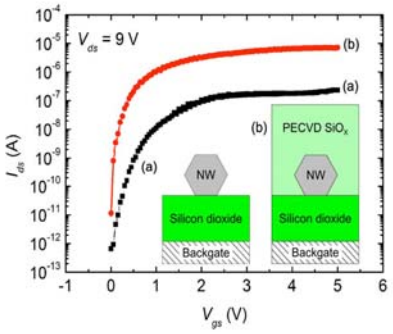
Specific tasks concerned:

- **Surface passivation and gate dielectrics**
- **Contacts and gates for nanowire FETs**
- **Processing of vertical nanowire devices**

Main results and conclusions:

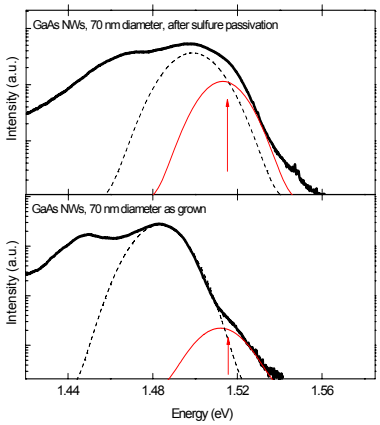
Surface passivation and gate dielectrics

Lateral nanowire n-MOSFETs (IBM). Fully depleted lateral n-channel MOSFET devices were fabricated using implantation for source and drain regions. Strong inversion and clear saturation currents are observed in FETs from intrinsic NWs with p-implanted source/drain regions, whereas NWFETs with Schottky contacts only operate in accumulation mode. The effect of surface preparation on the electrical characteristics were studied and revealed that encapsulating the devices in a protective oxide yields significantly increased on currents and steeper sub-threshold swings.[11] This analysis reveals the strong influence of the electrostatics on the transport properties and shows that the extraction of device parameters using conventional models may not be valid.



The figure shows the transfer characteristic of a lateral nanowire n-MOSFET as fabricated surrounded by air (black) and encapsulated in SiO_2.

Chemical passivation of nanowires (WU) The large surface to volume ratio of nanowires makes them very sensitive to surface effects such as nonradiative recombination centers or trapped charges. Surface passivation of GaAs nanowires by difference chemical treatments has been investigated and an improvement of the luminescence efficiency by a factor of 40 compared to as-grown wires could be achieved.

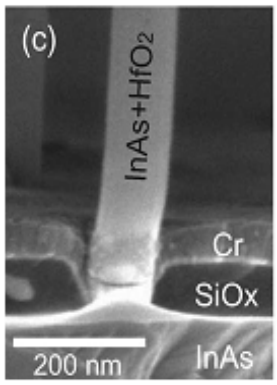


The figure shows the photoluminescence spectrum of an as grown (bottom) and a passivated wire (top)

[11] O. Hayden *et al.*, *Small*, **3**, p. 230, 2007.

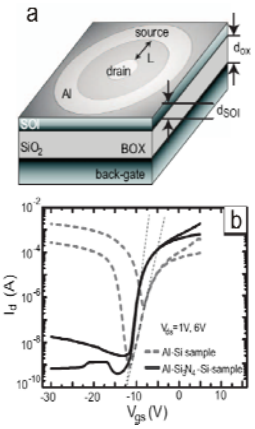
Contacts and gates for nanowire FETs

50 nm L_g Wrap Gate InAs MOSFET (QM). Wrap Gated, or gate all around devices show the best control of the channel potential. We successfully fabricated InAs high-κ (HfO_2) oxide nanowire field effect transistor, with a 50 nm long wrap gate. The first transistors were based on InAs wires grown on a n^+ InAs substrate. The high mobility and injection velocity of the InAs channel leads to a good drive current and excellent transconductance. [12]



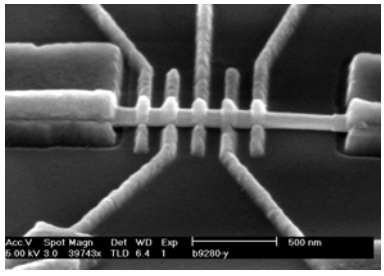
The figure shows a cross section of the MOSFET, showing the 50 nm Cr gate around the InAs nanowire.

Schottky barrier FETs (IBM). The use of thin Si_3N_4 interface layers between the silicon and metal contacts were shown to give Ohmic contacts whereas without the Si_3N_4 a normal Schottky contact was achieved. Furthermore, it was demonstrated that the Si_3N_4 interface layer gives Schottky barrier FETs with suppressed ambipolar behaviour due to a reduction in metal induced gap states. [13]



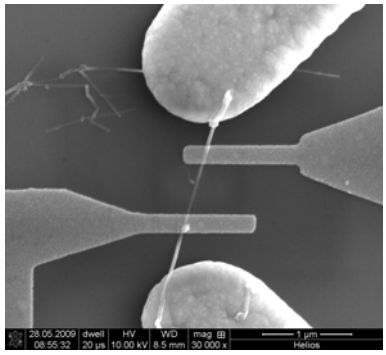
The figure shows a schematic of a Schottky barrier pseudo-MOSFET and the corresponding transfer characteristics with and without an interface layer.

Multiple gates for nanowire devices (TUD)
Nanowires with multiple gates on horizontal nanowires have been developed to create electrical quantum dots in InAs/InP nanowires. These devices are used to investigate quantum effects in coupled quantum dots nanowire**s[14].**



The figure shows a horizontal InAs/InP nanowire with multiple gates.

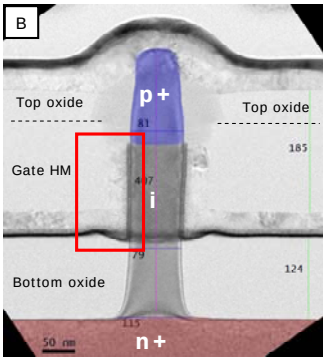
Nanowire FET with gated Schottky contact (WU, NL) Gated Schottky contacts allow a control over the polarity of the injected carriers, allowing to switch the operation of a nanowire FET from n-type to p-type. Such devices can be used to realize complementary logic without doping the nanowires.

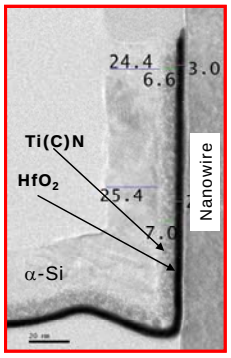


The figure shows a Si-nanowire FET with two gated Schottky contacts.

[12] C. Thelander *et al.* IEEE Electron Device Lett. 2008
[13] H. Ghoneim *et al.*, Proceedings of ULIS conference 2009.
[14] M. Scheffler *et al.*, Physica E **40**, 12020-01204 (2008)

Wrap-around gate vertical Si nanowire Tunnel-FETs (IMEC). We successfully developed a CMOS compatible process flow to fabricate vertical Si nanowire Tunnel-FETs using state-of-the-art processing tools onto 200mm wafers. An advanced gate stack using high-κ (HfO_2) oxide and metal gate (TiN) was implemented. The top contact was obtained by isotropic dry etch of the gate stack at the top of the wire using a gate hardmask. The gate is isolated from the substrate by a thick oxide layer. It is also isolated from the top contact by a nitride spacer and oxide layer. A capping layer connects multiple wires together. Top contact doping is achieved through epitaxial layer or tilted implants.

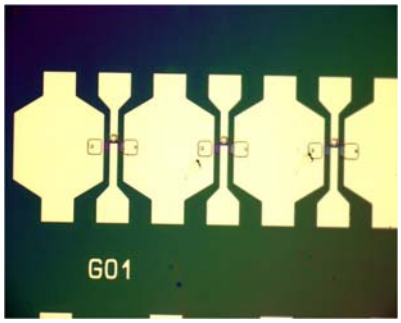




The figure shows a cross section of the vertical TFET featuring 3nm HfO_2, 7nm TiN and 25nm a-Si gate stack around the nanowires.

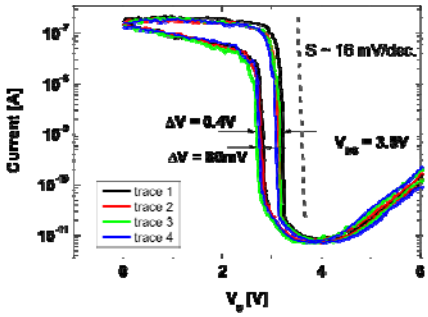
Processing of vertical nanowire devices

InAs Wrap Gated MOSFETs for RF and circuit applications (QM/LU). For RF and circuit applications, the transistors need to be integrated on an highly resistive, or insulating substrate. We developed here a technology for growing, and locally contacting InAs nanowires on a semi insulating InP substrate. The technology is based on a local ohmic substrate contact, which wraps around the base of the nanowires. This allows for RF characterization of the InAs MOSFETs, with first results of f_t=7 GHz and f_{max}=22 GHz.[15]



The figure shows a top view of a fully processed RF-compatible vertical nanowire transistor structure.

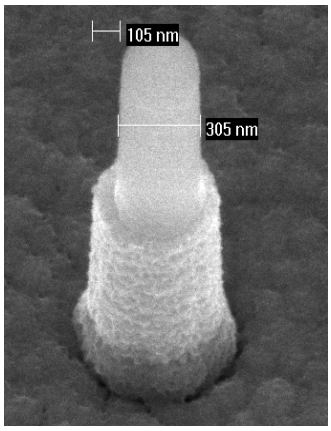
Vertical Impact Ionization MOS FETs (IBM-ZRL). A process for vertical silicon nanowire FETs was developed. Using this process vertical impact ionization FETs with sub-threshold swings down to 5 mV/dec. were demonstrated.[16] Please write a sentence about the improved stability to motivate and explain the picture.



The figure shows the stability of the transfer characteristics of a vertical IMOS FET.

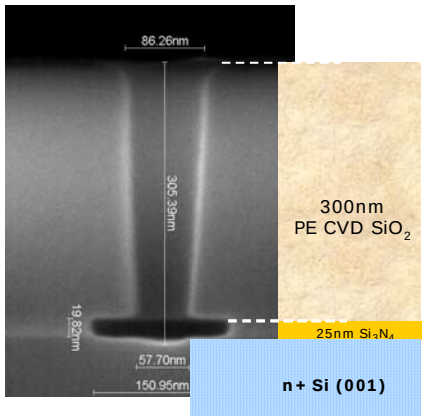
[15] M. Egard *et al.* submitted to Nano Lett. 2009
[16] M. T. Björk *et al.*, Appl. Phys. Lett. **90**, 142110 (2007)

Nanowires based spin memory (TUD) We created a spin memory in a single quantum dot embedded in an InP nanowire. The preparation of a given spin state by tuning excitation polarization or excitation energy demonstrated the potential of this system to form a quantum interface between photons and electrons. For this purpose, transparent contacts on vertical nanowires have been developed for FET devices and are currently under investigation[17].



The figure shows a vertical nanowire surrounded by a dielectric and a wrap gate.

SiO_2 template development for catalyst-free nanowire growth (IMEC). A process was developed to fabricate hole patterns on top of silicon for constrained growth of Si nanowires, without the use of catalyst. The template was prepared by patterning a plasma–enhanced chemical-vapor deposited (PE CVD) Si_3N_4/SiO_2 25nm/300nm film stack with openings or holes to expose the underlying Si. The patterning was performed through 193nm lithography and etching of the SiO_2 with Motif®, an advanced dry etch technique capable of shrinking printed feature sizes thanks to the deposition of a polymeric coating on top of the developed resist. Particular care was dedicated to cleaning of the side walls and the silicon bottom substrate to avoid defects creation during subsequent growth. To achieve suitable Si purity for epitaxial growth, a special sequence of process steps was needed to avoid Si contamination by carbon residues from etch.



The figure shows the cross-section of a via hole after plasma etch and hot phosphor opening of the Si_3N_4 bottom layer.

[17] H.M. Maarten *et al.,* Small **5**, pp. 2134 – 2138 (2009)

Work-package 3: Physics and Characterization

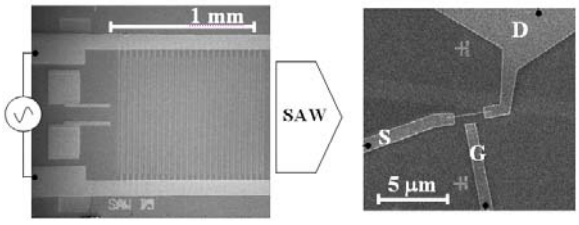
WP3 aimed for a thorough understanding of the physical properties of the nanowires that were required to achieve the overall goals of NODE. Thus WP3 used different experimental techniques to characterize and model the nanowires supplied by WP1.
The over-all objectives of this work-package were divided into four categories:

- **Electrical properties**
  - Room temperature transport
  - Effect of diameter dependence and surface passivation
- **Optical studies**
  - Assess intrinsic and extrinsic NW properties relevant for nanowire-based devices
  - Investigate the impact of surface modification on the optical properties of NWs
  - Raman and mid-IR spectroscopy
- **X-ray structural characterization**
  - Quantify the strain and composition in longitudinal and radial NW assemblies.
  - Development of X-ray techniques to study NWs: defects and single object studies.
- **Modeling**
  - Band structure calculation and evaluation of transport properties.
  - Effect of dielectric environment

Main results and conclusions:

Electrical properties

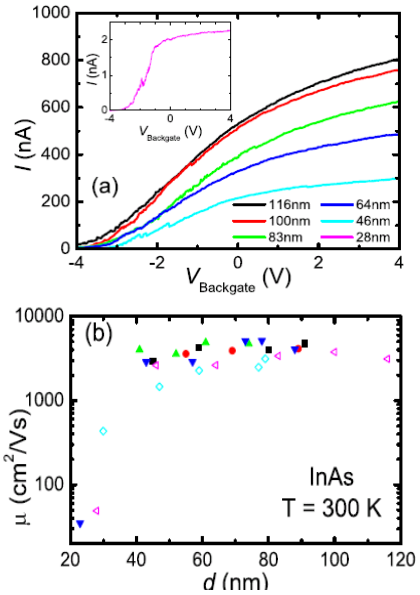
Room temperature transport (SNS). Room temperature transport properties of bare InAs and InAs/InP core shell nanowires[18] have been studied and a three dimensional electrostatic model was developed to compute the NW FET capacitance for a more accurate mobility determination. The measured values ranged in the 1-2 thousand cm^2/Vs for the thinnest wires (< 40 nm), while reached about 3 thousand for thicker wires. Remarkably all the wires showed relatively low values of electronic charge in the few 10^{16} cm^{-3} range. The highly Se-doped wires revealed an attendant strong increase in charge density up to ~ $1x10^{19}$ cm^{-3}; as expected the impurities introduced brought along a decrease in the mobility, which varied in the 4-6 hundred cm^2/Vs range for wire diameters of 40-50 nm. In parallel, NW devices were fabricated for charge pumping through surface acoustic waves (SAW)[19]. The NW FETs were implemented on top a $LiNbO_3$ substrate with piezoelectric transducers. An acoustoelectric current peak in the wire was identified when driving the transducer near its resonance frequency. This type of devices is quite interesting both for analog signal processing and for the implementation of single-photon sources under quantized charge pumping.
Furthermore, it yields a new direct method to measure the carrier mobility by observing the bias point at which the acoustoelectric peak in the current changes of sign, signaling that drift and acoustic wave velocity are the same.



Sketch of the device and set-up for the induction of acoustoelectric current in NW FETs.

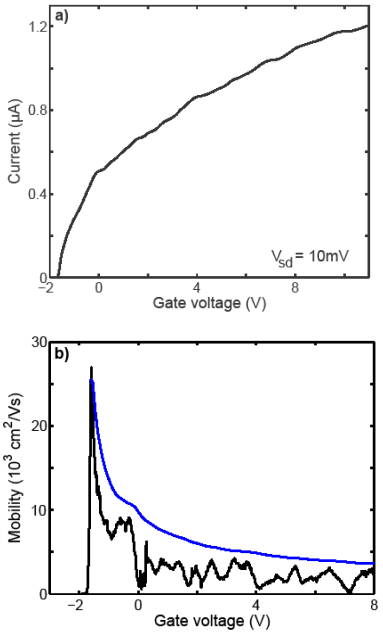
[18] S. Roddaro *et al.*,Nanotechnology 20**,** 285303 (2009).
[19] S. Roddaro *et al.*, submitted to Semicond. Science Tech.

Diameter dependence of tapered InAs nanowires [20] ***(TUD, PRE).*** Electrical conductance through InAs nanowires is relevant for electronic applications as well as for fundamental quantum experiments. Nominally undoped, slightly tapered InAs nanowires were used to study the diameter dependence of their conductance. Contacting multiple sections of each wire, we can study the diameter dependence within individual wires without the need to compare different nanowire batches. At room temperature we find a diameter-independent conductivity for diameters larger than 40nm, indicative of three-dimensional diffusive transport. For smaller diameters, the resistance increases considerably, in coincidence with a strong suppression of the mobility. From an analysis of the effective charge carrier density, we find indications for a surface accumulation layer.



The figure shows (a) the backgate sweeps for different sections within the same nanowire. The inset shows the data for the section with the smallest diameter. (b) the mobility determined from backgate sweeps. Different symbols correspond to the different devices studied.

Surface passivation of InAs nanowires by an ultrathin InP shell [21] ***(TUD, PRE).*** We report the growth and characterization of InAs nanowires capped with a 0.5-1nm epitaxial InP shell. The low temperature field-effect mobility is increased by a factor 2-5 compared to bare InAs nanowires. We also report the highest low temperature peak electron mobilities obtained for nanowires to this date, exceeding 20 000 cm2/Vs. The electron density in the nanowires, determined at zero gate voltage, is reduced by an order of magnitude compared to uncapped InAs nanowires. For smaller diameter nanowires we found an increase in electron density, which can be related to the presence of an accumulation layer at the InAs/InP interface. However, compared to the surface accumulation layer in uncapped InAs, this electron density is much reduced. We suggest that the increase in the observed field-effect mobility can be attributed to an increase of conduction through the inner part of the nanowire and a reduction of the contribution of electrons from the low mobility accumulation layer. Furthermore we found that by growing an InP shell around an InAs core, surface roughness scattering and ionized impurity scattering in the accumulation layer is reduced.

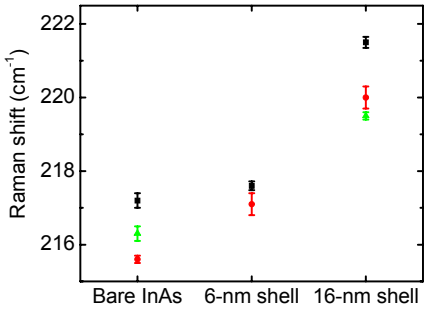


The figure shows (a) pinch-off curve and (b) extracted field-effect (black) and effective mobilities (blue) of a high mobility core/shell nanowire

[20] M. Scheffler *et al.*, submitted to Journal of Applied Physics
[21] J. van Tilburg *et al.*, accepted for publication in Semiconductor Science and Technology

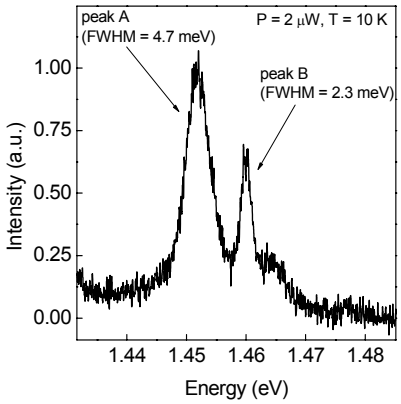
Optical studies

Raman and mid-IR spectroscopy (SNS). A micro-Raman set-up was developed and applied to InAs/InP core-shell structure, as a way to study the strain introduced in the structure and verify the reduced impact of surface states in the capped wires. A clear line width reduction was observed in wires with thick InP shells where less interaction with the surface was expected and a blue shift of the resonances with increasing shell thickness was also detected, which gives indication of the amount of strain in the InAs material.



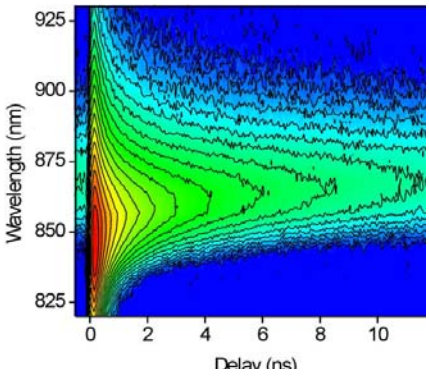
Energy position of the main transverse mode for NWs with different InP shells. Colours are used to distinguish among different wires in the same sample.

Micro photoluminescence studies of single InP nanowires (WU). The optical study of single nanowires provides important information about physical properties such as size quantization effects. Individual NWs show narrow emission lines with linewidths as low as 2.3 meV which reflects the high structural quality of the nanowires. Blueshifts of the NW emission energy between 25 and 56 meV with respect to bulk InP are related to radial carrier confinement in nanowires with diameters between 15 nm and 50 nm. Time resolved investigations reveal a low surface recombination velocity of 6×10^2 cm/s.[22]



Micro photoluminescence spectrum showing emission from two InP nanowires with narrow linewidths of 4.7 meV and 2.3 meV, respectively.

Study of surface capping of InP nanowires (WU, LU, QM). Time resolved photo-luminescence spectroscopy was applied to optimize the atomic layer deposition (ALD) of high-κ dielectrics (HfO_2, Al_2O_3) onto InP NWs – a process which typically leads to detrimental surface states. Applying a core/shell growth technique the InP surface quality could be significantly improved in terms of the surface recombination velocity S_0 which was reduced to $S_0 = 9.0\text{x}10^3$ cm/s in comparison with $S_0 = 1.5\text{x}10^4$ cm/s obtained for an untreated reference sample without surface treatment prior to ALD. In an alternative approach, in-situ post-growth annealing in H_2S atmosphere prior to ALD resulted in a nearly fourfold decrease of S_0. These results clearly show the importance of a proper surface treatment prior to oxide capping of III/V NWs for transistor applications.

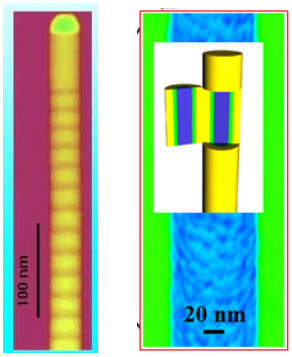


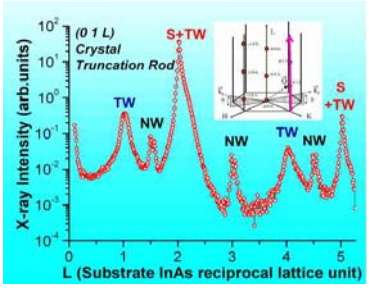
Spectrally and temporally resolved intensity map of the PL emission from HfO_2 capped InP NWs.

[22] S. Reitzenstein *et al.*, Appl. Phys. Lett. 91, 091103 (2007)

X-ray characterization

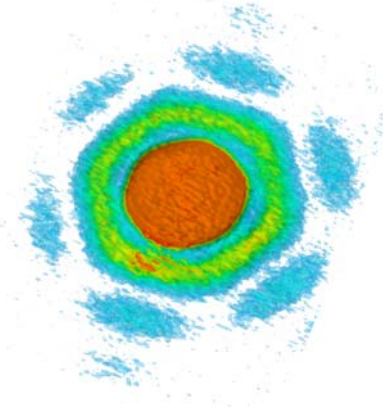
Study of radial and longitudinal heterostructures (CEA, LU, QuMat). Quantitative structural information about epitaxial arrays of VLS-NWs have been reported for a InAs/InP longitudinal[23] and core-shell[24] heterostructure grown InAs (111)B substrates. Grazing incidence X-ray diffraction allows the separation of the nanowire contribution from the substrate overgrowth and gives averaged information about crystallographic phases, stacking defects, epitaxial relationships with orientation distributions, and strain. The strain profiles have been compared to atomistic and finite element calculations performed at CEA, and Grazing Incidence Small Angles Scattering has been used to extract the shape, diameter and variability of the NWs.





Longitudinal and radial heterostructures measured by Grazing Incidence X-ray Techniques and example of a truncation rod measurement showing the [111] stacking in a longitudinal InAs/InP heterostructure.

Single object studies (CEA). The measurement of single NWs with coherent imaging techniques has been developed. This new technique gains insights into the *shape* of the objects[25], but also into the *strain* distribution inside one object. Original structural results obtained on sSOI lines with micro-focussed beams have been obtained (unpublished results) as well as the application of this technique to VLS grown samples.



Coherent diffraction of single 95 nm Si nanowire (111) Bragg reflection. The "ab initio" analysis of this pattern allows reconstructing the shape of the NW.

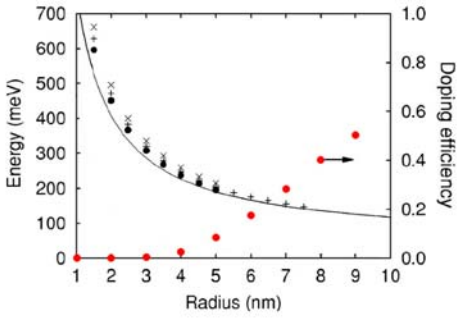
Modelling

Band structure calculations (CEA, LU). The band structure of group IV and various III-V NWs has actually been investigated in the whole 2-40 nm diameter range. The size dependence of the bandgap energy, subband splittings and effective masses has been discussed in detail [26] and used in collaboration with Lund for the modelling of InAs NW field-effect transistors.[27] Finally, the CEA has investigated the effects of strains on the electronic properties of III-V nanowire heterostructures (e.g., the reduction of the barrier height in tunnel devices).[28]

[23] J. Eymery *et al.*, Nano Letters 7 (9) 2596 (2007).
[24] J. Eymery *et al.*, Appl. Phys. Lett. 94**,** 131911 (2009).
[25] V. Favre-Nicolin *et al.*, Phys. Rev. B 79, 195401 (2009).
[26] Y. M. Niquet *et al.*, Phys. Rev. B 73, 165319 (2006).
[27] E. Lind *et al.*, IEEE Trans. Electron Devices 56, 201 (2009).
[28] Y. M. Niquet and D. Camacho Mojica, Phys. Rev. B 77, 115316 (2008).

Transport properties (CEA). The transport properties of ultimate silicon nanowires with diameters < 6 nm has been modeled using quantum Kubo-Greenwood and Green function methods. The impact of surface roughness[29] and dopant impurities on the mobility has been studied. The CEA has shown, in particular, that the impurity-limited contribution to the mobility could be larger in wrap-gate nanowires than in bulk due to the efficient screening of ionized impurities by the gate. Also, the resistance of single impurities can be very dependent on their radial position in the nanowire, leading to significant variability in ultimate devices.

Effect of dielectric environment on the electrical properties (CEA, CNRS/IEMN, LU). We showed that the dielectric confinement can be responsible for a significant decrease of the doping efficiency in nanowires.[30] Dopant impurities are progressively "unscreened" by image charge effects when reducing wire diameter, which leads to an increase of their binding energies and decrease of their activity. These predictions have been confirmed by recent experiments by the IBM group. The binding energies of shallow impurities are however very sensitive to the dielectric environment of the nanowires, and can be decreased by embedding the wires in high-k oxides or wrap-gates. Modelling has confirmed that many electronic properties of semiconductor nanowires are driven more by dielectric than quantum confinement, even in the sub 10 nm range, showing the importance of the "electrostatic" engineering of nanowire devices.



The figure shows the binding energy of various donors (black symbols, left axis) as a function of the radius R of silicon NWs in vacuum, and room temperature doping efficiency of P donors (red symbols, right axis). The doping efficiency rapidly decreases below R = 10 nm.

[29] M. P. Persson *et al.*, Nano Letters 8, 4146 (2008).
[30] M. Diarra *et al.*, Phys. Rev. B 75, 045301 (2007).

Work-package 4: Nanowire Devices

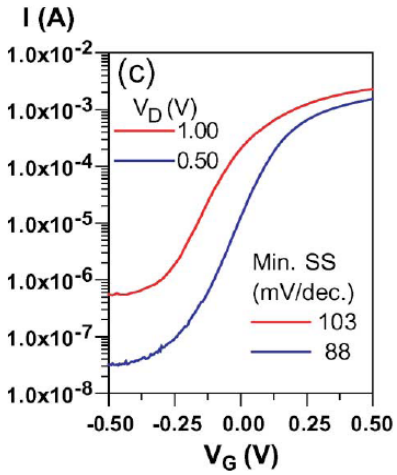
The overall objective of this work package was to develop *nanowire-based electronic devices* built on the knowledge established in deliverables WP1-3. We have explored to what extent nanowire (NW)-based devices can realize their potential as future PostCMOS logic. The work was divided into two main tracks:

1. **InAs-track:**
   - InAs FETs
   - other InAs- and III/V-based devices: memory elements, capacitors
2. **Si-track:**
   - Si FETs

Main results and conclusions:

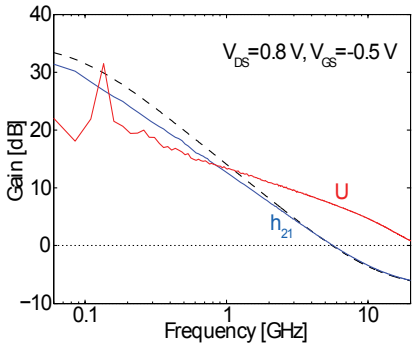
InAs FETs

Vertical InAs transistors (LU/QM). We have developed fabrication of vertical InAs nanowire wrap-gate field-effect transistor arrays with a gate length of 50 nm.[31] The wrap gate is defined by evaporation of 50-nm Cr onto a 10-nm-thick HfO_2 gate dielectric, where the gate is also separated from the source contact with a 100-nm SiO_X spacer layer. For a drain voltage of 0.5 V, we observe a normalized transconductance of 0.5 S/mm, a subthreshold slope around 90 mV/dec., and a threshold voltage just above 0 V.



The figure shows the sub-threshold I-V characteristics of an array of 55 vertical InAs nanowires.

RF characterization of vertical InAs transistors (LU/QM). In collaboration with QM, we have developed an RF compatible vertical InAs nanowire process, with InAs wires grown on S.I. InP substrates. By combining 70 wires in parallel in a 50Ω waveguide pad geometry, we measured S-parameters (50MHz-20 GHz) for vertical InAs nanowire MOSFETs. A maximum f_t of 7GHz and f_{max}=22GHz[32] was obtained. Small signal modeling allowed for the first extraction of intrinsic device elements forming a hybrid-π equivalent circuit.

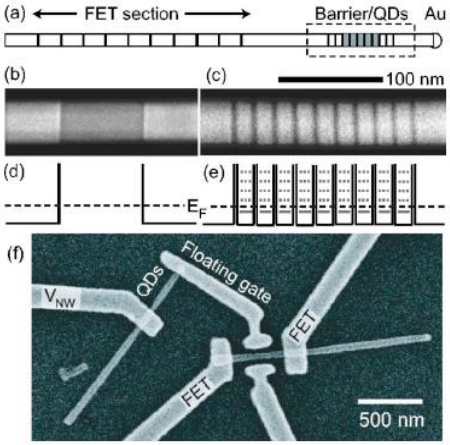


The figure shows measured and modeled RF gains for a 90 nm gate length InAs MOSFET..

[31] C. Thelander *et al.* IEEE Electron Dev. Lett. **29**, 206 (2008)
[32] M. Egard *et al.*, submitted to Nano Lett.

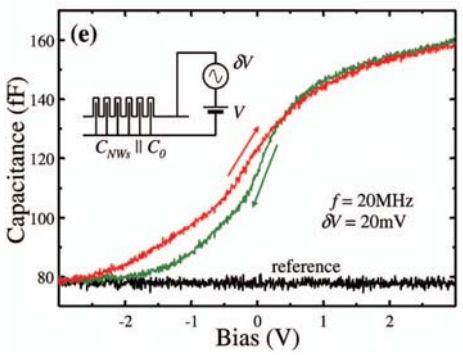
Other InAs- and III/V-based devices

Nanowire-based multiple quantum dot memory (LU). We demonstrate an alternative memory concept in which a storage island is connected to a nanowire containing a stack of nine InAs quantum dots, each separated by thin InP tunnel barriers.[33] Transport through the quantum dot structure is suppressed for a particular biasing window due to misalignment of the energy levels. This leads to hysteresis in the charging & discharging of the storage island. The memory operates for temperatures up to around 150 K and has write times down to at least 15 ns. A comparison is made to a nanowire memory based on a single, thick InP barrier.



The figure shows the design and implementation of a multiple quantum dot memory based on nanowires.

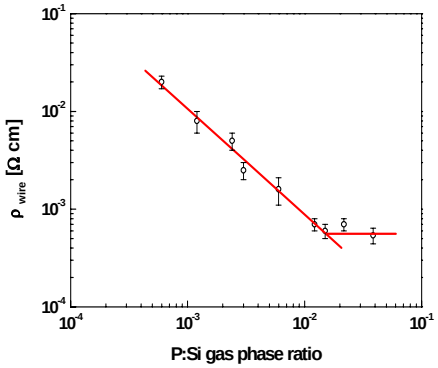
Nanowire capacitors (LU). Vertical InAs nanowire capacitors have been developed based on arrays of nanowires, high-k deposition, and metal deposition.[34] The capacitors show a large modulation of the capacitance with the gate bias, and a limited hysteresis at 0.5 V voltage swing. Via modeling of the charge distribution in the nanowires as a function of the applied voltage, the regions of accumulation, depletion, and inversion have been identified. Finally, the carrier concentration has been determined.



The figure shows measured CV profile at 20 MHz.

Si FETs

Doping limits in silicon nanowires (IBM). The control over doping levels was demonstrated for in-situ doped silicon nanowires using phosphine as the doping source. It was found that the maximum attainable doping is 1×10^{20} cm^{-3} limited by the solid solubility limit of phosphorous in silicon at the growth temperature (450C).[35]

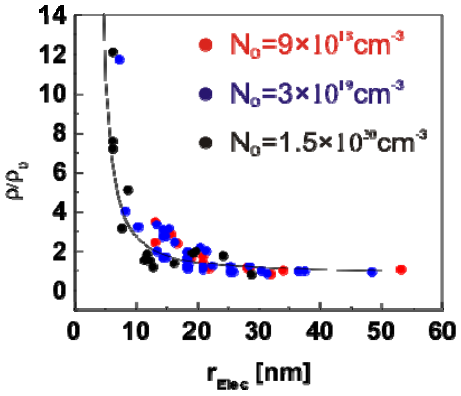


The figure shows the experimental data of nanowire resistivity vs phosphine concentration. Donor densities up to the solid solubility limit of phosphorous in silicon was achieved.

[33] H. N. Nilsson *et al.*Appl. Phys. Lett **89**, 163101 (2006)
[34] S. Roddaro *et al*. Appl. Phys.Lett. **92**, 253509 (2008)
[35] H. Schmid *et al.*, Nano Lett. **9**, 173 (2009).

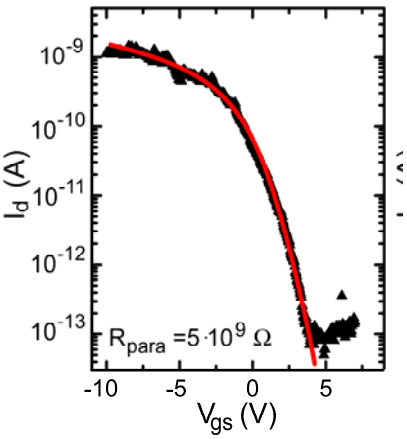
Doping deactivation (IBM). It was demonstrated experimentally that dopants inside scaled semiconductors experience a smaller screening as a function of decreasing size leading to a deactivation of the dopants. This effect is caused by a dielectric mismatch between the semiconductor and the surrounding medium.[36]

The figure shows how the resistivity of silicon nanowires increases with decreasing diameter due to doping deactivation caused by a dielectric mismatch between the nanowire core and the surroundings.



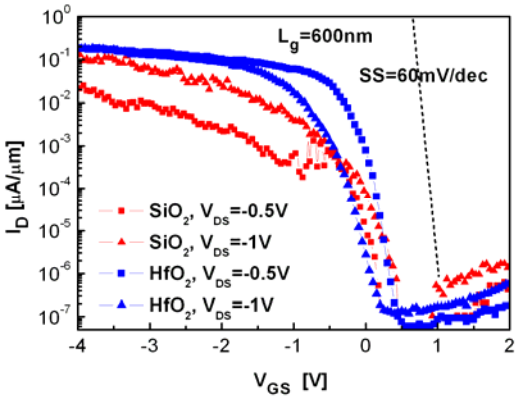
Silicon nanowire tunnel FETs (IBM). Tunnel FETs based on silicon nanowires were demonstrated for the first time. The FET structure was grown by the VLS method and doping was incorporated in-situ. The devices were fabricated in a lateral fashion with both a top and bottom gate. The data obtained on the FETs matched the expected sub-threshold slopes as modeled by a simple WKB approximation.[37]

The figure shows the transfer characteristics of a Si NW tunnel FET with top gate. The red line is calculated using the WKB approximation.



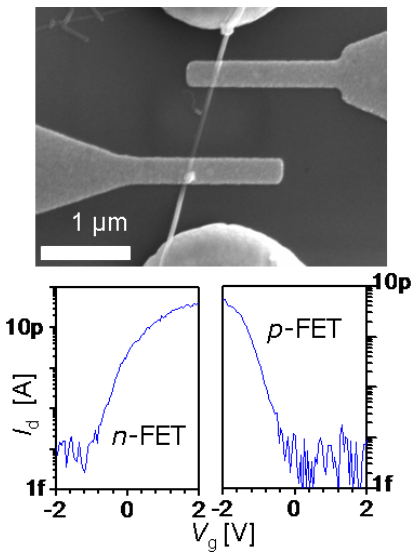
State-of-the-art all-silicon tunnel FETs (IBM). All-silicon nanowire tunnel FETs with high on-currents were demonstrated. The use of a high-k gate dielectric markedly improves the TFET performance in terms of average slope SS (SS measured between 10^{-7}μA/μm and 10^{-3}μA/μm is 120mV/dec.) and on-current, I_{on} (0.3μA/μm). The performance of the devices is close to what can be expected from all-silicon tunnel FETs.[38]

The figure shows the transfer characteristics of silicon nanowire tunnel FETs with SiO_2 (red) and HfO_2 (blue) gate dielectrics.



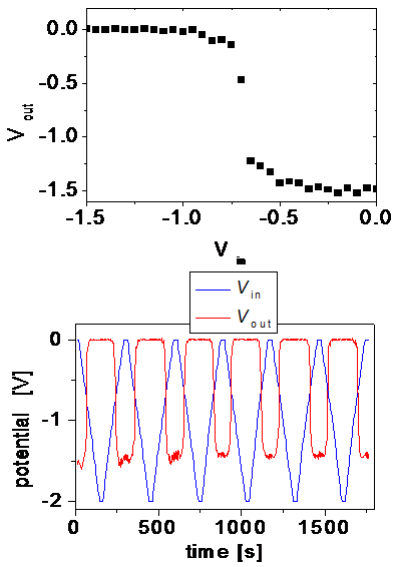
[36] M. T. Björk *et al.*, Nature Nanotechn. **4**, 103 (2009)
[37] M. T. Björk *et al.*, Appl. Phys. Lett. **92**, 193504 (2008).
[38] K. E. Moselund *et al.*, ESSDERC, September 2009.

Dopant-free polarity control of Si nanowire Schottky FETs (NL). The accurate and reproducible adjustment of the charge carrier concentration in nanometer-scale semiconductors is challenging. As an alternative to transistors containing doping profiles, dopant-free nanowire transistors have been devised. The source and drain regions are replaced by metal contacts that exhibit a sharp interface to the active region. The current flow is controlled by locally adjusting the electric field at the metal/silicon interface. Independent control of each contact results in transistors that can operate either as p- or n-type.[39]



The figure shows a silicon nanowire FET with two independent top gates, each coupling to a metal/semiconductor junction. The FET can be programmed as p- and n- type.

Complementary logic circuits built from undoped Si nanowire Schottky FETs (NL). To reduce the static power consumption of digital circuits complementary logic is required. This is enabled by the interconnection between p- and n- type transistors. Complementary nanowire based inverter circuits that do not require doping were developed and characterized. The results show that all logic functions can be performed at low power consumption without dopants. The entire thermal budget for processing is kept below 400°C, enabling a possible future replacement of low mobility organic printed circuits on flexible electronics



The figure shows silicon nanowire inverter characteristics; top: transfer characteristics, bottom: time resolved response.

[39] W. M. Weber *et al.* IEEE Proc. Nanotech. Conf. p.58*0* (2008)

Work-package 5: Benchmarking and integration

The work in WP5 was centered on *large-scale integration* of silicon-based nanowire devices and *evaluation* of vertical device architectures. During the first two years, paper study assessment were the main tools as preparations for full wafer implementation were ongoing: the requirements for the integration of grown nanowires in a CMOS environment were set and a list of allowed catalyst systems for nanowire growth were defined. Modeling and simulation was used as a tool to explore novel device concepts, optimize, predict and benchmark the device performance A tunnel-FET device was chosen as a promising vertical nanowire-device demonstrator. In the last two years of the project, the focus shifted to practical implementation and vertical device integration schemes were actively put to the test in the 200mm silicon processing facility at IMEC. Two routes were explored in parallel: while our researchers were looking for solutions for CMOS compatible growth of Si and SiGe nanowires, process development for wrapped-gate devices was done on etched vertical nanowires.

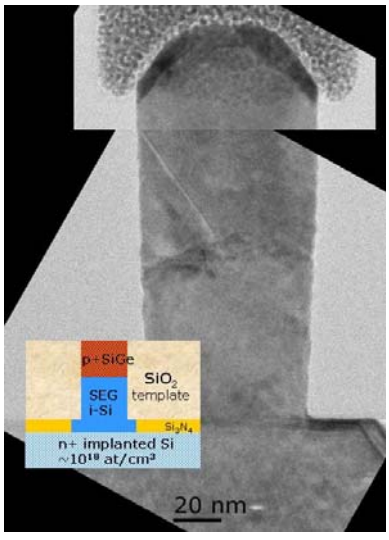
The over-all objectives of this work-package were divided into two main categories:

- **Process upscaling of nanowire growth and devices**
- CMOS compatible growth of nanowires (non-gold catalysts)
- CMOS compatible integration of nanowires
- Functional devices on full wafer validation
- **Vertical device architectures and benchmarking**
- Evaluation and benchmarking of vertical nanowire architecture
- Device and circuit modeling

Main results and conclusions:

Process upscaling of nanowire growth and devices

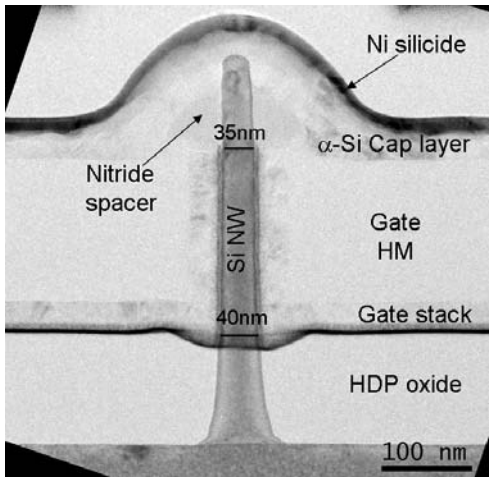
***Wafer-scale nanowire growth* (IMEC)** At first, catalyst-based growth of silicon vertical nanowire using none-gold catalyst systems was considered. Aluminum, which had been shown promising on coupon level tests (UHV-CVD at MPI), proved not up-scalable in the absence of UHV conditions. Indium particles did produce high-yield Si nanowires in PE-CVD but the growth was difficult to control. In view of the many limitations related to Vapor-Solid Liquid growth of silicon nanowires, a seedless (catalyst-free) constrained approach for growing Si and SiGe nanowires onto Si (100) substrates was developed. The growth approach takes advantage of the advances in Selective Epitaxial Growth (SEG) technology to fill the holes without the presence of catalytic metal particles. Nanowires with an intrinsic Si segment (channel) and p^+ -doped (B) segment of either Si, $Si_{0.85}Ge_{0.15}$ or $Si_{0.75}Ge_{0.25}$ (source) were successfully grown on top of n+-doped (100) substrates. [40]



The figure shows a TEM micrograph of a 60nm wide Si/SiGe heterojunction nanowire

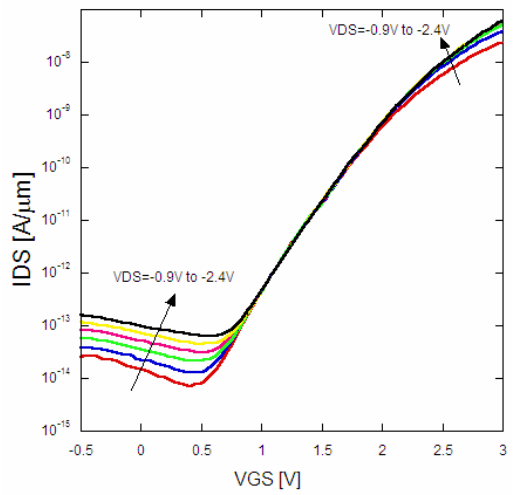
[40] F. Iacopi et.al., MRS Symposium Proceedings, Vol. 1178E.

***Large-scale nanowire device integration* (IMEC)** IMEC developed an integration flow together with the necessary process modules to fabricate vertical nanowire tunnel-FET devices with wrap-around gates. The nanowires were made by a top-down etch process, however, the integration flow is compatible with a bottom-up approach based on grown nanowires. Next to the wrap-around gate configuration which provides the best gate control over the channel, a vertical TFET architecture allows a more readily implementation of heterostructures which are needed to boost the tunneling current (see modeling part). Functional vertical nanowire TFET devices were built on a 200mm wafer platform.[41] Vertical integration implied, among other, the implementation of bottom and top isolation layers, and a amorphous Si capping layer which simultaneously connects the TiN metal gate.



The figure shows a TEM cross-section of the final vertical 35nm NW TFET device (no top oxide isolation) with an advanced a-Si/TiN/HfO_2 gate stack.

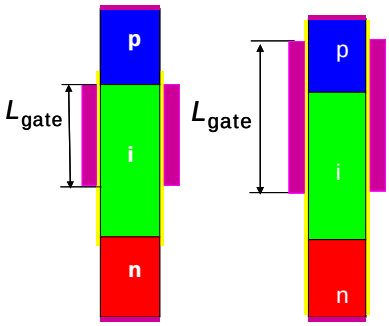
***Vertical nanowire TFET device* (IMEC)** Functional Si nanowire n- and p-TFETs were demonstrated and measured electrically at IMEC using a Kleindiek nanoprober apparatus mounted in a HRSEM (Fig.4). The experimental data are inline with literature data of all-Si Tunnel-FETs. To our knowledge, these devices are the first large-scale integrated vertical nanowire devices with state-of-the art high-k metal gate stack.[42]



The figure shows the input I_{ds}-V_{gs} characteristics of the n-TFET device with an epi grown P^+ source and a nanowire size of 50 nm on design

Vertical device architectures and benchmarking

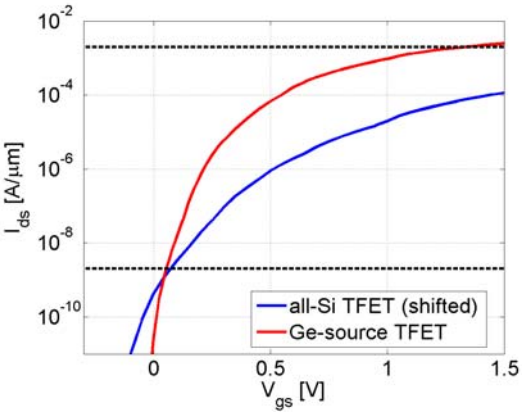
Short-gate and shifted-gate TFET device concepts (IMEC)
It was shown with the help of simulation that the position of the gate can impact the TFET device performance. The advantage of the short-gate TFET are the reduced ambipolar behavior, enhanced switching speed and relaxed processing requirements.[43] When the gate is shifted towards the source-channel a modest increase in on-current can be achieved.



The figure shows a schematic representation of the short-gate(left) and shifted-gate (right) concepts.

[41] A. Vandooren *et al.*, Proc. Silicon Nanoelectron*ic Workshop*, pp. 21-22, Kyoto, June 2009.
[42] D. Leonelli *et al.*, submitted to Electron Device Letters
[43] A.S. Verhulst *et al.*, Appl. Phys. Lett. **91**, 53102 (2007).

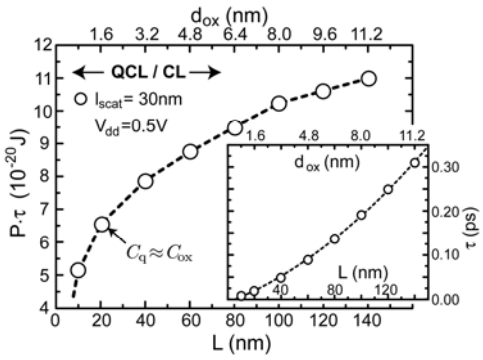
***Heterojunction-source TFET* (IMEC)** It was shown that the on-current of the TFET device can be increased considerably by placing a foreign source material on top of the Si nanowire channel. Germanium and InGaAs were identified as the source materials of choice for an n-type and p-type TFET device, respectively. The advantage of remaining the Si channel is obvious as conventional Si processing can be used for the gate-stack fabrication. For this work new models needed developed commercial device simulators failed to correctly predict the performance of heterostructure TFETs. [44], [45]. Together, the Ge-source for n-type and InGaAs source for p-type, enable a complementary silicon-based TFET suitable for competitive low-power applications. These heterostructure TFET configurations (Ge-Si, InA-Si and $In_{0.6}Ga_{0.4}As$-Si) and their corresponding *I-V* characteristics have been used as input for the circuit simulations by NXP.



The figure shows the comparison of $I_{ds} - V_{gs}$ characteristics of all-Si TFET (short gate) and the proposed heterostructure Ge-source Si-TFET, indicating the boost of the current with nearly 2 orders of magnitude to the same level as Si MOSFETs (dashed curve)s

Nanowire MOSFETs in the quantum capacitance limit

Quantum capacitance limit for conventional FETs (IBM). Scaling of NW transistors was investigated by modeling. The important implication of the analysis is that NW with very small diameter enable ultimately scaled transistor devices in a wrap-gate architecture since electrostatic integrity is preserved down to smallest dimensions. However, besides this pure geometrical argument the present study shows that NWs offer an additional scaling benefit. In the case of 1D transport, devices can be scaled towards the Quantum Capacitance Limit (QCL) which shows a clear scaling advantage in terms of the power delay product, i.e. the energy needed for switching the transistors. As a result, NWs exhibiting 1D transport are a premier choice as channel material for high performance, ultimately scaled FET devices.[46]

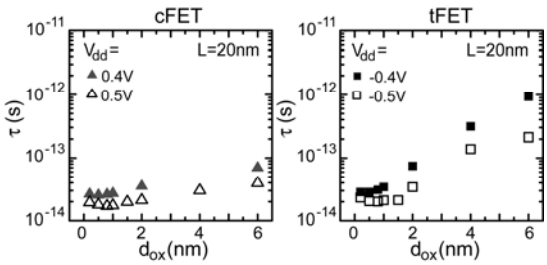


The figure shows the power delay product and gate delay (inset) versus gate length and oxide thickness for conventional FETs as the transition from classical limit to the quantum capacitance limit is made.

[44] A.S. Verhulst *et al.*, J. Appl. Phys. **104**, 64514 (2008).
[45] A.S. Verhulst *et al.*, Electron Dev. Lett. **29**, 1398 (2008).
[46] J. Appenzeller *et al.*, IEEE Trans. Electron. Dev. Vol. 55, pp. 2827-2845, (2008).

Tunnel FETs in the quantum capacitance limit

Nanowire tunnel FETs versus nanowire MOSFETs (IBM). Modeling of nanowire MOSFETs and tunnel FETs using non-equilibrium Greens functions was used to calculate gate delays as a function of scaling oxide thickness. It was demonstrated that when FETs are scaled to the quantum capacitance limit the tunnel FETs exhibit the same on-state performance as MOSFETs using the gate delay as the performance metric. The on-current is an order of magnitude lower for the TFETs though.



The figure shows gate delay versus oxide thickness for nanowire MOSFETs and tunnel FETs.

Work-package 6: Innovation related activities and training

Symposia and summerschool During the course of the NODE project, several conferences and workshops have been organized and funded, either partly or totally, by the NODE project.

- In connection with the NODE kick-off meeting a nanowire symposium was organized in Lund, 2005.10.06 with 250 participants. Invited and contributed oral presentations as well as poster presentations were given.
- An international nanowire symposium with 110 participants was organized in Eindhoven by Philips Research, 2006.09.19.
- The "Nanowire Growth Workshop", which is an international workshop on epitaxy and modeling of nanowire growth, has been organized and co-funded two times during the course of NODE, 2007.06.10 and 2008.09.15. The workshop had 50 and 70 participants, respectively. Invited and contributed oral presentations as well as poster presentations were given.
- The international conference on one dimensional nanostructures, ICON, was held in Malmö 2007.09.26-29. The conference had 170 participants from all over the world. Several top scientists were invited to present their results.
- In the summer of 2008 a summerschool on nanowires was organized in Cortona, Italy, and hosted by SNS Pisa, with 63 participants. The summerschool took place between July 1–5, 2008 and lectures were given primarily by scientists within the NODE consortium. The school was mainly targeted to PhD students within NODE, but also open to external participants. The lectures covered all aspects of nanowires relevant for the NODE project.
- The "NODE Device Workshop on Steep Slope Devices and Architectures", June 10-11, 2009, was organized and hosted by IBM Zurich Research Laboratory with 50 participants.
- As a conclusion of the project NODE supported the "NODE workshop on Nanowire Electronics" that was held in Lund, September 23-24, 2009. The workshop had around 65 participants. The workshop had sessions on wrap-gate transistors, ultra-low power devices, other nanowire applications, and integration issues. Each session started with an invited talk given by a person outside the NODE project and continued with contributed presentations given by NODE affiliated colleagues. The workshop ended with a panel discussion on systems applications.

NODE papers published in refereed journals

Publications 1–94 are already published, 95–96 are accepted for publication, and 97–103 are submitted to refereed journals.

1. "Structural properties of <111> B-oriented III–V nanowires" J. Johansson et al., Nature Materials 5, 574 (2006)
2. "On the formation of Si nanowires by molecular beam epitaxy" P. Werner et al., Int. J. Mat. Res. 97, 1008 (2006)
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5. "Nanowire-based one dimensional electronics" C. Thelander et al., MATERIALS TODAY 9, 28 (2006)
6. "Position-controlled interconnected InAs nanowire networks" Dick KA, Deppert K, Karlsson LS, et al. NANO LETTERS 6, 2842 (2006)
7. "Optimization of Au-assisted InAs nanowires grown by MOVPE" Dick KA, Deppert K, Samuelson L, et al. JOURNAL OF CRYSTAL GROWTH 297, 326 (2006)
8. "Phase segregation in AllnP shells on GaAs nanowires" Skold N, Wagner JB, Karlsson G, et al. NANO LETTERS 6, 2743 (2006)
9. "Nanowire-based multiple quantum dot memory" Nilsson HA, Thelander C, Froberg LE, et al. APPLIED PHYSICS LETTERS 89, 163101 (2006)
10. "Improved subthreshold slope in an InAs nanowire heterostructure field-effect transistor" Lind E, Persson AI, Samuelson L, et al. NANO LETTERS 6, 1842 (2006)
11. "Surface diffusion effects on growth of nanowires by chemical beam epitaxy"Persson AI, Fröberg LE, Jeppesen S, et al. JOURNAL OF APPLIED PHYSICS 101, 1 (2007)
12. "The morphology of axial and branched nanowire heterostructures" Dick KA, Kodambaka S, Reuter MC, et al. NANO LETTERS 7, 1817 (2007)
13. "Sulfur passivation for ohmic contact formation to InAs nanowires" Suyatin DB, Thelander C, Bjork MT, et al. NANOTECHNOLOGY 18, 105307 (2007)
14. "The structure of <111> B oriented GaP nanowires" Johansson J, Karlsson LS, Svensson CPT, et al. JOURNAL OF CRYSTAL GROWTH 298, 635 (2007)
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16. "Height-controlled nanowire branches on nanotrees using a polymer mask" Dick KA, Deppert K, Larsson MW, et al. NANOTECHNOLOGY 18, 035601 (2007)
17. "Directed growth of branched nanowire structures" Dick KA, Deppert K, Karlsson LS et al. MRS BULLETIN 32, 127 (2007)
18. "Electrospraying of colloidal nanoparticles for seeding of nanostructure growth" Böttger PHM, Bi ZX, D. Adolph D, et al. NANOTECHNOLOGY 18, 105304 (2007)
19. "Epitaxial Growth of III–V Nanowires on Group IV Substrates" Bakkers EPAM, Borgström MT, and Verheijen MA. MRS BULLETIN 32, 117 (2007)
20. "Remote p-Doping of InAs Nanowires" Li HY, Wunnicke O, Borgstrom MT, et al. NANO LETTERS 7, 1144 (2007)
21. "Single Quantum Dot Nanowire LEDs" Minot ED, Kelkensberg F, van Kouwen M, et al. NANO LETTERS 7, 367 (2007)
22. "Growth of Si whiskers by MBE: Mechanism and peculiarities" Zakharov N, Werner P, Sokolov L, et al. PHYSICA E 37, 148 (2007)
23. "Elastic strain relaxation in axial Si/Ge whisker heterostructures" Hanke M, Eisenschmidt C, Werner P, et al. PHYSICAL REVIEW B 75, 161303 (2007)
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34. "Time resolved microphotoluminescence studies of single InP nanowires grown by low pressure metal organic chemical vapor deposition" S. Reitzenstein, S. Münch, C. Hofmann, et al. Appl. Phys. Lett. 91, 091103 (2007)
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