SHORT E-S-i ‘“

SYNTHESIS REPORT

FOR PUBLICATION

SHORTEST

SHORT DURATION IN-SITU TESTS: ANEW APPROACH TO THE RELIABILITY EVALUATION OF ELECTRONIC ASSEMBLIES.

CONTRACT N : BRE 2-0270.

PROJECT N : BRITE lWRAM -5675.

PROJECT COORDINATOR : ALCATEL ESPACE (F).

PARTNERS :
IBM SEMEA (1)
IMO - LUC (B)
CEM (D)
SZE Microelectronics (D)

SUBCONTRACTORS : DESTIN NV(B)
SERMA TECHNOLOGIES (F)
UNIVERSITY DE BOURGOGNE (F)
IMEC (B).

STARTING DATE : 01/01/93. **DURATION :** 34 MONTHS.

PROJECT FUNDED BY THE EUROPEAN COMMUNITY UNDER THE BRITE/EURAM PRO(XL4MME.

DATE :1 December 1995

1. SUMMARY

Evaluation on a two days time scaIe of high reliability electronic assemblies by in-situ electrical and opto-i.mechanical test techniques.

KEYWORDS : ReliabMy - Evaluation - Short Duration - Tests - Standards.

SHORTEST “Short Duration in-situ tests : a new approach to the reliability evaluation of electronic assemblies” introduces, in an industrial environment, new, shorter and more effkctive reliability tests, based on the in-situ principle.

The traditional approach to reliability has been characterized by the determination of the cumulative failure curves. However, this approach is time consuming and there will not be enough test time nor test parts to resolve ftilure rates as low as 10 FIT. Using the ageing kinetics approac~ the reliability tests do not have to be continued until ftilure. It is sufficient to test until a difference in ageing behaviour can be detected to decide whether reliability is improved. A second advantage is, that in the ageing behaviour all information is present on how to improve reliability. Therefore, the detefina;ion of the ageing behaviour is ~he base for built-in reliability, The c&struction of the product can be improved for reliability, Statistical Process Control and Screening of incomes or final products can be installed in productio~ resulting in robust design and yield improvement.

The methodology of SHORTEST is to validate in-situ short test techniques for the evaluation of the basic ftilure mechanisms seen in electronic assemblies : solid state migratio~ electrochemical migration and corrosion and mechanical stress related phenomena. Both in-situ test and conventional tests are petiormed and a correlation analysis compares the results. The techniques which demonstrate good correlation have been the subject of a marketing study in Europe and recommendations are proposed for transfer in Quality Assurance and Process Design.

Five in-situ electrical amh’or optical test techniques have been developed in order to investigate the three basic failure mechanisms :

- In-situ resistance, leakage and impedance spectroscopy measurements : accurate determination of the ageing behaviour of an electrictd parameter (resolution less than 50 ppm) under wet and dry conditions.
- In-situ electrical and Mka-red thermal resistance measurements : continuous measurement of the thermal resistance degradation of devices under power cycling

All these test techniques have been evaluated against the three basic failure mechanisms on a huge variety of 10 subtechnologies (2500 test samples) used in high reliability products

The achievements so fw are the development and validation of seven in-situ test techniques . Five of the test techniques demonstrate capability of detecting failure mechanisms at 48 hours with moderate stress conditions and 50 % of the in-situ test results obtained at 48 hours on 10 subtechnologies correlate with conventional tests. The application of the method for Quality Assurance and BuiMhg-in reliability is foreseen.

The SHORTEST principles are under tildation within the consortium for the evaluation of active devices. An industrial version of the in-situ resistance test bench is now availabje and fi.uther industrial test bench developments are in progress. In parallel, a guidance based on the SHORTEST principles has been submitted to the CECC.

2. DESCRIPTION OF THE ACHIEVEMENTS

The primary objective of the BRITE EUR4M II program is to make the European manufacturing industries more competitive. SHORTEST “Short Duration in-situ tests : a new approach to the reliabWy evaluation of electronic assemblies” introduces, in an industrial environment, new, shorter and more effective reliability tests, based on the in-situ principle.

The traditional approach to reliability has been characterised by the determination of the cumulative ftilure curves. However, this approach becomes time consuming by the continuous improvement of the reliability, since there will not be enough test time nor test parts to resolve failure rates as low as 10 FIT ‘“. Using the ageing kinetics approac~ the reliability tests do not have to be continued until failure. It is sufficient to test until a difference in ageing behaviour can be detected to decide whether reliability is improved. A second advantage is that, in the ageing behaviour, all information is present on how to improve reliability. All relevant reliability materhd and design parameters are present in the reliability models to fit the ageing behaviour. Therefore, the determination of the ageing behaviour is the base for built-in reliability. With the knowledge of material and design parameters reievant for the reliability 1) the construction of the product can be improved for reliability , 2) Statistical Process Control and 3) Screening of incomes or final products can be installed in productio~ resulting in robust design and yield improvement. The investigation of the basic mechanisms, and their specific influence on the reliability, is of big importance.

METHODOLOGY

The methodology of SHORTEST was to validate in-situ short test techniques for the evaluation of the basic fhilure mechanisms seen in electronic assemblies : solid state migratio~ electrochemical migration and corrosion and mechanical stress related phenomem.
Five in-situ electrical and/or optical test techniques have been developed in order to investigate the three basic fhilure mechanisms:

- In-situ resistance, leakage and impedance spectroscopy measurements to address the solid state migration and corrosion.
- In-situ electrical and ifia-red thermal resistance measurements to address thermo mechanical degradation.

Both in-situ tests and conventional tests ᶻ have been performed and a correlation analysis compares the results. Three levels of correlation were investigated :

- correlation between in-situ and conventional tests results
- validation of in-situ results by physical failure analysis
- cross-correlation between two in-situ short test techniques on a given technology.

The techniques which demonstrate good correlation have been the subject of a marketing study in Europe and recommendations are proposed for transfer in QuaMy Assurance and Process Design. The final aim of the marketing study was to build an exploitation plan for SHORTEST in accordance with the European Industry needs.

TEST BENCH DESCRIPTION

The Ma-red thermography test bench is devoted to the thermo mechanical phenomena while electrical test techniques address the solid state migration and the electrochemical migration and comosion failure mechanisms. The electrical thermal resistance test bench allows the interesting investigation of a thermo mechanical behaviour by an electrical measurement.

A brief description of these five test benches is given hereafter. They have shown capabdity to detect ftilure medmnisms kinetics on 48 hours.

● **In-situ resistance (R) : Bets site LUC.**
Accurate determination of the ageing behaviour by measuring the changes of contact resistance under wet and dry conditions [3-]. The high temperature stabdity (below 10rn°C) allows a resolution of a few ppm.

.In-situ leakage (L) : Beta site IBM.
Leakage cuments of dielectrics or insulators between conductive lines are measured under combined temperature and humidity. Temperature is stabilized below 50m°C while humidity rate is monitored with less than 1°/0 of oscillation.

.In-situ impedance spectroscopy (Z): Beta site ALCATEL **ESPACE.**
Accurate measurement of complex impedance UP to lMHz allows to distinguish with frequency the ageing contribution of different parts" of a de&e (solder joint, ceramic m-aterial, met&diel&ic interface). The high temperature stabiIity is better than 70m"C from ambient to 150°C. That permits a resolution of less than 50 ppm on impedance.

.In-situ infra-red thermal resistance (IR-IWH) : Beta site CEM.
The thermal resistance degradation of device under power cycling is investigated by an ifia red determination of the temperature at the top of the die. The thermal resistance is evaluated within O, lKiW of resolution.

.In-situ thermal resistance (RTH): Beta site DESTIN.
The thermal resistance degradation of device under power cycling is investigated with high resolution and allows to follow a thermo mechanical degradation mechanism by an electrical measurement, Resolution is below O,OIK/W.

All these test techniques have been evaluated against the three basic failure mechanisms on a large variety of 10 subtechnologies used in high reliability products for power, computering and space telecommunications.

TEST PLAN

The ability of the test vehicles to reveal separate failure mechanisms is a key issue. Appropriate test vehicles were designed in order to keep the mixed fdure modes neg@ible. The test vehicles demonstrate elementary technologies for electronic assembly in a wide range of operation environments. In order to make the correlation analysis more efficient it was decided to produce so called ((Good }} and a Bad }) samples. Each test vehicle was manufactured in two production lots, one under controlled processes and one with a deliberate deviation in the process. 2500 samples were manufactured and 590 were tested with in-situ techniques. The remaining samples were tested with standard procedures (Military and ESA specifications) for correlation purpose.

The in-situ test matrix (Table 1) herebelow sums up all test techniques and the technologies investigated (590 samples tested).

In-Situ test	Beta Site	Solid State Migration	Electro chemical migration + corrosion	Thermo-mechanical stress
R	**Wc**	**AFG**	FGD	
L	IBM LUC		A D	
z	ALCATSL	G &		
IR-RTH	CEM			K
RTH	DESTIN			J-K

Technologies investigated :

A : Gold wires bonding on Aluminium pad.
C : C4 joints (Flip chip) on ceramic substrate.
D : Soldering between copper clip on ceramic substrate.
F : Conductive giueing of Ag wires on Al thin films.
G : Soldering with InPb on Au thin films.
G': Soldering with MPb of chip component on Au thin films.
H : Soldering with Sn62 of chip component on PCBS.
I : Soldering of DIL Flat Pack on PCB'S.
J : IMS Power module.
K : DCB Power module with Cu layers or Ag/Pd thick film.
L : Thick film multilayer dielectrics.

Table I : in-situ test matrix.

DEMONSTIL4TI'VE RESULTS

All these test techniques demonstrate capability of detecting ftilure mechanisms at 48 hours with moderate stress conditions.
Figures 1 to 4 illustrate the abiIity of in-situ electrical thermal resistance measurements to discriminate {t good>) and a bad >> samples.
Indeed a power module with copper layers (Fig. 1) shows a predictable drifi during ageing (Fig.2) whereas power module with AgPd layers (Fig.3) presents an exponential behaviour (Fig.4). The measurements of totally different kinetics allow to vflidate the Quality of different layer natures in power module assemblies.

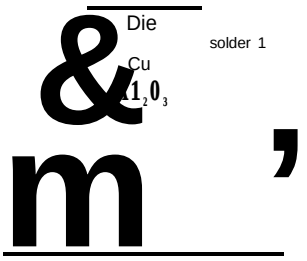

Fig. 1: Power module with C% layers (technology Kl).

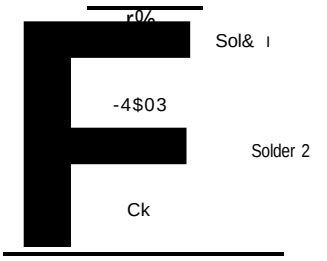

Fig. 3: Power module with Agl?d layers (technology K2),

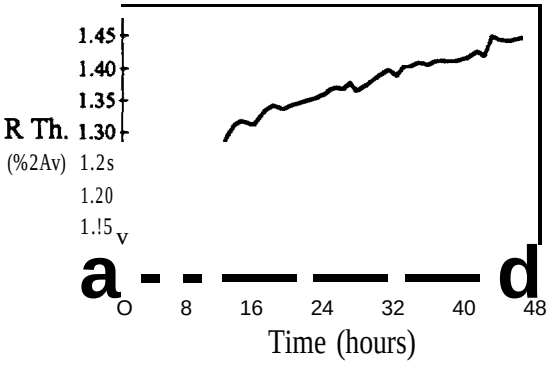

Fig. 2: RTH measurements on technology K1.

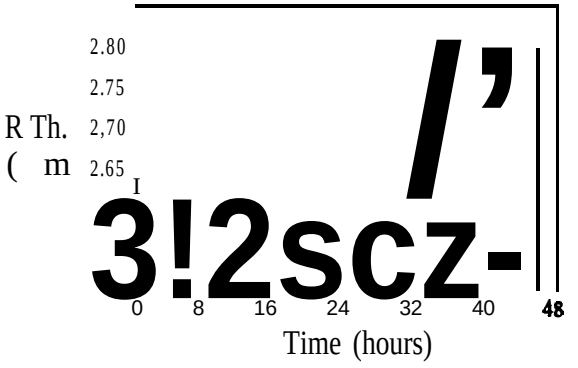

Fig. 4: RTH measurements on technology K2.

In-situ results are correlated to standard tests (thermal shocks and thermal cycles) and are validated by physical failure analysis.

Figures 5 to 7 show the good agreement between two in-situ test benches on a same technology. The sample is a dielectric material in-between two metal electrodes (Fig. 5) on akmina substrate (technology L).
Five compositions of dielectric have been evaluated by impedance and leakage measurements. Both techniques allow the ranking of the five compositions at low temperature for in-situ **Z (Fig.6)** and at high temperature for in-situ L (Fig.7). The low temperature range is representative of the operational conditions 4-whereas the high temperature regime is related to the manufacturing process.
Moreover in-situ rankings comelate with standard test classification which is

D1 -D3 cc D6 CCD2 - D5.

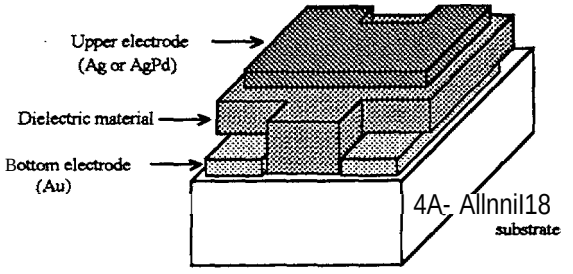

Fig. 5: Overview of technology L sample.

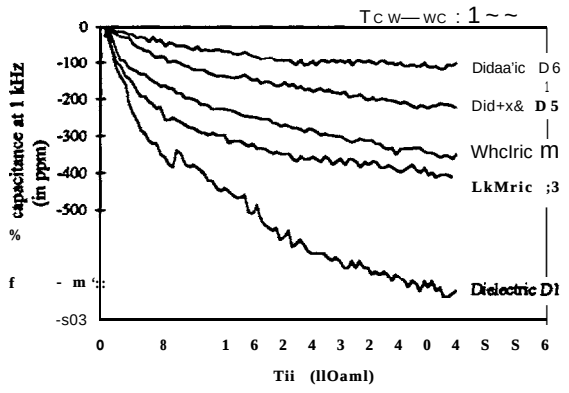

Fig. 6: lmpedancs measurements on technology L.

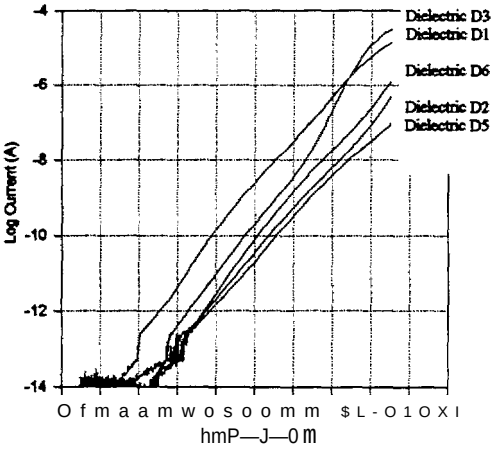

Fig. 7: Leakage measurements on technology L.

CORRELATION

The chart herebelow (Table 2) summarizes the status of the correlation analysis per technology.

In-Situ test	Technologies investigated	Correlation with standard tests	Correlation with faihme analysis
R	Al	No correlation	Correlation
	D2	No correlation	No correlation
	F	No **correlation**	**No correlation**
	Feedbsck ~	N.A.	N.A
	FC	Correlation	**Correlation**
	G	**No correlation**	**Correlation**
L	**A2**	**No correlation**	N.A.
	D1	Correlation	Correlation
	L	Correlation	Correlation
z	G'	No correlation	Correlation
	H	I Correlation	I Correlation
	L	No correlation	~ Correlation
RTH	J and K	Correlation	**Correlation**
IR-RTH	Jand K	Correlation	**N.A.**

Table 2: Correlation table,

Half of the in-situ results obtained at 48 hours correlate with conventional tests. When correlation is regarded with respect to the failure modes, two thirds of the results are correlated.
Interesting cross correlations have also been established :
- between L and **Z** in-situ techniques on Thick film multilayer dielectrics.
- between electrical and opticaI RTH on Power modules.

EXPLOITATION OF THE RESULTS

The final goal of SHORTEST is to introduce the developed in-situ test techniques in industry. At this stage of the program the feasibility is demonstrated but the ability to comply with the industrial specifications is not proven. The test benches are not yet optimized in terms of test capacities and cost objectives. The actual needs of the indust~ are gathered through a marketing study which started at the end of the second year of the project. A questionnaire was prepared and 10 targeted European companies were dkectly interviewed to validate the questiomaire which was then sent to 400 individuals in industries or laboratories in Europe. The answers are expected mid july 95 and will be the subject of a Qualhy Function Deployment Analysis. An exploitation plan shall be issued out of this analysis before end 95.

The net result of the interviews today is a lot of interest in the principles, a large demand of complementary tests and the application to the design and the selection of technology processes and the statistical control of processes. The application to the qualikation is not straightforward, mainly due to normative and contractual reasons.

In addition to the marketing and in response to the normative problem the consortium is preparing recommendations for a CECC specification which would integrate the SHORTEST principles.

A design guide will also be produced to more specifically describe the fields of application of the developed test benches,

CONCLUSION

Demonstrative results and correlation are strong enough to proceed from now on to industrial applications.

SHORTEST test benches are presently developed and in an industrialization phase.

The most promising applications are the choice of technologies, the screening test, the evaluation of processes and the incoming acceptance test.

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3. SCOPE OF APPLICATION OF THE RESULTS

The results of SHORTEST can be used and exploited to evaluate and quali& new technologies on a very short time scale and improve the test methodologies and standards.

3.1. Position of the consortium

IMO-LUC, as a member of the CECC reliability working group, will manage the transfer of the SHORTEST results to the CECC system. A draft guide was submitted October 1995 to CECC.
SERMA TECHNOLOGIES could play a role in the marketing.
IMO-LUC , DESTJN, Universit6 de Bourgogne and CEM may develop test methods and/or propose expertise and test sewices for the evaluation of new technologies.
DESTIN is the manufacturer and supplier of the electrical test equipments.
IBM and ALCATEL ESPACE will use SHORTEST techniques to develop new products for their customers and improve their test procedures and facilities.

3. 2A. Future ap~lkations for SHORTEST

The marketing study has revealed various potential applications for the desigq evaluatio~ qualification or control of processes, products or systems :

PROCESSES
MICRO-INTERCONNECTING
PCBS UNPOPULATED 'AND POPULATED WITH SMT
SMT REPORT
NEW REPORT TECHNOLOGIES
FLEX TECHNOLOGY
BONDING

ELEMENTARY PRODUCTS
MCM
MCM SUBSTRATES (L, C, D) UNPOPULATED AND POPULATED
POSSIBLE CRACKING AND DELAMINATION IN MCM-D
CORROSION OF MCM-D IN 80 / 80 ATMOSPHERE WITH +/- 15 V BIAS
HIGH TEMPERATURE DEGRADATION (OVER 200 C) OF MCM-D
POWER MODULES
CHARACTERIZATION OF CAPACITOR AND PIEZO-CERAMIC COMPONENTS
SMT CAPACITOR
CONDUCTIVE GLUE
ANISOTROPIC CONDUCTIVE ADHESIVE
THICK FILM MATERIALS UNDER HIGH DC-VOLTAGE AND THERMAL STRESS
THICK FILM CHARACTERIZATION FOR HYBRIDS
CONTACT RESISTANCE / CONNECTION UNDER HIGH DC-VOLTAGE AND THERMAL STRESS
SOLDER JOINT
INSULATION MATERIALS UNDER HIGH DC-VOLTAGE AND THERMAL STRESS
INSULATION MATERIALS FOR PLASTIC PACKAGES
BGA
COB
SIC
PACKAGE
TAB
MATERIALS FOR PCBS
CHARACTERIZATION OF SMART CARDS
NEW LEAD FREE SOLDER PASTE COMPOSITIONS

SYSTEMS
SENSOR PRODUCTION
MEDICAL
TEMPERATURE PROBE

4. EXPECTED ACTIONS AFTER PROJECT END

ALCATEL ESPACE	has planned the industrialization of in-situ SHORTEST DC Liile Test and Electrical RTH on active devices.
	AIXATEL considers the possibility to join the "Technology validation project " of IMO-LUC as a supplier of demonstrators for high density interconnects.
IBM	Considers the possibility to participate to the Technology Validation Project. Co-funding EC.
	Interconnections under humidity ardor thermal cycling for process development.
CEM	Intends to improve IR-RTH for design power modules for IGBT and MOSFET (5V, 500A). and proposes measurement methods for mechanical stress.
SERMA	Too early to define an exploitation plan but keeps in contact with DESTIN for the marketing.
IMO / LUC	Proposes a "Technology Validation" project on interconnects. Develops a technique for Electro migration on chip. Would like to propose a standard within CECC.
DESTIN	is producing and supplying a SHORTEST bench for electromigration. Has submitted a SEA proposal in ESPRIT about electomigration on chip. Will develop the DC life test and the Electrical- RTH for Alcatel active devices with IMO-LUC contribution.

5. THE CONSORTIUM

5.1. Consortium Description

Name of Organisation	Type	Role	Country	Nr Employees	Nr Researchers
ALCATEL ESPACE	I	Pc	F	**1300**	**200**
IBM SEMEA	1	P	I	**2500**	**150**
SZE deleted					
Limburg University Center @MO LUC) and IMEC	u	P	B	**250**	200
CEM	**N u**	P	D	**19**	**11**
DESTIN N.V.	**I**	Sc	B	**2**	**2**
Universit6 Bourgogne	u	se	F	**30**	**25**
Serma Technologies	I	Sc	F	70 (TBc)	

The short duration project is meant for transferring new, shorter and more effective reliability tests in an industrial environment.

The starting point is the concept of in-situ test method patented by IMO-LUC.
All partners have installed a test bench at their site and have performed short in-situ and standard test, including ftilure analyses, on test vehicles produced by IMEC, IBM SZE microelectronics and Alcatel,

Transferability to desig~ qualification and manufacturing of products is undertaken by two major industrial companies in computer with IBM and in space Telecommunications with ALCATEL Espace.

IMO-LUC, DESTIN, Univ. de Bourgogne and CEM have developed the test techniques.

Serma Technologies has performed the marketing study.

5.2. Names and addresses of the Dartners organisations

PARTNERS	TASK LEADER	KEY PEOPLE	TEL.	FAX	ADDRESS
IBM (P)	P. SILIPRANDI	F. BAIO	(39) 396005829	(39) 396005015	J'ia '~cco 61- 2Q0[59] VIMERCATE - ITALY
IMO / LUC (P)	L. DE SCHEPPER	W. DE CEUNINCK	(32) 11268826	(32) 11268899	Wetenschapsparlq Universitaire Campus B-3590 DIEPENBECK BELGIQUE
CEM (P)	T. AHRENS	M, KRUMM	(49) 432193780	(49) 4321937878	llsti [5]: 'Ostfach 1368 D-2350 NEUMUNSTER ALLEMAGNE
DESTIN (SC)	L. TIELEMANS		(32)11268811	'[32) 11268899	Wetenschapspark 1 B- 3590 DIEPENBECK BELGIQUE
SERMA TECHNOLOGIES (Se)	D. TRIAS	JP. BESSAGUET	(33) 56478015	(33) 56479728	Pare Cadera Nerd - Bat B3 Avenue du Pdt JF. KENNEDY 33700 BORDEAUX - FRANCE
IMEc (Se)	See lMO/LUC				
ALCATEL ESPACE (PC) Project Coordinator	G. GREGOIUS		(33) 61195656	(33)61 195211	26, avenue JF. Champollion BP 1187 31037 TOULOUSE CEDEX
Task leader	F, BOUTON	D MATHELIN	(33)61 195571 (33) 61195487	(33) 61195211	
UNIVERSITY de BOURGOGNE (SC)	M. MAGLIONE	C. DEKEUKELEIRE	(33) 80395945 (33) 61196166	(33)61 195211	
EC- BIUTE EURAM Contract Officer MTA Thematic research Grouping	H. FRIMA J. VIEIRA Da SILVA		(32) 22964970 (33) 145610502	(32) 22958046 (33) 145632258	European community 200, rue de la Loi, DG XII / C2 -3 B1049 BRUSSELS - BELGIQUE M~ke@ Technoh$es Avanc~es 36 av FOCHE, 75008 PARIS-F

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