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Functional and Reliable CAD for Power Circuit Design

PROJECT COORDINATOR : Siemens AG [referred to as "Siemens")

PARTNERS :

Universität der Bundeswehr (Associate Partner of Siemens referred to as "Bundeswehr")
Philips Research Laboratories (referred to as *'Philips RL")
Nederlandse Philips Bedrijven BV (referred to as "Philips CIT")
ANACAD Electrical Engineering Software (referred to as "ANACAD")
University College of Swansea (referred to as "Swansea")

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1 Summary

1.1 Keywords

CAD; Power electronics; Physics-based (compact) models; Circuit simulation; Power semiconductor devices

1.2 Abstract

Power electronic sub-systems are an essential part of a multitude of industrial processes and products. However, despite their importance, they are still designed through **a series** of prototyping cycles, even though CAD techniques have been shown to be effective in reducing the time-to-market as well as the overall design cost for the other electronic products. This difference in design methodologies arises because the device models on which the CAD approach is based, do not reproduce the behaviour of the power components correctly. The extension of CAD techniques to the design of power electronic circuits is essential if these processes and products are to be realised more rapidly and with greater reliability.

it is the goal of this project to extend the existing benefits of CAD to the design of power electronic circuits and to provide, as a new feature, the possibility of reliability simulation and optimisation. The first of these objectives has been achieved by the development of computer models (so called compact models) for the most important power device types:

- power diode
- power bipolar and MOS transistor
- IGBT (Insulated Gate Bipolar Transistor
- thyristor and GTO (Gate Turn Off thyristor)

The models are based on a physical description of all effects relevant to the device operation. A series of compact models of different levels of complexity have been developed for each device:

- Level 1, a pure electrical model incorporating an accurate treatment of conductivity modulation and associated charge storage effects
- Level 2, an electro-thermal model representing the device and its package by a thermal network of heat capacitances and thermal leaks, The temperature dependence of the model parameters determine in combination with the thermal equivalent circuit the influence of the temperature on the device characteristics.
- Level 4, an electro-thermal model including a Safe Operating Area (SAO) defined by measurement
- Level 5, an electro-thermal model with a physics-based SOA

An empirical approximation of the ambipolar diffusion equation was chosen as the common basis for the time-dependent description of the charge stored in the lightly doped parts of the bipolar devices. For the MOS-controlled parts (MOSFET and IGBT) a surface MOS-structu re and a drift zone were chosen as the common basis for the model development.

For all the power devices given above models of Levels 1, 2 and 4 could be established based on the common approach of modelling. The availability of the compact models is a very important step towards the first goal, but for its achievement two further tasks have to be fulfilled: (a) a parameter extraction methodology is required and (b) each model must be validated comprehensively.

a) A parameter extraction scheme could be determined for each device type. A modular concept could be achieved following the common approach of model development.

b) A number of practically important power circuits have been identified and six simplified benchmark circuits covering the functional parts of model validation have been extracted. These

circuits have been designed and set up. All model versions have been **comprehensively** tested making use of the benchmark circuits.

The physics-based models developed in this project correctly reproduce the electrical and thermal behaviour of power devices under all operational conditions. The usage of these model allows a faster design of power electronic circuits at reduced costs,

The second goal consists in the establishment of Level 5 models for the diode, the bipolar transistor and the MOSFET. To determine the reliability limiting effects of these devices a field feedback structure has been established. From the field data the dominant failure mechanisms have been extracted and simplified descriptions of these effects have been implemented in the corresponding models.

2 The Consortium

2.1 Names and addresses of the partner organisations

Project Coordinator:

Siemens AG, Corporate Research& Development, Otto-Hahn-Ring 6, D-81 739 Munich, Germany

Partners:

ANACAD Electrical Engineering Software, 11A, Chemin de la Dhuy, 38240 Meylan, France
Nederlandse Philips Bedrijven BV, Centre for Manufacturing Technology, Development Support, PO Box218/SAQ-1102, 5600 MD Eindhoven, The" Netherlands
Philips Research Laboratories, Cross Oak Lane, Redhill, Surrey, RH1 5HA, United Kingdom
Universität der Bundeswehr, Institut für Elektronik, WE 4, Werner-Heisenberg-Weg 39, D-85579 Neubiberg, Germany, (Associate partner of Siemens)
University of Wales, Department of Electrical and Electronic Engineering, Wales, Swansea SA2 8PP, United Kingdom

Project reference number:

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2.2 Consortium Description

The consortium is made up of two industrial concerns (Philips and Siemens), a software house (ANACAD) and two universities, The profile of the consortium is given in Table 1.

Table 1: Consortium profile

Company	Type	country	Role	No. Employees	No. Researchers
Siemens A.G.	I	D	C	373,000	42,000
Philips Electronics, UK	I	UK	PR	12,000	250
Philips Electronics N.V.	I	NL	PR	230,000	3000
ANACAD	I	F	PR	6.2	32
Univ. Bundeswehr	U	D	AP	950	120 (in dept.)
Univ. Swansea	U	UK	PR	400	40 (in dept.)

(C: coordinator; PR: partner; AP: associate partner)

Before providing a short introduction of each partner and its role in this project, it has to be stressed at this point that all partners have actively participated in the development of a common approach the models are based on.

2.2.1 Siemens A.G.

Measured by sales and number of employees, Siemens is one of the world's largest electrotechnical companies. It has manufacturing and sales organisations in about 130 countries and generates more than half of its sales from business outside of *Germany.*

[n the field of power semiconductor devices, Siemens, together with Eupec (a company owned by Siemens), is a major manufacturer. The product range *covers* the whole spectrum of power device types as well as the whole range of power handling capabilities (from low to high power), Moreover, Siemens is a major user of power devices and a major supplier of power electronic

systems world-wide. About one quarter of Siemens' total sales (44.5BECU in 1995) are related to power electronic circuits and systems,

Siemens regards progress in the application of CAD techniques to power electronic circuit design as very important to improve the competitiveness of its power components and sub-systems in the marketplace therefore working hard to achieve the objectives of this project. During the project Siemens entered the market with low level models for its power MOSFET product range in order to enhance the value of their customers, 'The successful application of these models created a demand for models of the smart power modules TEMPFET and PROFET containing a MOSFET as switch,

The main roles of Siemens in this project have been:

- project coordination
- MOSFET, IGBT and GTO/thyrsitor model development and parameter extraction methodologies
- extraction, definition and set-up of benchmark circuits
- model validation

2.2=2 **Philips**

Philips Electronics is Europe's leading manufacturer of lighting and consumer electronic products as well as semiconductor devices. These three sectors contribute 13%, 45% and 15% of the turnover, with the remainder being largely professional products and systems. Philips generates more than 40% of it's turnover outside Europe, with over half of this in North America.

Power conditioning sub-systems of the type targeted in this project are used in a wide range of low-energy lighting products, and also for televisions, video cassette recorders, personal computers etc. and driver stages for audio systems, motor drives, covering the low to medium power range and largely targeted at consumer and automotive applications. Products include all the device types this project is dealing with.

Like Siemens, Philips is keen to establish a mare rigorous approach to the design of power circuits and sub-systems through the use of CAD, The project is important to future business plans in three ways. Firstly, now that CAD for circuit design has become available for the company's device product range to ensure long-term business with customers both within and outside the company. Secondly, the company has stated a target of halving the time taken to introduce new products over the next few years in order to improve its competitive edge, especially in comparison to major Japanese companies. CAD is seen as essential to achieve this aim. Final{y, the company seeks to improve product reliability to improve profitability and customer satisfaction. The power sub-systems are a major source of failures in the current product range and it is intended that the failure aspects of the compact models proposed here should be applied to optimising reliability using CAD,

The main roles of Philips RL in this project have been:

- diode, BJT and MOSFET model development and parameter extraction methodologies
- failure in models

The main roles of Philips CFT in this project have been:

- failure in models
- extraction, definition and set-up of benchmark circuits
- model validation

2.2.3 ANACAD

ANACAD covers a range of products based on its simulation tool, ELDO. Capabilities include mixed signal, analogue behavioral and timing simulations as well as a range of post-processing and control systems. Analogue behavioral simulation is an essential requirement for the models developed in this project as this capability allows designers to model not just electrical networks but other physical systems, of which thermal networks are of particular relevance, The same approach can then be used to model complete sub-systems, even if they include motors, relays, tamps, etc.

The widespread demand of analogue behavioral simulation capabilities prompted ANA(2AD to devote a significant effort to the development of this capability. ANACAD's only competitor in this field in ANALOGY, based in the U.S.A. However, it is not easy to retain competitiveness in this market as it is currently the centre of attention of many companies. ANA(2AD relies on projects such as this one, together with strategic partnerships with both device manufacturers and CAE main stream **vendors, to retain its current technological lead,**

The main role of ANACAD this project has been:

- model implementation in circuit simulator

2.2.4 Bundeswehr

The Institute of Electronics is part of the Faculty of Electrical Engineering of the Federal Armed Forces (Bundeswehr) University, München. Its present major interest is the development of power device models and parameter extraction techniques for the purposes of circuit simulation. It currently collaborates closely with industry in this field of research.

The main role of Bundeswehr in this project has been:

- diode, BJT, IGBT and GTO/thyristor model development and parameter extraction methodologies

2.2.5 University of Wales, Swansea

The University of Wales, Swansea provides facilities and opportunities for advanced teaching and research in all academic subjects. Within the University, the Department of Electronic Engineering furthers this aim in the context of its own subject area and forges, where relevant, links with other research organisations and industries both within Europe and elsewhere. The department's role can be illustrated by its interaction with a range of European and North American industry, including British Gas, British Steel, ABB, British Telecom, ST and Bell Northern, Canada. A specific example is its participation in a "Link project, funded by the U.K. Department of Trade, modelling the operation of IGBT. This project is in collaboration with a number of U.K. industrial and academic establishments.

The main roles of Swansea in this project have been:

- device simulation support for model development
- model validation

3 Technical Achievements

3.1 Introdcution

It is the aim of this project to develop physics-based {so-called compact) models for the most important power devices which can be used for circuit simulations. The second goal is to enhance these models so they are able to predict device failure.

This task consists of three steps: the development of models of different levels of complexity, the establishment of extraction methodologies for all parameters and the comprehensive model validation. Before the beginning of the model development a common modelling strategy for all devices has to be acquired and **agreed** on by ail partners.

In the following sections these four steps are discussed.

3.2 Common Modelling Approach

The development of the power device models is based on the device physics, The device behaviour is derived from the effects which occur inside the device. These derivations are not always possible in an exact way, empirical descriptions based on experience must also be used, but the modelling is kept close to the physical causes of the different effects. The resulting model equations and the parameters used are therefore related to physical and technological quantities. The models contain information how the device behaviour depends on the technology. The influence of parameter variations can be investigated and a "worst **case" analysis is** possible.

3.2.1 Common Elements of Device Structure

Power devices have common elements of their structure and of the physics of operation for which common descriptions can be used. The structure of power devices can be subdivided into the following basic regions:

- a thick low-doped semiconductor layer which is necessary to obtain the required blocking voltage of a power device
- high-doped end regions
- junctions between regions of different doping (pn-junctions or junctions between high and low doping)

For these regions different descriptions are applied.

In all power devices except the MOSFET {under normal operation) the low-doped layer is swamped by a plasma of electrons and holes when the device is in its on-state. This layer can be filled completely or only by part (e.g. BJT) by the charge carriers which are injected from the neighboring regions. The charge stored must be extracted when the device is switched off. The injection, storage and extraction of the charge carriers mainly determines the static and dynamic characteristics of power devices. It leads to a modulation of the conductivity, to turn-off delays, and to significant energy losses during switching,

In conventional semiconductor device models (e.g. in SPICE} quasi-static descriptions are used for the charge carriers; this means that the charge distribution is always a function of the instantaneous voltages. This method is completely insufficient for power devices, a real dynamic description is required instead. The development of a charge model has therefore been one of the main tasks of the project.

For the high doped end regions a quasi-static description is suitable; it yields the current component of the minority carriers which are injected into these regions.

The equations of the pn-junctions give the widths of the space charge regions at the junctions and the charge carrier densities at the borders of the space charge regions as a function of the junction voltages. These values are then the boundary conditions for the adjacent regions. Depending on the manufacturing process the junctions can be approximately abrupt or graded with a distinct doping profile.

Devices with art isolated gate (MOSFET, IGBT) have several voltage dependent capacitances according to their structure. Models of these capacitances covering all regions of operation have been developed, For the current in the transistor channel the standard equations are used.

3.2.2 **Modelling of the Plasma**

The time dependent charge carrier distribution is described by the diffusion equation which is a partial differential equation of second order. An analytical solution of it can be found in some special cases but in the general case only numerical solutions or approximations are possible.

After analysing different methods an approach has been chosen which uses an empirical description. From theoretical considerations and from numerical device simulations it is known, how the charge distributions change when the devices are switched on or off. The charge variations are approximated by relatively simple functions. Inserting these functions into the diffusion equation yields an ordinary differential equation which can easily be solved.

The results of this approach agree well with results of one-dimensional numerical solutions, furthermore the equations obtained are similar to a part of the exact analytical solutions of the special cases solvable.

From the charge carrier distributions the equations of the total charge and the current are derived. The resulting equations are very compact and therefore well suited for the implementations in computer programs for circuit simulations. Short calculation times can also be obtained.

3.2.3 **Temperature Effects**

The influence of temperature on the device characteristics is given by the temperature dependence of the model parameters. Three physical parameters are dominating: mobility and lifetime of the charge carriers and the intrinsic carrier concentration. The dynamic temperature behaviour caused by the self-heating due to power losses is calculated with the help of an equivalent network consisting of thermal capacitors and thermal resistors. The capacitors and resistors are the elements for heat storage and heat flow, respectively. They represent the device body, package and heat sink.

3.3 **Model Description**

Compact Models have been developed for the power diode, power bipolar and power MOS transistor, IGBT and GTO/thyristor. The models have several levels of complexity. On the lowest level (Level 1) only the electrical characteristics of the devices are described. On the second level {Level 2) the thermal characteristics and also the electro-thermal interactions are included. The models use a thermal network of heat capacitances and thermal leaks to represent the device and its package. The circuit simulator can therefore calculate the actual device temperature which depends on the dissipated energy. The temperature in turn, affects the electrical characteristics of the device. The temperature distribution inside the device is not considered; an uniform temperature is used instead. The next model level (Level 4) includes a Safe Operating Area (SOA) which is defined by measurements. The program of the models checks whether critical values of device operation are reached or exceeded. If this happens a message is given to the user. Critical values are e.g. maximum current and voltage, maximum or minimum temperature.

The second task, the inclusion of the reliability limiting effects in some of the compact models, resulted in a further model level (Level 5) with a physics-based SOA. Level 5 models have been developed for three devices, power diode, bipolar transistor and MOSFET. It comprises of three steps:

(a) The establishment of a statistical data base. The data for this task can not be obtained in the laboratory, but the data sources are field data. A field feedback structure has been established for this purpose.

(b) The identification of the most relevant failure mechanisms. For the bipolar transistor and the MOSFET the most important reliability limiting mechanisms have been extracted on the base of several hundred thousand devices in the field.

(c) For both devices, models for the failure modes have been developed and implemented into the compact models . For the diode there have been problems in obtaining the field data. The alternative approach, using the reliability model of the BJT has been pursued.

3.3.1 **Power Diode**

The diode model considers the following effects which cause a contribution to the diode current:

- recombination of stored charge carriers and charge variations in the low-doped middle region
- injection of charge carriers into the high-doped end regions
  variation of the depletion region at the pn-junction (depletion capacitance]
- leakage current at reverse bias, avalanche breakdown.

The first item has the most significant influence on the diode characteristics, especially on its switching behaviour. The dynamic charge description of the common modelling approach is used to take into account the time-dependent charge distribution which determines the relation between current and voltage; it is especially important for the reverse recovery of the diode at turn-off .

The transient characteristics are also influenced by the kind of junction (abrupt or graded) between the low- and high-doped regions.

A further major effect is the resistivity modulation of the low-doped region. Its gradual variation during turn-on causes the forward recovery of the diode (Fig. 1 in sec. 3.5). Charge distribution and mobility degradation at high charge carrier densities are considered for the calculation of the resistance.

3.3.2 Power **Bipolar Transistor (BJT)**

The power bipolar transistor differs from standard bipolar transistors by a thick low-doped region in the collector layer. Because of this structure the transistor exhibits three regimes of operation in its on-state: active region, quasi-saturation and full saturation, These different states are determined by the charge carriers (plasma) in the collector; the switching between the states and especially the charge extraction at turn-off is described with help of the dynamic plasma model of the common modelling approach. Further effects considered by the model are the dependence of the current gain on voltage and on current, the base-emitter zener breakdown and the influence of graded junctions.

3.3.3 Power MOSFET

The model of the power MOSFET uses the standard equations for the current in the transistor channel. The typical features of a power transistor resulting from its structure are included:

- voltage-dependent capacitances
- resistance modulation of drain drift region
- inverse body diode,

The capacitance between gate and drain has the most important influence since it causes a feedback between the output and input terminals (Miller capacitance). An electrostatic approach which includes lateral effects is used to describe its large variations with voltage. Since the MOSFET is an unipolar device the resistance of the low-doped drain region is not modulated by a significant change of the charge carrier density, however, the resistance varies due to variations of the effective area and a degradation of the charge carrier mobility at high electric field.

3.3.4 IGBT (Insulated Gate Bipolar Transistor)

The IGBT consists essentially of a MOSFET and a bipolar transistor with a thick low-doped base layer. The MOSFET current acting as base current of the bipolar transistor and the voltage-dependent capacitances of the MOSFET structure are described according to the model approach for the power MOSFET. Using the plasma model the base charge and the total IGBT current are obtained,

The IGBT model is suitable for the different IGBT types which are called NPT- (Non-Punch-Through) IGBT and PT-(Punch-Through) IGBT.

3.3.5 Thyristor, GTO (Gate-Turn-Off Thyristor)

Thyristors have a four-layer structure with two low-doped regions. By calculating the current components at the borders of the layers and considering the interaction of the different components the thyristor characteristics are obtained. The current feedback depends strongly on the level of charge carrier injection; this leads to the two states of operation in forward bias, blocking state and conduction mode. A dynamic description of the charge carriers in the low-doped regions is applied, which is essential to obtain the correct dynamic behaviour. The turn-off is determined by charge storage effects; the thyristor exhibits a reverse recovery similar to the power diode, typical turn-off characteristics of the GTO are the negative gate current, the avalanche breakdown of the gate-cathode junction and the tail current after storage time.

3.4 Parameter Extraction

It is clear from the sections reported above that the “compact models” require a considerable number of parameters to produce numerical results within a CAD simulation. It is equally clear that the collection of accurate parameter sets is one of the most Important on going activities required to maintain the validity of the ‘[compact model” suite.

In order to make the problem as manageable as possible with such a wide range of devices a common strategy was developed which brings together, **in a physical way, the various groups of** parameters. In addition the parameter schemes were chosen so that each parameter was as independent of the other measurements as possible. A deliberate attempt was made to base parameter extraction schemes on electrical data which was familiar to the design engineer. Much of this data is available from the manufacturer in data sheet form, The ability to relate the models to such data is an important method of instilling confidence in the user that the models are accurate. A second important point is that the parameter schemes are set in an hierarchical form. As each parameter is measured its value is fixed and used in the next stages of fitting. Thus as far as

possible the simultaneous optimisation of a number of parameters is avoided. Optimisation may give slightly better results for a particular measurement but leads to difficulties in an overall scheme. The number of parameters is kept to the minimum required. Little advantage is gained from long sets of parameters for which many are given default values. For all the devices the parameters can be divided up into sets:

a) Physical parameters which describe the basic constructional and material properties contributing to the" behaviour of the device.

   These usually describe the properties of the thick voltage supporting i-region built into all power devices, and the diffused regions forming contacts and injection controlling regions. They are in effect the physical Parameters familiar to device designers. For example these include doping levels and approximate profiles, areas of contact regions. In principle such data can be obtained electrically by capacitance / voltage, breakdown and physical examination. As far as possible data is taken from manufacturers information.

b) Those which deal with the steady state on/off conditions relating to currents and voltages.

   In the case of the bipolar devices in the on-state the bipolar plasma built up in the device from the combined effects of injection and recombination giving rise to the forward I/V characteristic. Parameters are required which describe both the injection and recombination effects. These can be derived from detailed examinations of I/V characteristics and simple switching measurements.

   For the MOS device a simple description of the transfer characteristic is sufficient to deal with the on-state.

   In the reverse state the requirement is to describe the leakage associated with recombination centres this is usually done by a fixed current.

c) Those which are associated with the transient behaviour of the device in the switching cycle.
   In the bipolar devices transient measurements are required over a wide range of conditions to get the value of second order parameters describing the plasma removal. Instrumentally this is one of the most difficult areas to characterise because of" rapid transients, and dependence on drive schemes in three terminal devices. For the CAD user these transients must be accurately described as the start up and turn-off conditions of power devices are the most important characteristics of power circuits.

   For the MOS devices transients are dominated by capacitance effects between the metal/polysilicon contacts, thin oxides and depleted semiconductor regions, Within the regimes of operation of MOS-devices in power circuits values derived from simple capacitance data are sufficient.

These sets are sufficient for the basic description of the isothermal behaviour of the devices (Level 1 models), To include thermal effects '{self-heating) standard models are used for the thermal characteristics of the package, combined with thermal coefficients from the literature for the temperature effects on the basic physical parameters {Level 2 models). These would include standard variations in mobility, lifetime, intrinsic carrier density, transconductance, threshold voltage, as well as thermal resistance and capacitance of the device and mounting system. Many of these effects are included in the Level 2 models as standard formulations for the variation of physical parameters as a function of temperature.

Level 4 models require additional data from safe operating area plots to give warnings of expected failure, These are effectively boundary limits set from manufacturers data.

Table 2: Parameter sets for devices investigated (Level 1); classification given above

Device	Total no.	(a)	(b)	(c)	Comment
Diode	12	4	6	3	3 further parameters for graded junctions
Bipolar Transistor	19	6	12	1	graded junctions already included
MOSFET	13	3	6	3	MOSFET part only without reverse diode
IGBT	17	4	8	6	3 further parameters for graded junctions
GTO	12	5	9	7	graded junctions add optional parameters
Thyristor	12	5	10	6	graded junctions add optional parameters

As device complexity rises two effects can be observed. In the first case the number of parameters rises. This is because of the extra number of component parts of the device. For example the IGBT requires a description of both the bipolar and MOS parts, In addition the device action becomes more controlled by internal feedback mechanisms, making it more difficult to derive information from the external three terminal measurements,

The details of deriving the parameters are specific for each device. In general standard electrical measurements under short pulse conditions to avoid heating are essential. One of the most difficult parameters to determine is the recombination lifetime τ in the i-region of the devices. This is a most important parameter as it is the feature deliberately controlled in device manufacture to tailor recovery behaviour. In devices containing accessible diodes diode recovery methods can be used. Temperature effects can be simulated by alteration of the ambient conditions. Though most of the parameters are derived from standard test conditions the test of the accuracy is in the examination of the devices/predictions in the benchmark circuits. As these are chosen to be close to realistic operational conditions they provide a severe test of the parameter set.

As more use is made of CAD it is to be expected that refinements to the parameters and the evaluation will occur; however, it is important that the maximum use be made of the existing schemes and to only introduce extra parameters on the basis of good electrical **evidence.**

3.5 Model Validation

The third and last, but very important step towards robust and reliable compact models is their stringent validation by comparing their predictions to the observed characteristics of benchmark circuits. These differ from the more idealised circuits used during the model development in the respect that the devices are driven using waveforms more representative of those typically encountered in power conditioning systems. For this purpose six benchmark circuits have been designed and set up.

The aim of the validation of the models is to prove the validity **and** usefulness of the models and to clearly document it in order to ensure the designer that these models are suitable to his design applications. To achieve this objective, two steps can be distinguished:

- numerical validation,
- physical validation.

3.5.1 Benchmark circuits

During the development of the models permanent testing of their features is of vital importance to know whether the objectives have been reached. These tests can also be used as guidelines for further development activities, The ultimate test is of course the model validation which proves

the usefulness of the model in typical design applications and shows whether all physical effects required have been included in the model. To carry out these tests effectively a set of well chosen benchmark circuits has been established.

The benchmark circuits should meet the following requirements:

- the circuit is representative for real applications, because it is important to validate the model in its context of use,
- the set of circuits allows the model developer to test all the required physical effects of the models,
- the circuit operates in a mode where the typical power device features are most prominent,
- the measurement equipment and the parasitic effects of the circuit are easy to represent in the simulation circuit,
- the circuit is as simple as possible to enable the model developer to pinpoint shortcomings of the model from discrepancies between simulation and measurement results.

So, to define the set of benchmark circuits a list of all required physical model properties has to be compiled. From this list six benchmark circuits have been extracted, designed and set up.

3S.2 **Numerical validation**

The numerical validation is intended as a help to bring about a model of which the parameters can easily be characterised, a simply maintainable implementation of the model in the simulator, and a robust behaviour of the model during simulation computations. This validation checks with respect to the appropriate model requirements the numerical aspects of the model description, the implementation in the circuit simulator, and the numerical behaviour of the model in the simulations.

The numerical validation takes the following points into account:

1. limitations of the model,
2. types of analysis in which the model can be used (DC, AC and transient),
3. application range of the equations and their parameters,
4. parameter extraction,
5. equation continuity,
6. convergence problems,
7. correctness of output messages for errors and warnings.

To validate these items simple test circuits can be used.

3.5.3 **Physical validation**

The physical validation addresses the question whether all relevant physical effects have been covered sufficiently and the usefulness of the model in the typical applications.

The physical validation comprises the following steps:

1. Check the basic device characteristics by comparing the simulated and measured characteristics,
2. Test all relevant physical model properties by choosing the appropriate benchmark circuits, comparing simulated results and measurement data, and checking whether the model behaviour meets the model requirements.

The results of the various tests of both validation steps are summarised in model validation forms in order to have an overview of the status of all models during their development.

3.5.4 Validation library

The validation library presents the final result of the model development activities carried out during the project. H contains sections of validation results of the models for diode, bipolar transistor, MOSFET, IGBT, GTO and thyristor. For each power device such a section provides an overview of the validated model versions, the particular test circuits and simulation circuits, and the comparison of measurement and simulation results, The description of the simulation circuits provides schematic diagrams, tables of component values used for the various test conditions and analysis data. In addition, input files of simulation circuits are available which allow the designer to easily repeat the simulation himself.

The following figures give an impression of the work performed in this task,

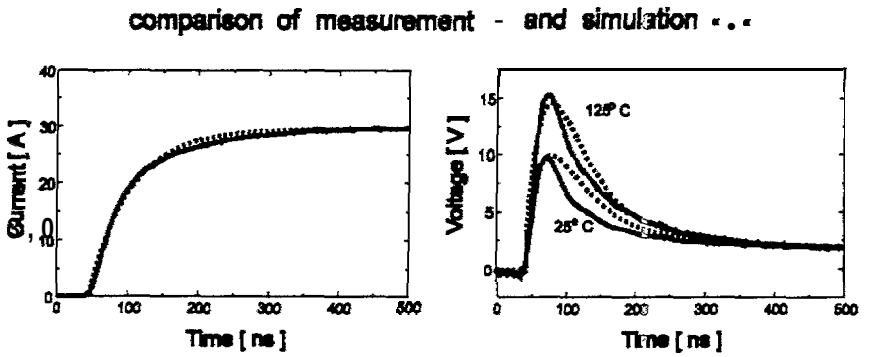


Fig. 1: Turn-on waveforms (forward recovery) of the power diode (BYP 103)

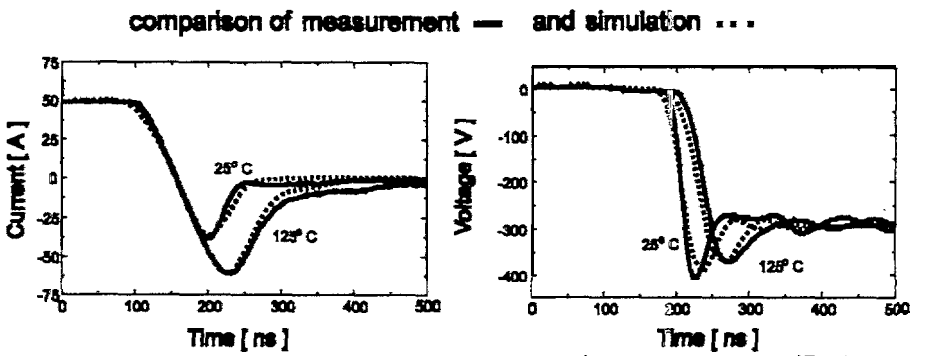


Fig. 2: Turn-off waveforms (reverse recovery) of the power diode (BYP 103)

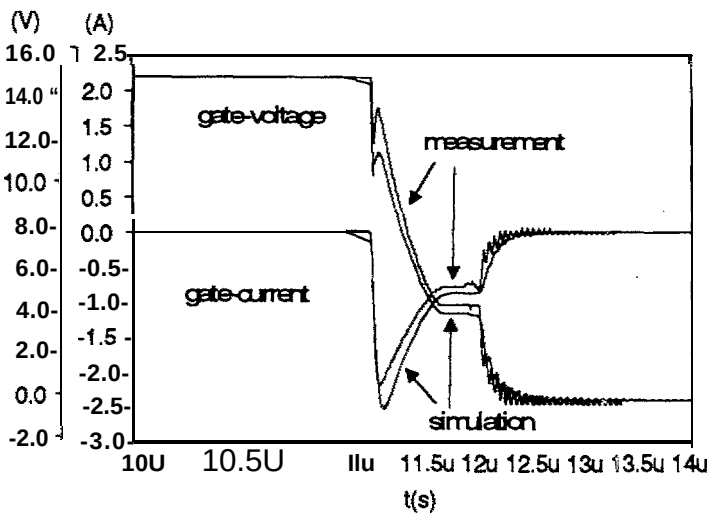


Fig. 3: Gate discharging at inductive load switching for the MOSFET BSM 181 F

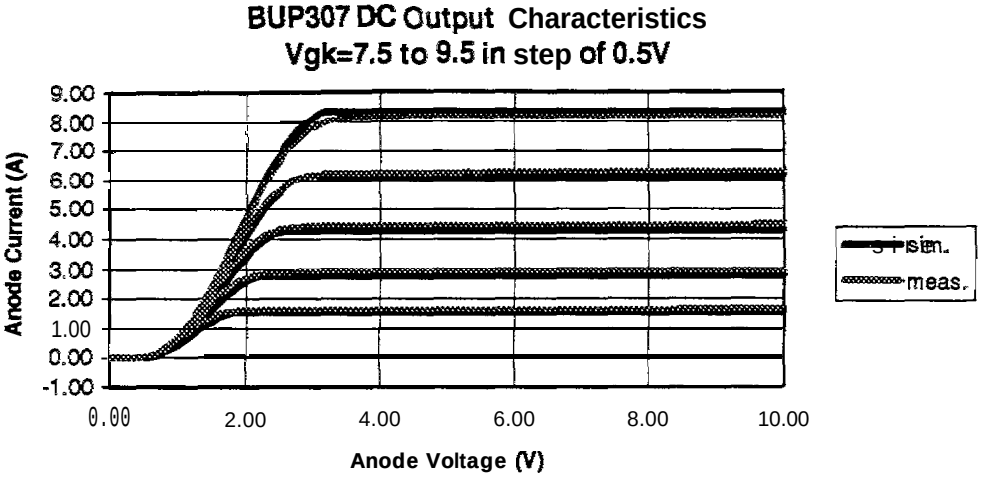
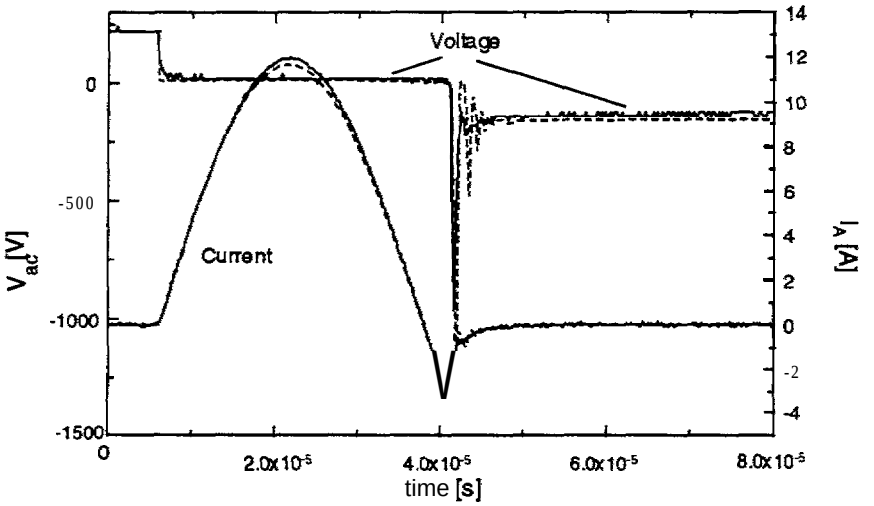


Fig. 4: DC output characteristics of the NPT IGBT BUP307



Fig, 5: Passive commutation of the thyristor BT151-500R at the nominal value of I_{TRMS}; f≈15.6kHz; measurement: -; simulation: ---

3.6 Summary

At the beginning of this project a through comparison of existing modelling methodologies has been earned out. An empirical approximation of the ambipolar diffusion equation was chosen as the common basis for the time-dependent description of the charge stored in the lightly doped parts of power devices. The common approach proved to be successful for the establishment of compact models for all power devices.

For all power devices Levels 1,2 and 4 models have been developed. Level 5 models including a simplified description of the dominant failure mechanisms have been created for the diode, bipolar transistor and MOSFET.

Parameter extraction schemes could be established for all parameters.

Six benchmark circuits as close as possible to important operational conditions of the different devices have been extracted, designed and set up. These circuits have been used for a comprehensive validation of all models developed. Except for the GTO, this process could be finalised as scheduled. All assessment activities together with the guidelines of using the models are collected in a validation library,

4 Exploitation plans and follow-up actions

4.1 ANACAD

Objectives in developing power circuit design tools for ANACAD is to increase the market penetration of simulation technology (ELDO) in specific application domains within the targeted market segments. ANACAD is focusing in three strategic areas: telecommunication, automotive and device manufacturers to increase added value to generic CAD technology (IC simulation) on both workstation and PC operating systems, The key benefit of delivering CAD power circuit design is to lower the acceptance barrier of GAD technology of end users.

The strategy for this project is based on the following directions:

1) Device manufacturers: Need a closer relationship with the semiconductor suppliers and also with the partners in this project as it is necessary to determine the parameter sets of the power devices.

2) Component users: It is necessary to establish a service relationship with these users in order to characterise their devices with respect to the different types of application,

In order to ensure this strategy, we have to work in a privileged relationship with the project partners for the characterisation of their models, test and validation of our product as well as to give them, and of course other European partners, the characterisation service we have as ANACAD using some Mentor Graphics facilities,

Finally, in this strategy we have no objections to work with third parties (different partners outside of the project). The only assumption for us is, that we take a period of at least 12 months exclusivity with the project results (up to June 97). We need to have this exclusivity over one year as a technology leader, then we can work in co-operation with any third party.

The primary objective of this exploitation plan, beside providing additional device modelling capabilities, is to proliferate ANACAD's simulation technology with an effective differentiation compared with our competition, This means in particular

- provide products of higher value to our customers
- increase product acceptance with embedded capabilities targeted
- address customer requirements in design reliability
- first time working silicon and application
- shrink ramp-up period for the process extraction phase and methodology development
- reinforce relationship with customers by developing products aligned with requirements in CAD for power circuit design
- pull through other ANACAD products from the complete product line (optimisation)
- drive ANACAD's development along the CAD technology curve to maintain competitiveness
- maintain market perception of technological leadership and development
- PC product line will exist around mid 1997

4.2 Philips

For Philips the main purpose of this project is to use the results to prevent especially the late design changes of those products where (development) throughput time and time to market are especially important. The basic strategy of Philips to exploit the result of this projects in the various sectors in the Philips organisation is to use the following steps:

- raise awareness by giving lectures and workshops
- organizing Philips internal symposia with major focus on the results of this project
- execute pilot projects together with potential partners using available project research results

form partnerships on implementation and further research,

Table 3 gives the status of the contacts per product group and the commitment per product group to use the results of this project.

Table 3: Status of contacts and project commitment

Product category	Status contacts	Recent / current project	Commitment
Monitors	Fixed partner in this project	Major carriers, especially in the deflection area	Co-operation focuses especially on the reliability analysis and improvement of deflection circuits
Televisions	Fixed partner in this project	Major carriers for this project	Will use results in entire product group for both SMPS and deflection provided that results are adequate
Lighting (electronic)	Regular contacts on progress, especially lighting research	Minor earners, especially in electronic ballast	Depending on results; could become a major user of project results; requires quite mature models
Shavers	Initial discussions were held	No projects yet	

4.3 Siemens

Siemens sees the application of the project results along the following directions:

a) "Added value" to power components
b) Clarify faults of power components in customer applications
c) CAD assisted power sub-system design in various application areas

The following table summarises the exploitation efforts of Siemens.

Table 4: Exploitation plan of Siemens

Group	Contacts	Status	Commitment
Semiconductors	Regular contacts on progress	Major carriers for this project	project
Drives and Standard Products	Fixed partner in this project	Major carriers for this project	project
Medical Engineering	Regular contacts on progress	Minor carriers, especially in special power converters	project
Power Transmission and Distribution	Regular information on progress	Minor carriers, especially in DC power transmission	negotiation
Transportation Systems	Regular information on progress	Minor carriers, especially in converters for electric trains	negotiation
Automotive Systems	Regular information on progress	Minor carriers, especially in motor ignition systems	negotiation

4.4 Universities

Bundeswehr and Swansea plan to exploit the results of the project in three main areas, namely, teaching, research and industrial training.

5 Collaboration sought

At the moment no partner seeks of an external collaboration.

ANACAD needs potentially external R&D resources from universities in order to update the different modelling techniques. However, at present no decisions have been made.

6 References

The following papers have been presented at the given conferences and published in the corresponding proceedings:

M. Bayer, R. Kraus, K. Hoffmann:
A new analytical GTO-model for circuit applications.
26th Annual IEEE Power Electronics Specialists Conference (PESC'95), vol. 2, pp. 879-885, Atlanta, Georgia, USA, June 18-22, 1995

T. Kern, R. Kraus, K, Hoffmann:
A precise analytical model for diffused power diodes.
6th European Conference on Power Electronics and Applications (EPE'95), vol. 1, pp. 1.146-1.150, Sevilla, Spain, September 19-21, 1995

R. Kraus, M. Reddig, K. Hoffmann:
The short-circuit behaviour of IGBTs based on different technologies.
6th European Conference on Power Electronics and Applications (EPE'95), vol. 1, pp. 1.157-1.161, Sevilla, Spain, September 19-21, 1995

J. Sigg, M. Bruckmann, P. Türkes:
The series *connection of IGBTs investigated by experiments and simulation.*
27th Annual IEEE Power Electronics Specialists Conference (PESC'96), vol.2 pp. 1760-1766, Baveno, Italy, June 23-27, 1996

P. Türkes, J. Sigg:
Electrothermal simulation of power electronic devices.
2nd Meeting of the European Community on Computational Methods and Applied Sciences (ECCOMAS), invited talk, Pans, France, September 9-13

From Siemens a German patent is pending concerning one of the circuits established for parameter extraction:

Registration date: July 27th 1995
Registration number: 19527538.1