HICAAP - Highly Integrateble Converters for Advanced AC Photovoltaics

A project of the European Non-Nuclear JOULE III Program

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Abstract

In May 1997 the European Commission started the project "Highly Integratable Converter for Advanced AC Photovoltaics" as a part of the Non-Nuclear JOULE III Program. The goal of this project was to develop a Module Integrated Converter (MIC) with extended lifetime (at least 15 years) and low production costs.

One crucial factor for miniaturisation is the integration of many functions into a single chip, usually an Application Specific Integrated Circuit (ASIC). The second factor is the increase of the switching frequency in order to reduce the size of passive components.

The consortium is composed of the research centres ISET (Germany), ECN (The Netherlands), IMEC (Belgium) and NMRC (Ireland) as well as the company Soltech seated in Leuven, Belgium.

ECN developed and simulated the control algorithm for the grid detection and the MPP-Tracking, while IMEC created the ASIC according to the specifications from ECN. Now all necessary software modules for further simulations are available at ECN.

The ASIC is fully functional and tested. An interested industrial partner can use this device in a future product development as is.

ISET developed a robust DC-AC inverter of 100W AC output power with standard magnetic components. The interested reader can find some useful hints for developing a DC-AC inverter. Some unexpected problems appeared during the project development so that at the current stage some more inquiry needs to be done on passive components in order to develop an industrial product.

NMRC developed flat integrated magnetic components for the use in the inverter developed at ISET. This includes the transformer as well as the filter chokes. The current sensor is integrated into the transformer, which is a very interesting feature. NMRC also built up a considerable knowledge in packaging issues, thermal properties of the inverter and reliability estimation.

In this document each partner gives a detailed description of his results achieved during the project.

Table of Content

Part A: Market Study, Power Electronic Design and Cost Analysis

1.1 Motivation

The increased use of renewable energy and rational use of conventional energy sources are fundamental pillars of a responsible energy policy for the future. Because of their sustainable character, renewable energy sources, almost exclusively based on solar irradiation, are capable of preserving resources, preventing the greenhouse effect due to CO_2 emission and providing energy services virtually without any environmental impact. Grid connected photovoltaic (PV) systems distinguish themselves in the method of energy transfer: there is no need for energy storage devices such as batteries.

Recent trends in grid connected photovoltaic systems show coexistence of different kinds of converter concepts. The combination of Module Integrated Converter (MIC) and solar module – often called "AC Solar Module" – allows a direct connection of the solar modules to the grid by converting the module DC voltage to 230V AC (Fig. 1). The MIC concept has some important advantages over string orientated or central inverter concepts such as:

- Increased energy yield in case of systems suffering from shading effects.
- Reduced danger of arcs due to replacement of the DC installation by an AC installation.
- Minimised safety problems, since no live conductors are accessible during installation
- Simplified configuration of PV systems due to standardised interface (230 V~).

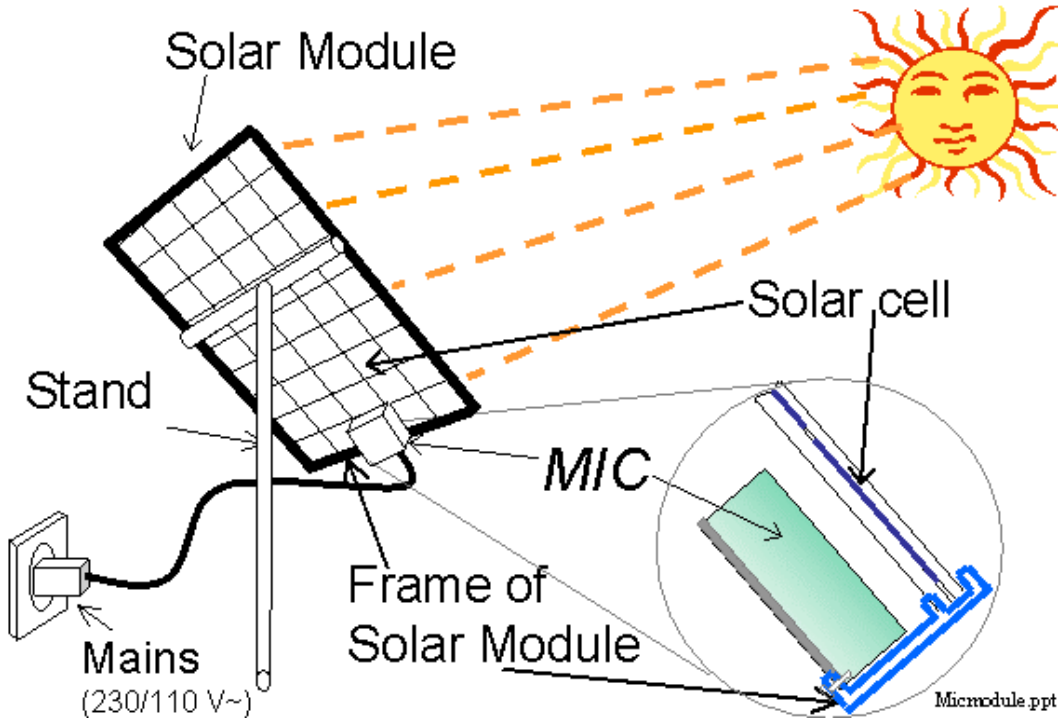

Fig. 1: Cross-section of a MIC mounted to the frame of a solar module.

Usually the rated power of the MIC is slightly lower than the rated power of the solar module. In the future a large number of solar modules will have an average power of 100W to 150W which corresponds to an area of solar cells of $1m^2$ to $1.5m^2$.

Nevertheless, the central inverter concept will remain popular especially in very large-scale PV systems. Depending on the PV system's site and properties of installation, string oriented systems are most likely to be used in the medium and high power range.

1.2 Market study

For the definition of the most important ratings of the module integrated inverter it is necessary to investigate the recent market of PV modules. Using a data bank system at ISET collecting data of almost all suppliers of PV modules and systems technology in the world one can find the data for the following overview about PV modules (Fig. 2).

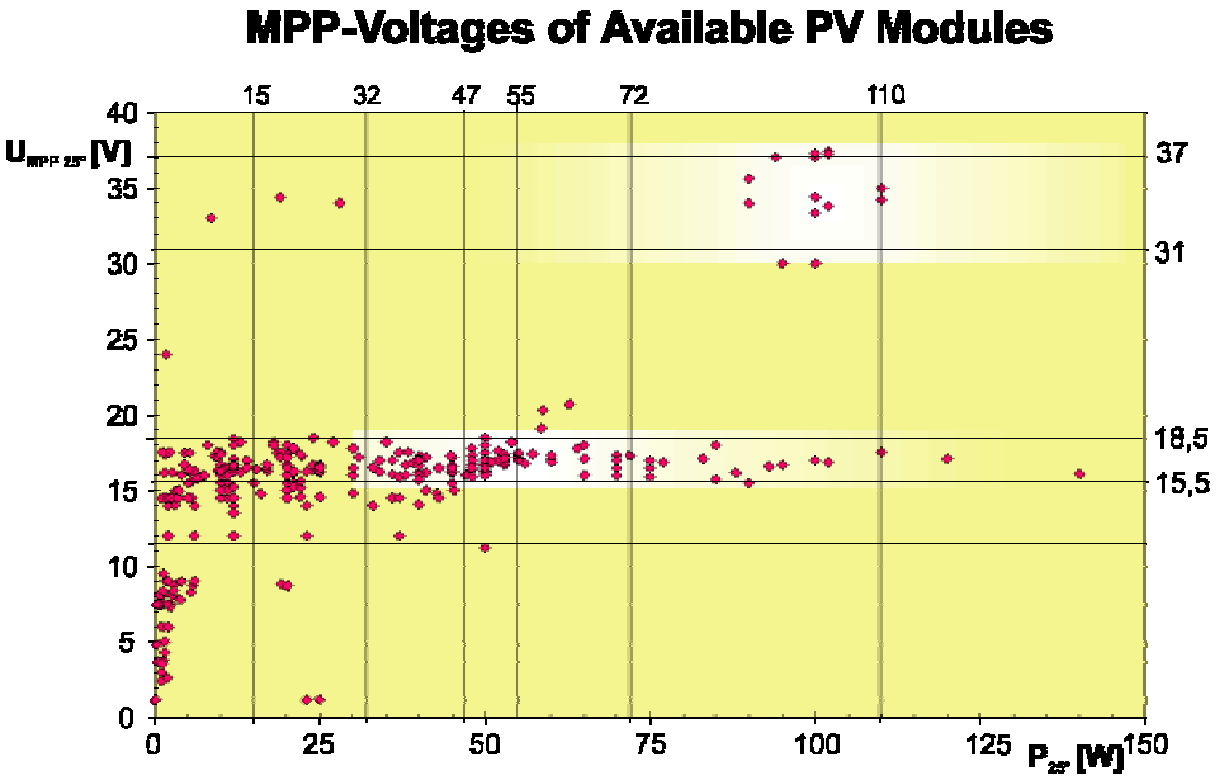

Fig. 2: MPP voltages and rated peak power of commercial available PV modules

Additionally, a lot of experts have been interviewed about their expectations concerning the PV market for the next 5...10 years.

Conclusions of the investigations are:

- maximum sizes of PV modules will be limited to 2...3m²,
- single cell area will be enlarged,
- average efficiency is expected to become 15%,
- a major part of the PV applications will be buffered by 12V or 24V batteries and so
- the input voltage of those inverters will be kept at 18...36V (MPP) and
- the most interesting power range of MIC's in the next 5...10 years will be from 100...300W.

The expectations concerning the number of pieces per year are necessary for market analysis, too. Some investigations concerning this issue are reported in [7][1]. Based on different scenario the PV market is expected to grow as shown in Fig. 3 and 4. The average annual increase of the PV market is about 20% for the last 10 years. In 1997 125MWp PV modules have been installed world wide (40% more than 1996). The market is expected to increase about 15...20% per year. So a market volume of about 380...540MWp could be expected in the year 2005. These figures seem to be realistic since for example only Japan aims on 2,5GWp in 2010.

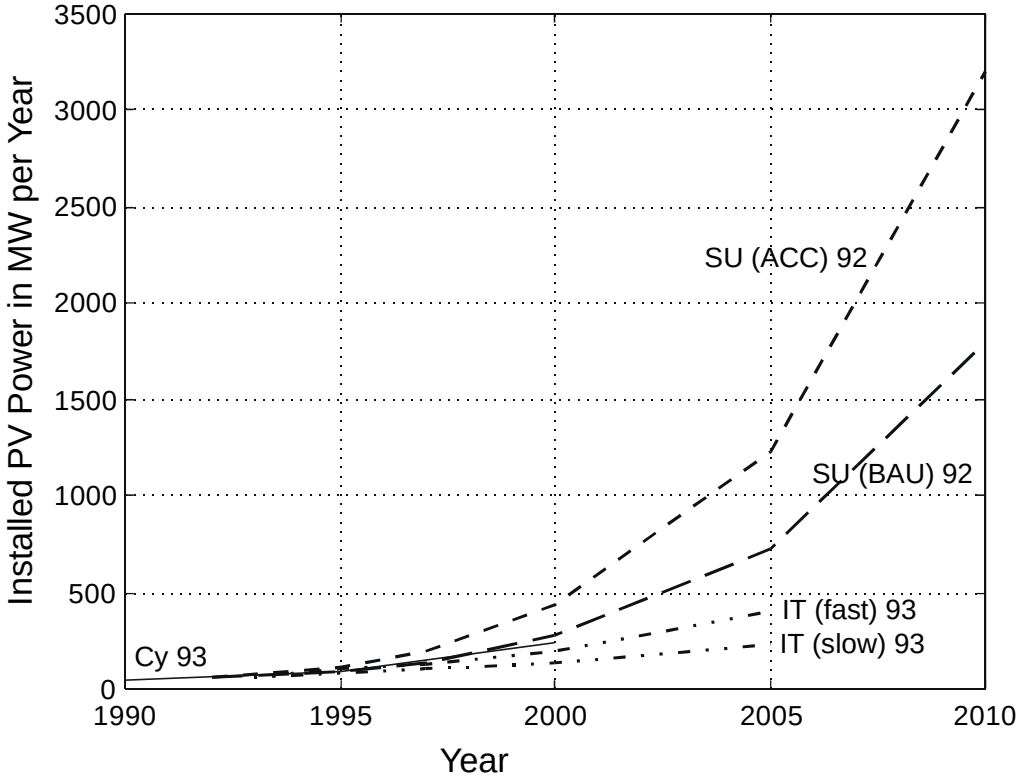

Fig. 3: World wide PV market increase expectations of various experts [1]

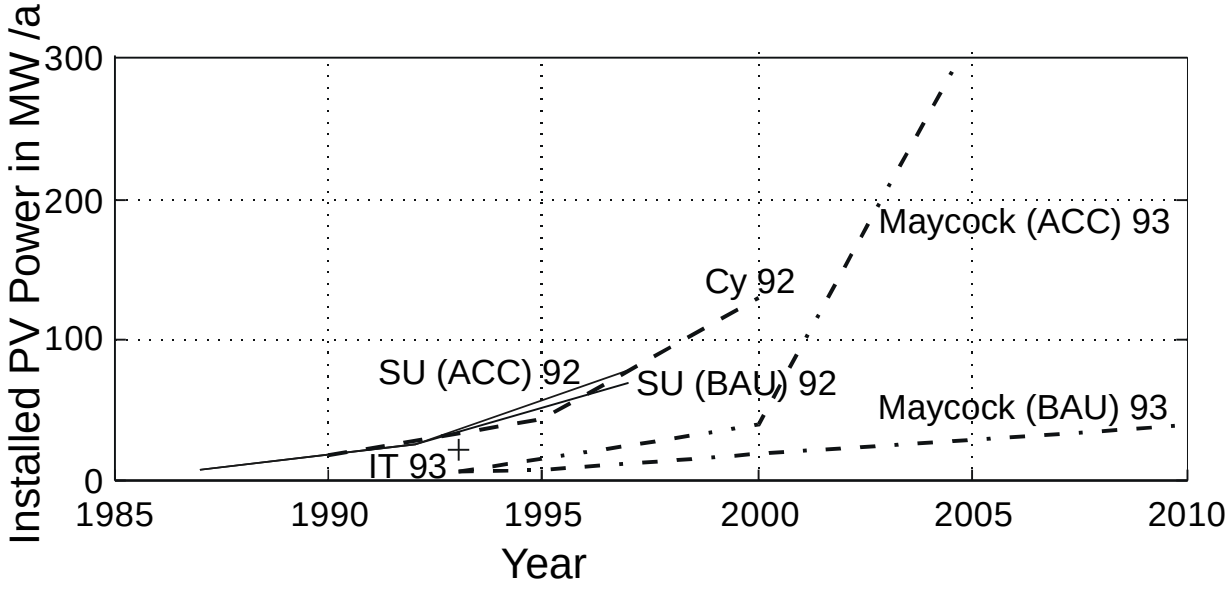

Fig. 4: PV market increase for not grid connected household application [1]

But not the whole PV market is identical to the market for module integrated inverters. MICs will be implemented in only a part of the grid connected systems. Based on national and international statistical data (reference [1]) the overall potential use of PV has been estimated. Starting with Germany, most of the applications will be grid connected systems as shown in Fig. 5. The majority of these systems will be smaller roof top integrated systems. But the energy supply situation in Germany is not directly comparable with many other countries. Practically all households are connected to the public grid in Germany.

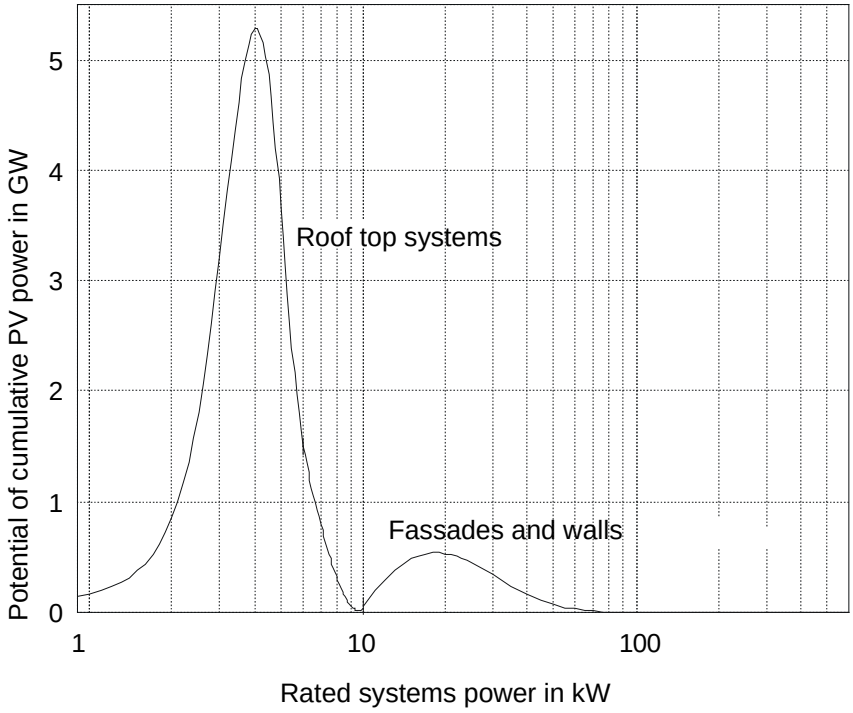

Fig. 5: PV use potential in grid connected systems in Germany

Investigating the recent use and the need for electrical energy in all countries the characteristic curve of potential PV use has another form (Fig. 6). Starting with several 10W up to some 100W Solar Home Systems represent an important part of rural electrification. Usually these PV systems consist of one or few PV modules, a battery charge controller and a battery. The loads are DC loads supplied by the battery. Only sometimes these small systems are equipped with a small additional inverter for AC generation. It makes no sense to implement MIC's in those systems. The amount of these kinds of systems are not a part of the potential market for AC modules.

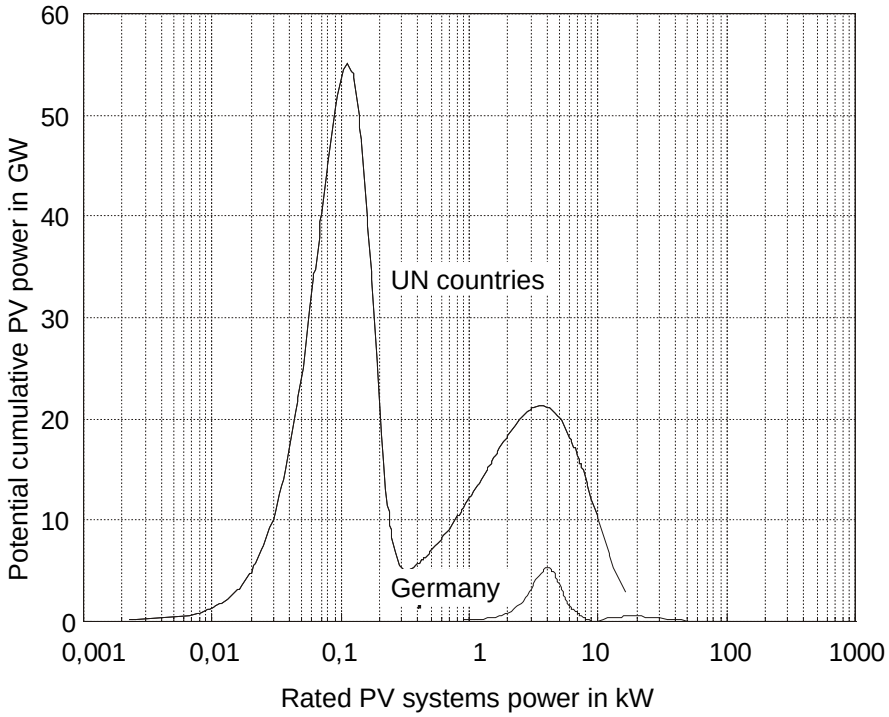

Fig. 6: Comparison of the PV use potential in UN countries and in Germany

In principal all systems with more than 1kWp rated power are a part of our market expectations. These systems will be grid connected systems or hybrid systems. In order to supply common loads, hybrid systems are buffered with batteries and equipped with inverters. In the last five years a new systems technology for hybrid systems has been developed. In this case all components are connected via the AC line. Thus the systems design becomes very simply. Expansion of the system can be achieved by adding one more energy supplier (for example one AC module) to the AC bus. So also PV application in hybrid systems are potentially a part of the AC module market.

In total this potential market has about 350...400 GWp world wide. Considering the recent market volume (see page 15) a market saturation is far away. If one third of PV production is supposed to be grid connected or similar application, in 2005 the potential market for AC modules would be 110..130MWp. Assuming that at this time two thirds of this market volume would be covered by string inverters in the kW range a more or less realistic market expectation could be 55...65MWp per year in 2005.

Considering the rated power of one MIC in a range of 100...300Wp this market volume corresponds to 160,000 to 500,000 pieces per year.

2.1 Inverter Topologies

36 different inverter topologies have been investigated with respect to their feasibility of adapting low power ranges at low input voltages to the grid [2]. They can be divided into five classes:

I. Inverter concept with DC-voltage link:

In order to fit the low PV-voltage level to the public grid level, common DC-DC converters are used. These converters are connected with a DC-voltage link to a high frequency switching converter.

II. Inverter concept with pulsed DC-Voltage-Link:

These concepts use the same inverters as I., however their control unit generates the absolute value of a 50Hz sine wave instead of a DC-voltage. This pulsed DC link voltage is inverted by a 50Hz switching inverter.

III. Inverter concept with AC-Voltage-Link:

DC-DC converters including a HF-transformer need a diode rectifier to get a DC output voltage, otherwise the output voltage is a bi-directional square wave voltage with a frequency of the switching frequency. An inverter concept with AC-Voltage-Link is able to feed this voltage form into the grid. Therefore the inverter needs voltage bi-directional switches.

IV. Direct inverter concept:

One of these concepts includes a common high frequency switched inverter connected to a 50Hz transformer. The other concept is a transformerless topology which includes two bi-directional Zeta or Cuk converters in parallel-series-connection.

V. Pulsed DC-Voltage Link using resonant converter:

This is the same inverter concept as discussed in II. However, instead of a common DC-DC converter series or parallel resonant converters are connected to the link

2.2 Steps of Calculation

All these topologies have been studied under the same conditions:

- Power range 165W
- same switches and switching frequency
- passive components: same core materials for inductance and transformer and same types of capacitors

In the first step the inverters have been compared with respect to the switch stress and the transformer size. Many topologies are not suitable because of the high switch stress and the size of the transformer, especially all converters of the category III due to their bi-directional switches.

Nine different inverter concepts have been chosen for the next step: all concepts of class IV and V, concepts with full-bridge and Cuk-converters of class I and II and concepts with boost-converters of class I. The second step the calculations focussed

on the efficiency, volume and costs of each topology. Although the concept with 50Hz transformer presented a good efficiency, the concept dropped out due to the high volume determined by the 50Hz transformer. The dramatic difference in volume can be seen in fig. 7.

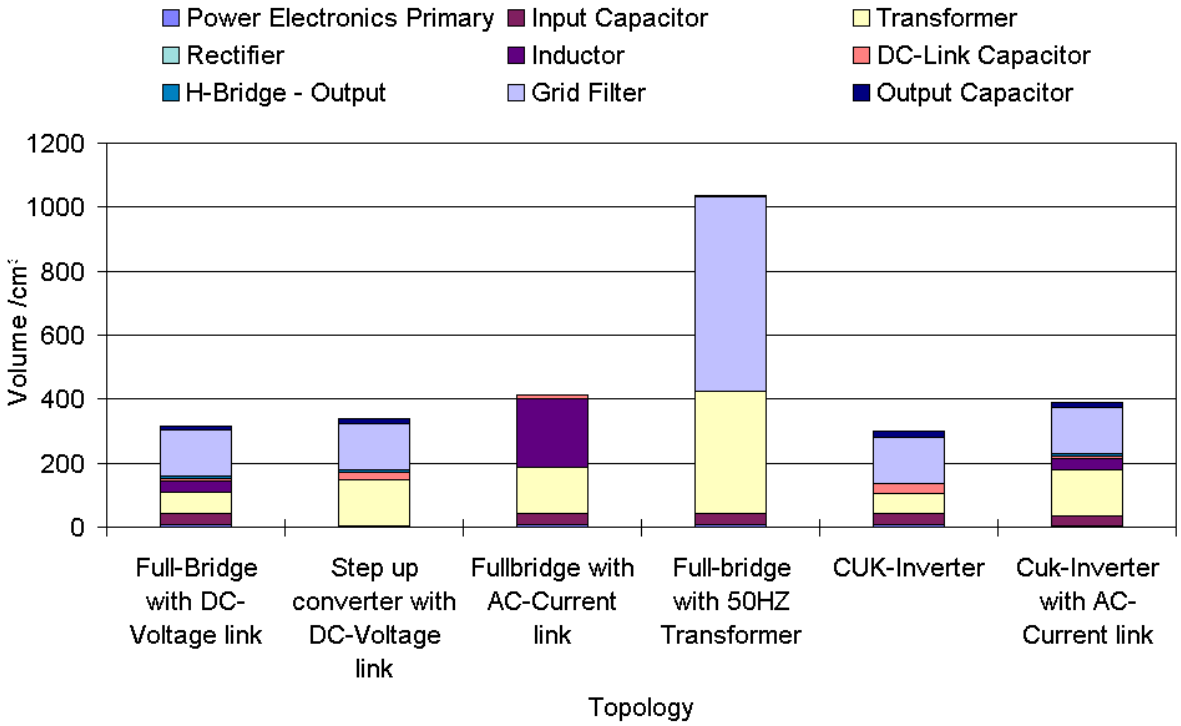

Fig. 7: Comparison of the different topology with respect to the volume

All transformerless concepts are disregarded as well. The resonant concept which of course do not have a high efficiency at 20kHz are still considered for the next step, since now the switching frequency is increased to 100kHz. Since the inverters do not differ significantly in their volume and costs, the inverters are compared with respect to the achievable efficiency. An estimation for achievable efficiencies can be seen in fig. 8:

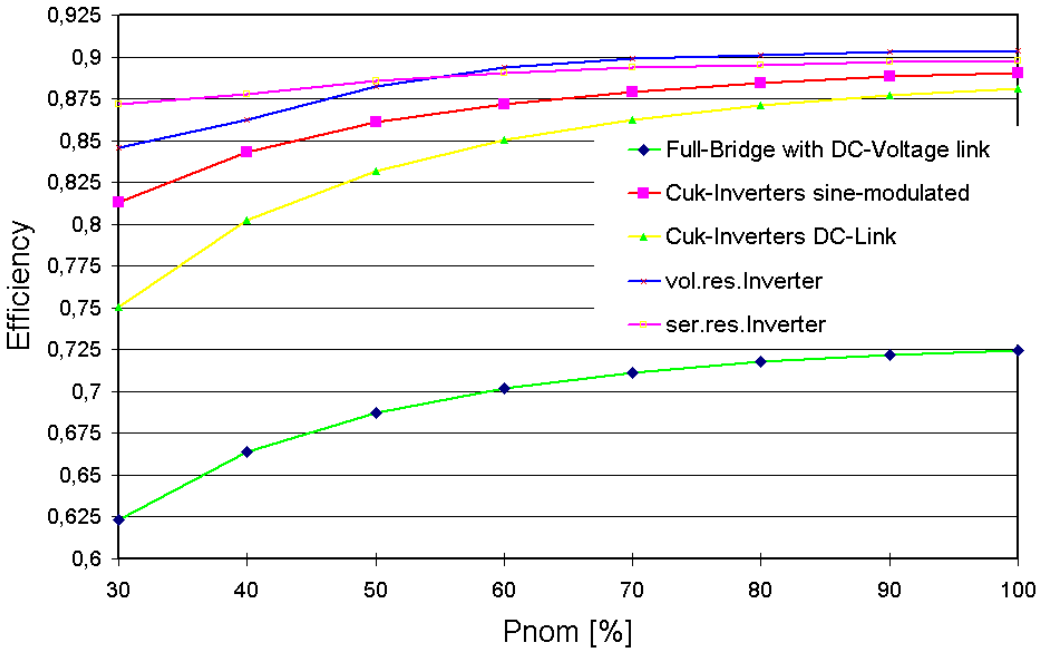

Fig. 8: Efficiency Estimation for Several Concepts @ 100kHz Switching Frequency

2.3 Half-Bridge Series Resonant Inverter

Due to the higher efficiency at low load the inverter concept with series-resonant converter has been chosen for the hardware realisation of the HICAAP Module integrated converter. The principle schematic is shown in fig. 9. [3] Main advantages of the SRC topology are the zero current switching characteristics at $\omega_{switch}<\omega_{res}$ and the current source behaviour over the complete range of operation. The latter feature makes this topology suitable for direct grid coupling inverters. The resonant frequency has been chosen to about 300kHz.

To emphasise the importance of the transformer leakage inductance as a significant characteristic of the topology, this inductance is shown as a separate device L_{res} in the schematic.

Initially, the capacitors C1 and C2 each carry have the input voltage. At turn on of either T1 or T2, the energy stored in the capacitors transfers to the resonant inductor. For example, at turn on of T1 C1 discharges across the inductor and the transformer and transfers the energy into the inductor. Since the capacitors C1 and C2 are in parallel the high-frequency circuit diagram, the effective capacitance for the resonance circuit is the sum of C1 and C2.

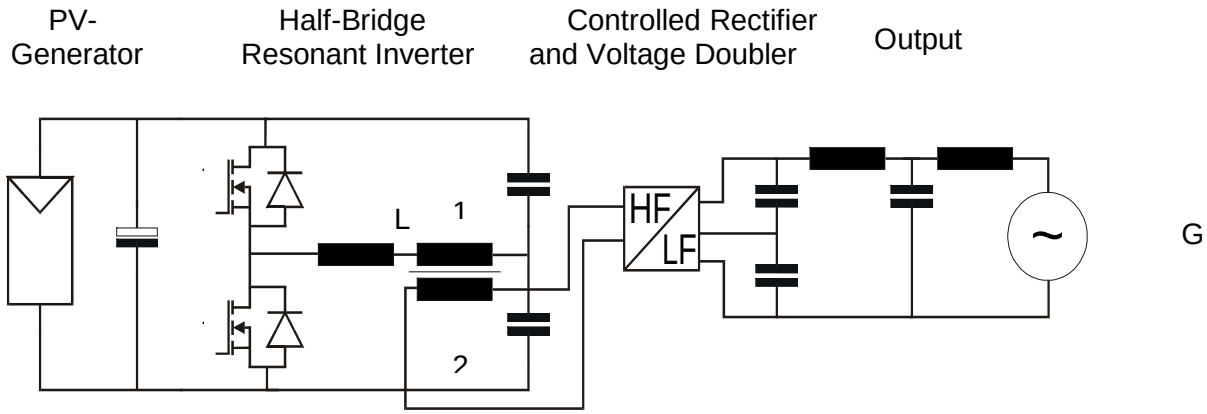

Fig. 9: Schematic of Inverter Topology

With a shorted transformer the initial driving voltage for the resonant inductor current is half the PV-panel voltage and the stored energy is $W_{C1}=\frac{1}{2}*2*C*(U_{C1})^2$. Assuming lossless conditions, this energy transfers completely to the leakage inductance and the maximum transformer current can be calculated from $I_{max} = U_{max}*\sqrt{\frac{2*C}{L}}$. Putting in the chosen values for C (270nF) and L (500nH) and assuming 36 volts for the MPP-voltage, the peak current at normal conditions results in 27A peak. When the voltage of C1 is zero, the transformer current reaches it's maximum value and reverses the capacitor voltages. Worst case, the peak voltage of the capacitor can reach twice the input voltage to the inverter. The current waveform and the voltage across the capacitor C2 are shown in fig. 10. Current and voltage are perfectly sinusoidal, the distortions are due to aliasing of the digital storage oscilloscope.

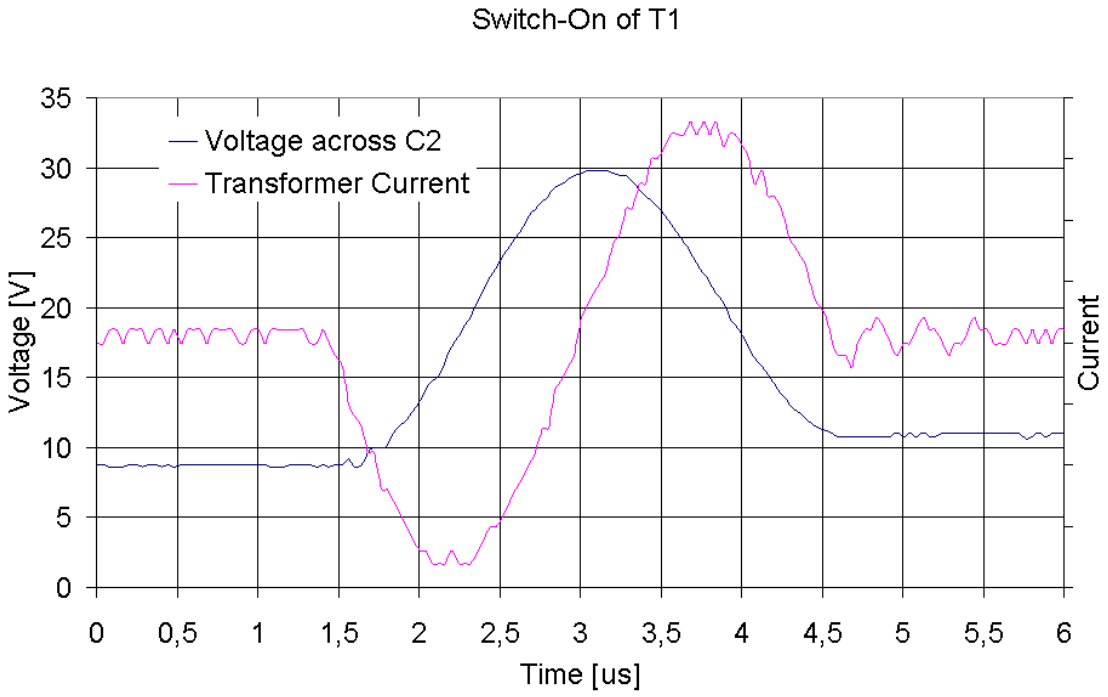

Fig. 10: Voltage Across the Capacitor and Transformer Current (Switch-On of T1)

The high current loads the MOSFETs and the reverse diodes, but divides on the two capacitors. This clearly shows the demand for expensive high quality devices.

This tremendous peak current causes significant losses in the switching devices (MOSFET and body diode) as well as the resonant capacitors. At intermitting operation, the losses in the body diode can be minimised by keeping the MOSFET switched on during the resonant cycle, so that the body diode of the MOSFET does not conduct. This produces some problems in the zero-crossing detection circuitry, since the first zero crossing needs to be neglected and the second detected safely. At non-intermitting operation, the inverter starts hard-switching. The need for a dead-time in the MOSFET operation causes the body diodes in the MOSFETs to conduct and the switching losses due to the reverse recovery time of the diodes get rather significant.

Another disadvantage of the chosen topology is the variable frequency operation mode. The output current of the inverter is controlled by changing the switching frequency of the inverter between a certain minimum and a maximum value. All frequencies in-between can occur so that any resonance in filters or the control-loop can be excited. This leads to considerable problems in EMC and the controls of the inverter. Some of these problems can be seen in Fig. 11.

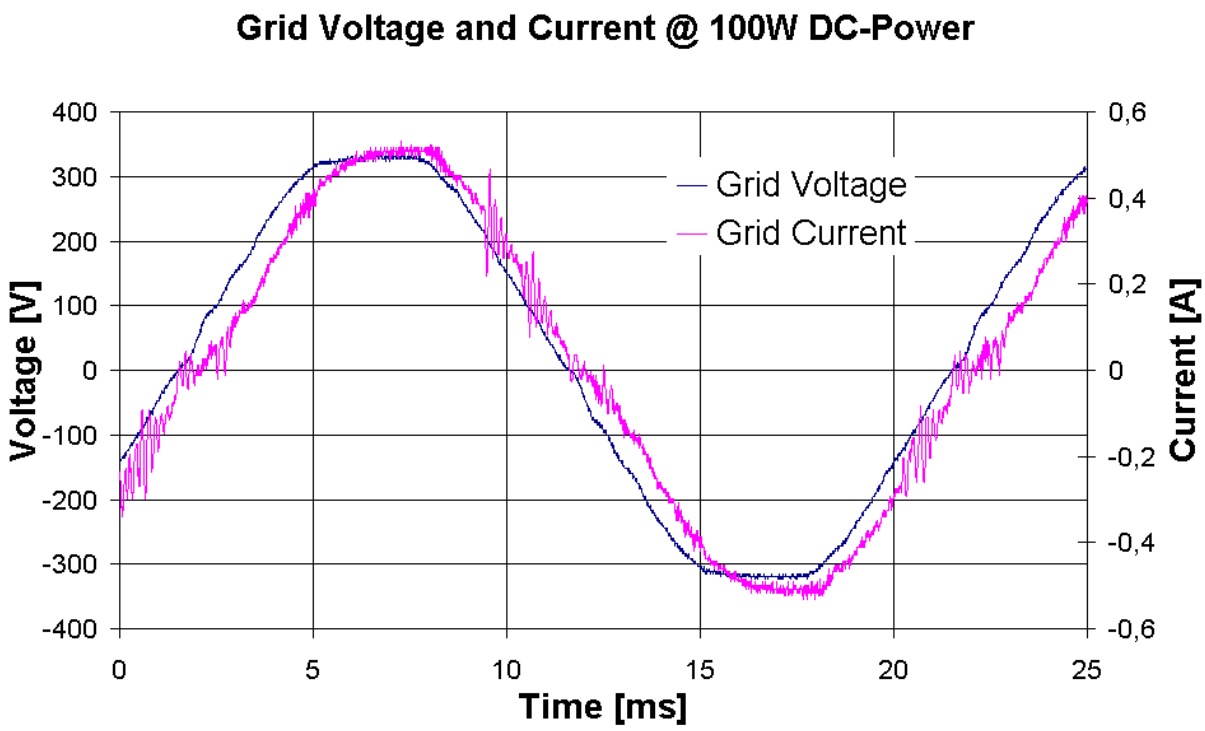

Fig. 11: AC Current and Grid Voltage

The phase offset between current and voltage is due to the command signal generation in the test set-up and is compensated in operation with the ASIC.

Since the single phase inverter has no natural continuous power output to the grid but a 100Hz modulated power, the DC-input needs to be filtered with an electrolytic filter capacitor. The resulting DC input current and voltage are shown in fig. 12. The filter capacitor is calculated so that the maximum voltage ripple voltage is maximum

5% at rated input current and voltage. The energy losses due to the ripple current of the PV-panel are negligible as can be calculated from the Eq. 1.

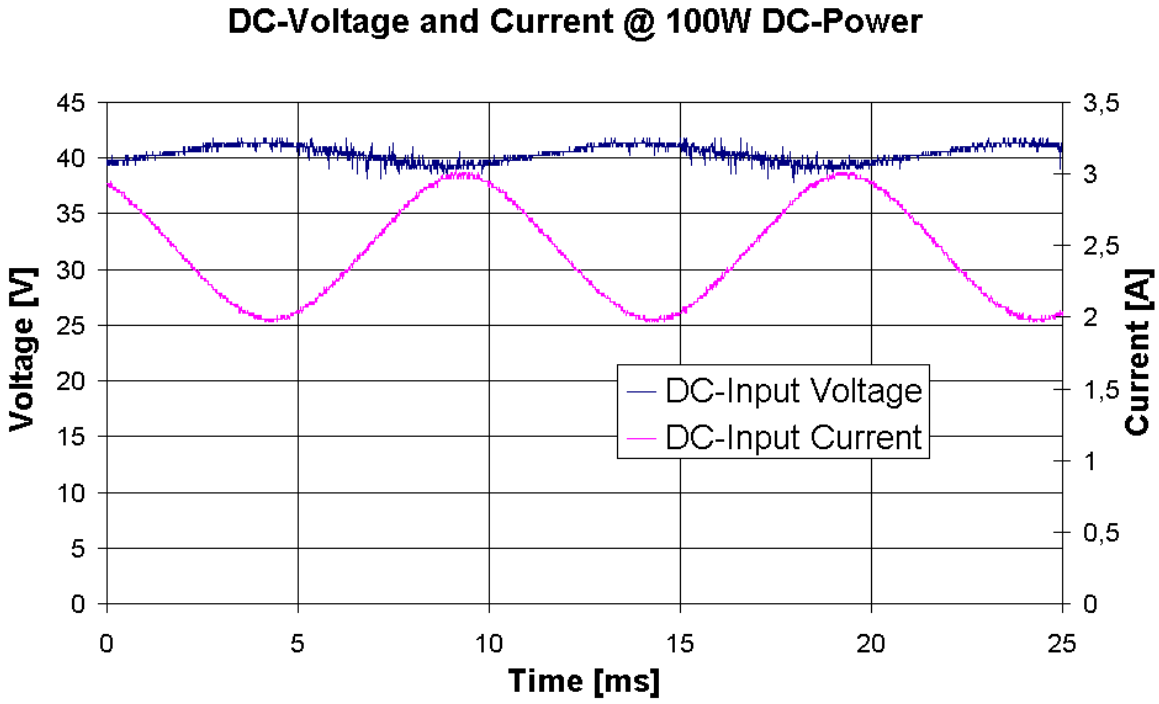

Fig. 12: DC-Input Current and Voltage

The variables a are c wildcards for the average DC-input current and voltage whereas b and d replace the amplitude of the superimposed AC components. The amplitudes of the AC components can be estimated from Fig. 12.

$$P(t) = \frac{1}{T}\int_0^T [a+b*\sin(\omega t)]* [c+d* \sin(\omega t)]dt$$

$$= a*c + \frac{1}{T}\int_0^T [b*c* \sin(\omega t)]dt + \frac{1}{T}\int_0^T [a*d* \sin(\omega t)]dt + \frac{1}{T}\int_0^T [b*d* \sin^2(\omega t)]dt$$

$$= a*c + \frac{b*d}{2} \qquad \text{Eq. 1}$$

The estimated values are:

a=2.5A c=40.3V b=0.5A d=1.2V

This clearly shows that the AC-component on the DC input values has almost no impact on the power output of the inverter. This results needs to be verified with the real combination of a PV module and the inverter.

Fig **13** shows a picture of the final laboratory test board.

Fig. 13: Photography of the Power Unit for the MIC

2.4 Cost Analysis

At the beginning of the project 40 topologies for DC/AC energy converters have been investigated with respect to their technical and economical parameters. Figure 14 shows the cost calculation results for the 5 best topologies.

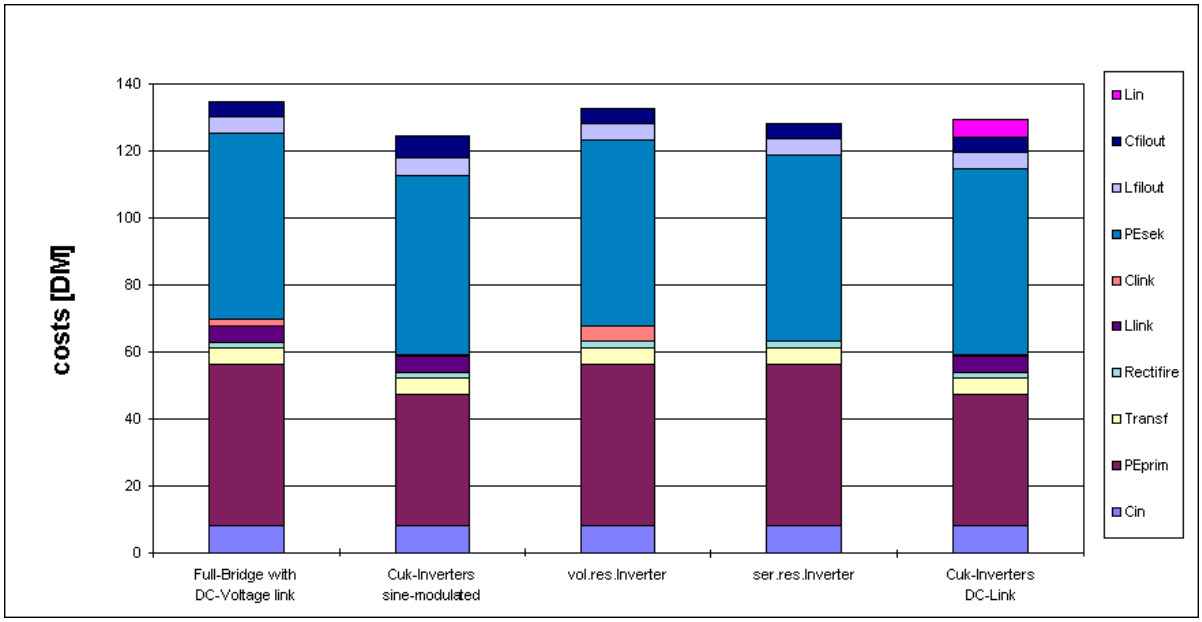

Figure 14: Costs of power electronics part for the 5 best inverter topologies based on a 110Wp inverter and material costs per 100 pieces

Cost reduction is a function of volume. Usually a cost reduction by 10 to 15% can be expected by doubling the number of pieces per year or per order. Forming this in a mathematical equation results in

$$C(n) = \left(\frac{n}{100}\right)^{0,77...0,85} * C(100)*100$$

Figure 15 shows the cost decrease as a function of quantity. The parameter is the cost degradation factor.

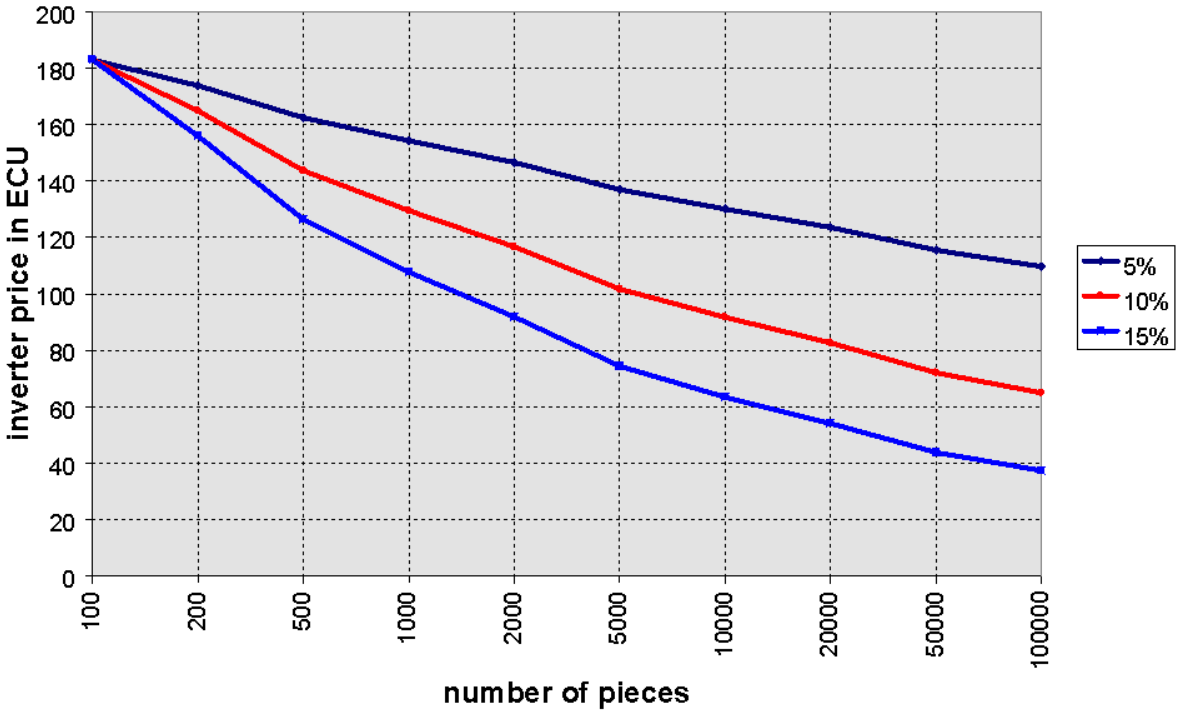

Fig. 15: Decrease of costs with increasing amount of manufactured pieces

Figure 15 shows that the expected cost for a Module integrated converter will be between 60€ and 130€ at 10.000 units per year. The manufacturing price estimation done by an electronic component manufacturing company is shown in Table **1**:

Table 1: Cost Calculation

1,000 units	~70€
10,000 units	~60€

These costs include the power parts and the controls of the inverter, some costs need to be added for the housing, connectors, cables etc.

The estimated costs for the MIC are close to the optimistic forecast, so the assumption of 15% cost degradation by doubling the units seems to be realistic.

The cost distribution of the inverter can be seen in fig. 16. The low voltage power unit still consumes a great portion of the overall costs (~26%). This is due to the high request for reliability and temperature stability as well as the high demand for high quality MOSFETs.

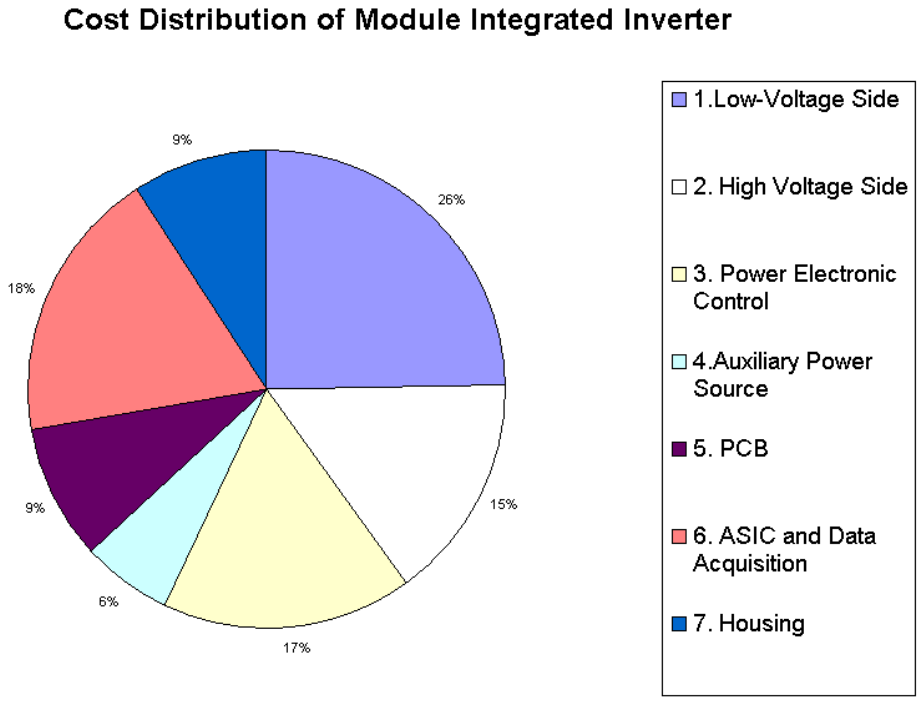

Fig. 16: Cost Distribution on the Single Units of the Inverter

There is a good chance of further cost reduction in the ASIC and Control unit since the price for the ASIC is mainly determined by the silicon area used. Decreasing the chip area by using more fine technology (i.e. using 0.35µm instead of 0.7µm) can cut the price for one ASIC almost by half.

3 Further work

Some things have not been tested during the project runtime:

- Integration of planar magnetic components
- Investigation of EMI while grid connected
- Investigation of reliability and robustness
- Behavior of several inverters in parallel

The output controlled rectifier is expected to be the most sensitive to disturbances from the grid. Since new components (COOLMOS, fast IGBT) got available within the last half year, the choice of the topology needs to be questioned again. Power

electronic component will be improved at the same pace as digital components so that the investigation of the best topology for a new development needs to be done more frequently and more concentrated on the products available in near future.

4 Acknowledgements

In the last two years different people have been involved in the HICAAP project. Authors of this report are:

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Dr. Ing. habil. Peter Zacharias, ISET

Part B: Market study and Temperature Distribution of PV Modules

5.1 Market overview of commercially available modules.

In order to develop an inverter with electrical specifications that matches the characteristics of the photovoltaic modules, we need to study the photovoltaic module market and the expected tendency of the market. We concentrated on the modules which possibly will be used as an AC module.

Table 1 gives an overview of module types with a nominal power higher then 100Wp of different manufacturers.

Manufacturer	Module type	Voc (V)	Isc (A)	Vmp (V)	Imp (A)	Pmax (W)	Size (mm)
GPV	GPV110M	43,3	3,7	34,2	3,2	110	650*1300
	120PXMP2	41,7	4,0	33,4	3,6	120	730*1450
Kyocera	KC120-1	21,5	7,5	16,9	7,1	120	652*1425
Neste	NM110G 12V	21,7	7,0	17,4	6,3	110	650*1293
	NM110G 24V	43,4	3,5	34,8	3,2	110	650*1294
Solarex	MSX240	85,2	3,8	68,4	3,5	239	1130*1908
	MSX120	21,3	7,6	17,1	7,0	120	991*1128
Siemens	SM110/12	21,7	6,9	17,5	6,3	110	660*1316
	SM110/24	43,5	3,5	35,0	3,2	110	660*1316
	SM100/12	21,0	6,5	17,0	5,9	100	660*1316
	SM100/24	42,0	3,3	34,0	3,0	100	660*1316
	SM110/12L	21,7	6,9	17,5	6,3	110	652*1307
	SM110/24L	43,5	3,5	35,0	3,2	110	652*1308
	SM100/12L	21,0	6,5	17,0	5,9	100	652*1309
	SM100/24L	42,0	3,3	34,0	3,0	100	652*1310
Shell (R&S)	RSM100	42,0	3,2	33,0	3,0	100	673*1308
ASE	300 G DFG50	60,0	6,2	50,5	5,6	285	1283*1892
		60,0	6,4	51,2	5,9	302	1283*1893
		64,5	6,7	51,7	6,1	315	1283*1894
Isofoton	I-100	21,6	6,5	17,4	5,7	100	651*1310
	I-110	21,6	6,8	17,4	6,3	110	651*1310

Table 2: Commercially available standard modules

The modules given in the above table are standard modules. Some manufacturers offer the possibility to manufacture custom sized modules. These modules can differ in terms of electrical and mechanical characteristics from the standard modules. These custom made modules are mainly used as facade and roof integrated units. In general, these units have more cells than the standard available modules. Nowadays the standard modules are mainly made for stand-alone applications with system voltages of 12V, 24V and sometimes 48V. One could predict that, as the grid connected market expands, the number of cells will increase.

Most of the modules are assembled with 100 X 100mm² (100cm²) cells but more and more multi-crystalline cells of 125 X 125mm² (156cm²) or 150 X 150mm² (225 cm²) are appearing on the market. With the increasing efficiency for bigger cells, the future modules will have power ratings as indicated in table 2.

	156cm² cells	225cm² cells
Systemvoltage 12V	85 Wp	120 Wp
Systemvoltage 24V	170 Wp	240 Wp

Table 3

5.2 Mounting of MIC to photovoltaic module

Figure 17 and Figure 18 present the temperature behaviour of module and module frame compared to ambient temperature for different insulation.

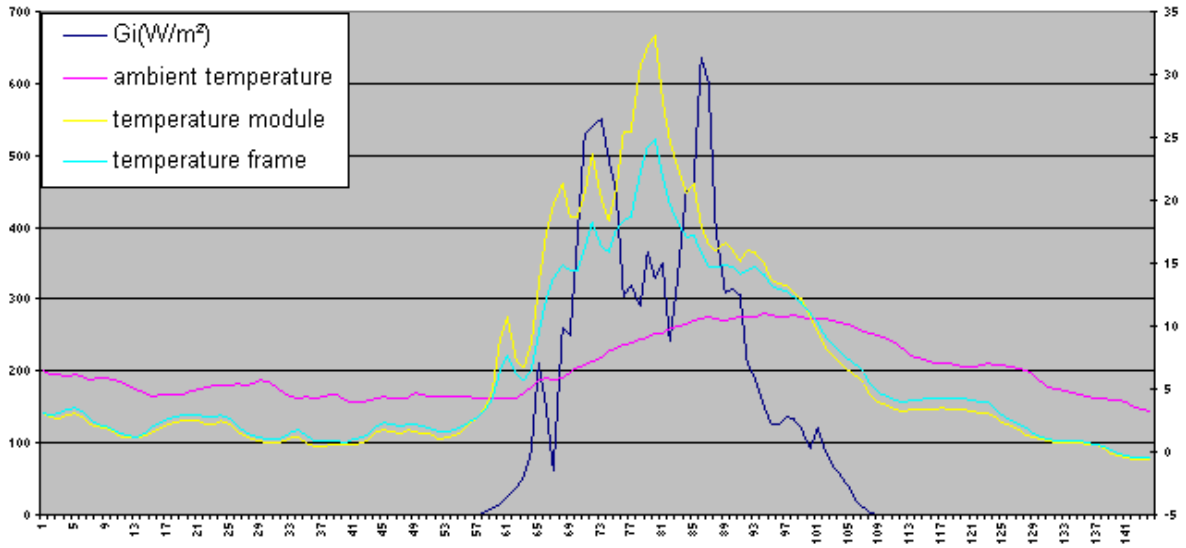


Figure 17: Temperature profile January

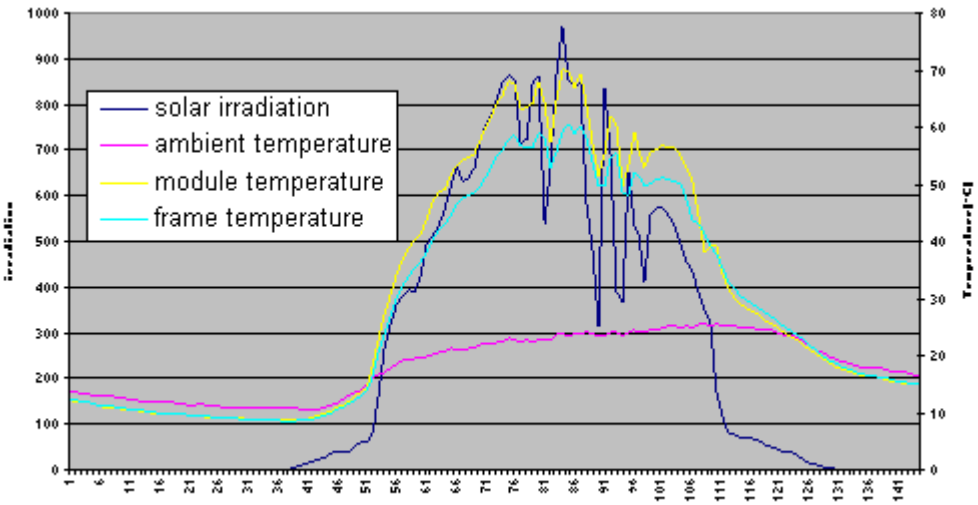


Figure 18: Temperature profile july

We notice here a temperature difference of up to 10°C between the back of the module and the frame. For this reason we can conclude that preferrably the mounting of the MIC should be done at the frame.

The frame will serve as a heatsink but also replacement of the MIC later is much easier compared to a MIC glued at the back of the module. A glued MIC to the back side is also to avoid becase of possible delamination of the back Tedlar foil from the module.

Figure 19 presents a relative cheap box composed with two aluminium extrusion profiles where in the middle a hole is foreseen for mounting to the frame with topping screws. A botom plate with a U shape can be mounted between two profiles. The MIC can be fixed between the two profiles and casted in polyurethan resin.

Figure 19

Figure 20 shows the mounting with long tapping screws to the frame. Finally the proposed mounting combines a cheap design with lower functioning temperature of the MIC, easier mounting and replacing and no possible damage cause for the module.

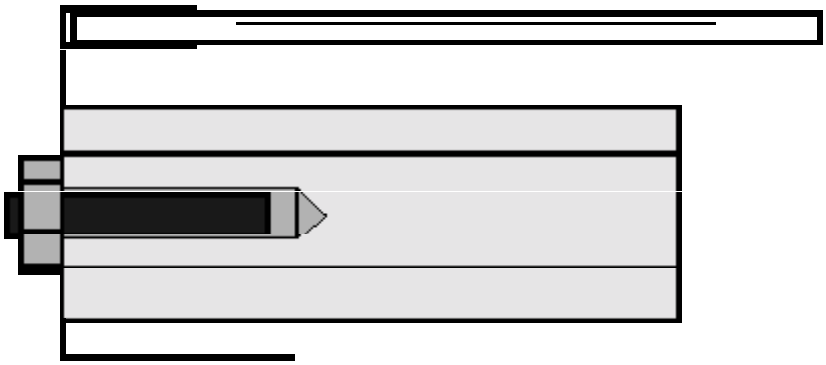


Figure 20

Part C: Design of Control Algorithm

6 Design goals, requirements and constraints

A control algorithm for the module-integrated converter (MIC) was developed at the Netherlands Energy Research Foundation (ECN). The design goals were:

- Optimization of the available solar power through minimization of the self-consumption of the inverter and optimal MPP tracking
- Safe and reliable operation of the MIC under all circumstances
- Delivery of power to the grid which is low in harmonic content

The main task of the controller is to generate the target output current value $I_{AC,set}$. This setpoint is based on the DC voltage setpoint $V_{DC,set}$ generated by the MPP tracking algorithm and on the operating point of the PV module.

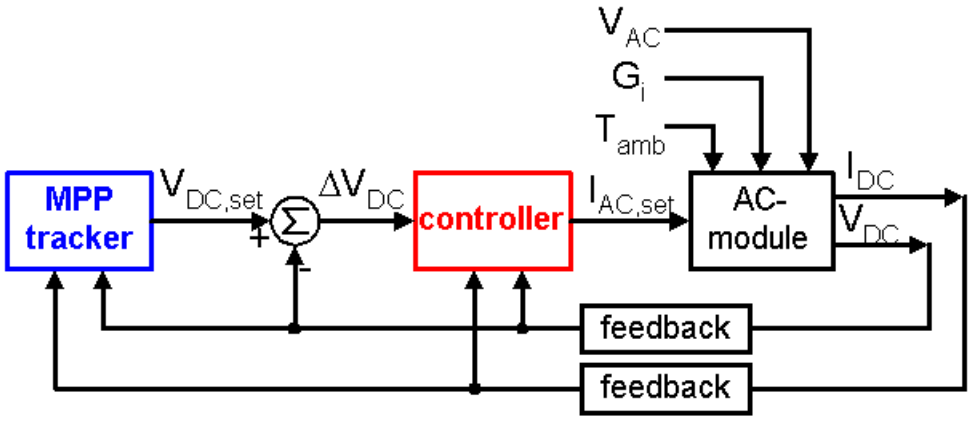


Figure 21: system block diagram

Figure 21 is the block diagram of the system: the “plant” is the inverter executing the conversion of the DC energy from the photovoltaic source to AC energy ready for grid injection. The control system consists of a MPP tracker and the controller.

The various disturbance inputs are the solar irradiance G_i, the ambient temperature T_{amb} and the disturbances in the grid voltage V_{AC}.

6.1 Control Algorithm

The controller uses a highly non-linear algorithm because of the non-linearity of the disturbance inputs G_i and V_{AC}. The control strategy is implemented as a state machine: the calculation of the output current set-point is different in each state, depending upon the operating parameters of the PV module and general safety- and grid-connection requirements.

Overall three modes can be distinguished: the start-up process, the burst-mode and the continuous mode. In the start-up process the controller passes through a number of stages, performing consecutive checks to assure a safe and correct operation of the controller at start-up. The controller passes through the booting stage in principle only once a day in the morning. The rest of the day while a minimal amount of solar irradiance is available, the converter is either active (controller in the 'continuous mode' or 'burst mode') or shut-down (controller at minimum power consumption). The controller dwells in this 'slumber state' at low levels of solar irradiance or in between power output 'bursts'.

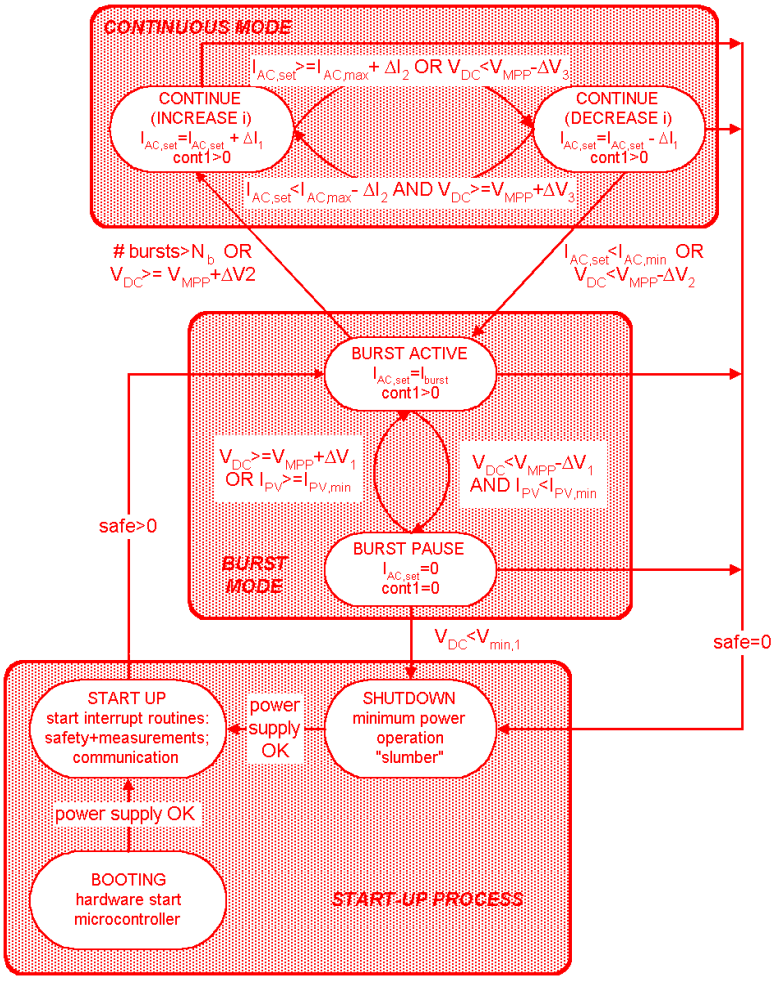


Figure 22: control algorithm State Machine

In the so-called ‘burst’ mode [4], the control system decides, based on an estimate of the power level, to alternate periods of zero output power with power delivery bursts during a number of grid cycles. At low power levels, the DC current from the PV module charging the input capacitor of the inverter is very small. The slow slew rate of the voltage across the capacitor allows to omit one or more full sine waves of

inverter output current, without this voltage exceeding a specified MPP voltage window. Once the upper limit of this window is reached the inverter can be activated for one or more bursts of power delivery, pulling the capacitor voltage down again the lower allowed limit (Figure 23).

The effect of the burst mode on the efficiency curve is such that the operating point simply skips the part of the curve where the efficiency of the inverter is really low (Figure 24).

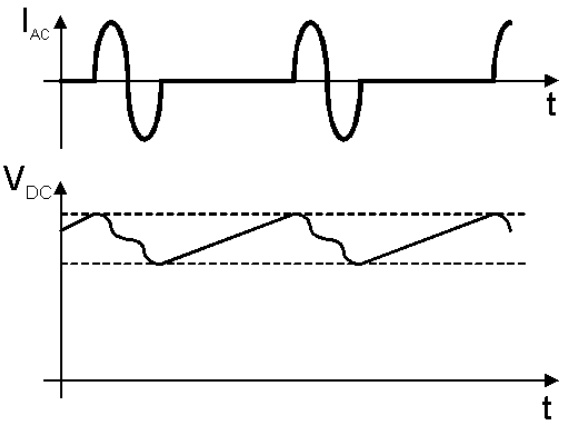


Figure 23: IAC and VDC during single bursts at low irradiance

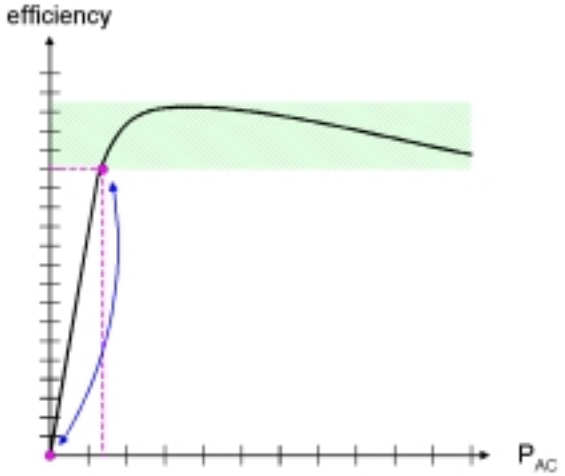


Figure 24: Effective efficiency curve through use of 'burst mode'

The continuous mode consists of two states: 'continue increase I' and 'continue decrease I'. Depending upon the level of the DC voltage the setpoint of the AC current is either incremented or decreased. The size of this step in the setpoint is dependent upon the deviation of the DC voltage from the MPP voltage. The MPP tracker calculates the MPP voltage. The AC current setpoint is updated only once every grid cycle to minimize the harmonic content of the current that is injected into the grid and eliminate a harmful DC component.

To add some flexibility to the ASIC controller and allow for fine-tuning of the algorithm the following parameters of the master controller were adjustable through a RS-485 interface with the chip: $V_{min,1}$,$V_{min,2}$,ΔV_1, ΔV_2, ΔV_3, $I_{ac,max}$, $I_{ac,min}$, ΔI_1, ΔI_2, $I_{PV,min}$, I_{burst}, N_b. These parameters determine the thresholds and hysteresis bandwidths of the transitions from one state to another, I_{burst} is the amplitude of the AC current setpoint in burstmode and N_b is the maximum number of bursts before switching to continuous mode (see also Figure 22)..

The minimal degree of flexibility was desired during the HICAAP project because the ASIC could only be manufactured once: this way it was possible to compensate for some inaccuracies during the design of the controller by means of a simulation model. This model is described in the fourth chapter. Of course, this flexibility is no longer required once the algorithm is optimized for a specific combination of PV module and power-electronic inverter: the interface with a PC can be left out and the control parameters can be fixed during ASIC production.

6.2 MPP tracker

The MPP tracking method is based on the ripple in the DC voltage and current. This ripple, inherent to the single-phase grid connection and the finite energy buffer at the DC side, provokes an oscillatory movement of the operating point along the I,V curve of the module. During the trajectory of the operating point along the curve the DC voltage and current are sampled at a high sampling rate and the corresponding DC power level is calculated. The large computational power of the Application Specific Integrated Circuit allows to calculate derived quantities from the measured parameters within one single grid cycle. Based on these quantities the average position of the operating point of the inverter is determined and the corrective measure to steer towards the MPP is taken.

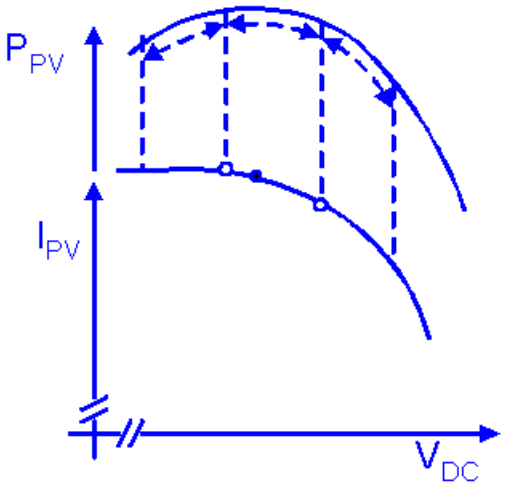


Figure 25: MPP tracking strategy

Hence the MPP tracker makes optimal use of computational power of ASIC without disturbing the DC-to-AC power conversion process. This is unlike other MPP tracking algorithms where intentionally the operating point is displaced to track the MPP based on the change of the DC voltage and current levels. These so-called 'perturbation and observation' methods could in fact cause the inverter to move away from the MPP and consequently will overcompensate this movement in the next corrective action. The method that is devised during the HICAAP project could be labeled ‘inherent’ perturbation and observation method because it uses the natural dynamics of the system. An extra benefit is that there are no unnecessary perturbations that might cause operation away from the MPP.

Again to enable the fine-tuning for optimal dynamic behavior once the prototype was manufactured the following parameters of the MPP tracker: K_p, K_1, K_2 were adjustable through an RS-485 interface with the ASIC. K_p is the proportional feedback factor of the DC voltage error in the AC current control loop; K_1 and K_2 determine the slew rate of the DC voltage setpoint.

7 Simulation Model and Results

A simulation model was built and translated into C code to verify and further fine tune the control algorithm and evaluate the MPP tracking.

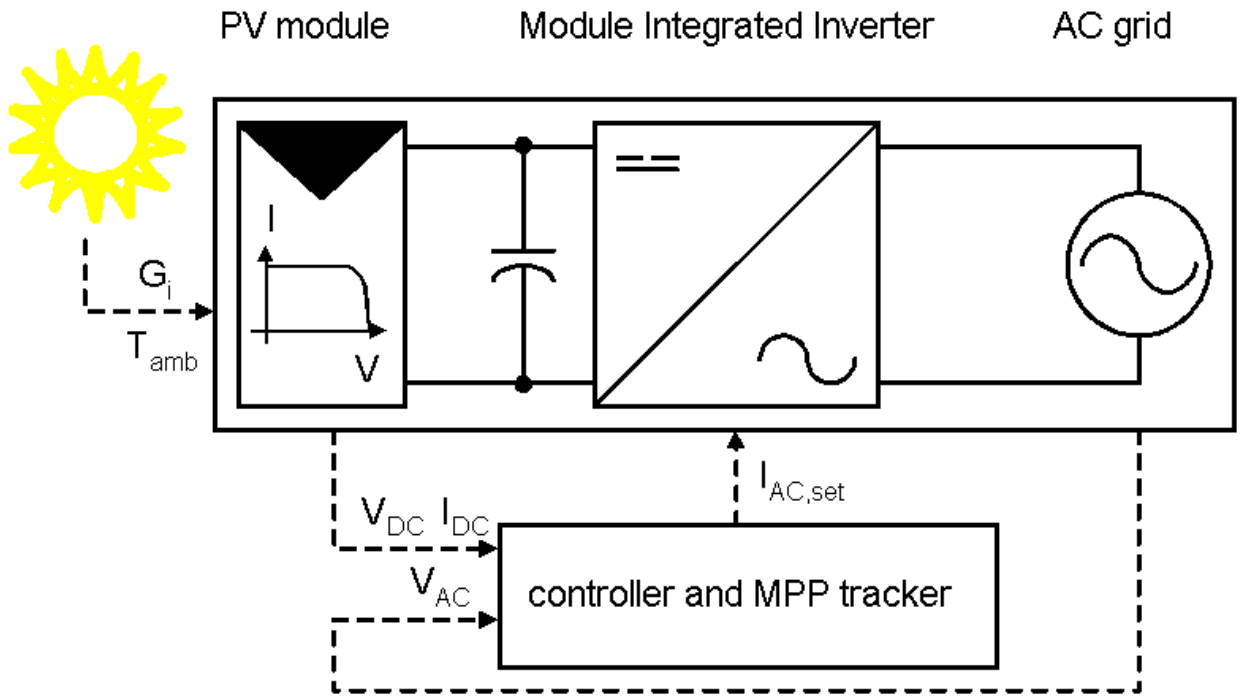


Figure 26: Simulation Model

Figure 26 illustrates the buildup of the simulation model. One file describes the behavior of the PV module depending upon the parameters of the cell technology, the levels of solar irradiance and ambient temperature and the DC voltage determined by the inverter. This inverter is modeled as an electrolytic capacitor and a power conversion unit with a certain efficiency. This idealization is justified because of the low amount of energy storage in the conversion unit compared to the DC capacitor. Two separate files describe the controller and MPP tracker, and finally one file acts as the master simulation file in which all disturbances (variations in solar irradiance) and the flow of interim results from one part of the model to another is coordinated.

The time steps in the various parts of the model are dependent on the required accuracy and the dynamics of the specific component. E.g. since the AC current setpoint is only updated every 20ms, the control and MPP tracker files are only executed with that same period; during each grid cycle however the calculation time step is equal to the sample period at which the ASIC measures the DC values.

This approach results in a powerful tool to design the MPP tracker and overall control strategy. The model is fast (simulation rum time is 10 to 20 times the simulated time when using a 120MHz Pentium processor PC), very flexible (each part can be investigated and fine-tuned separately) and accurate. The accuracy of the model is clearly illustrated by the following two pictures: the simulation results of Figure 27 almost exactly duplicate the behavior of the AC current, DC current and voltage and the DC power in the laboratory test result of Figure 28.

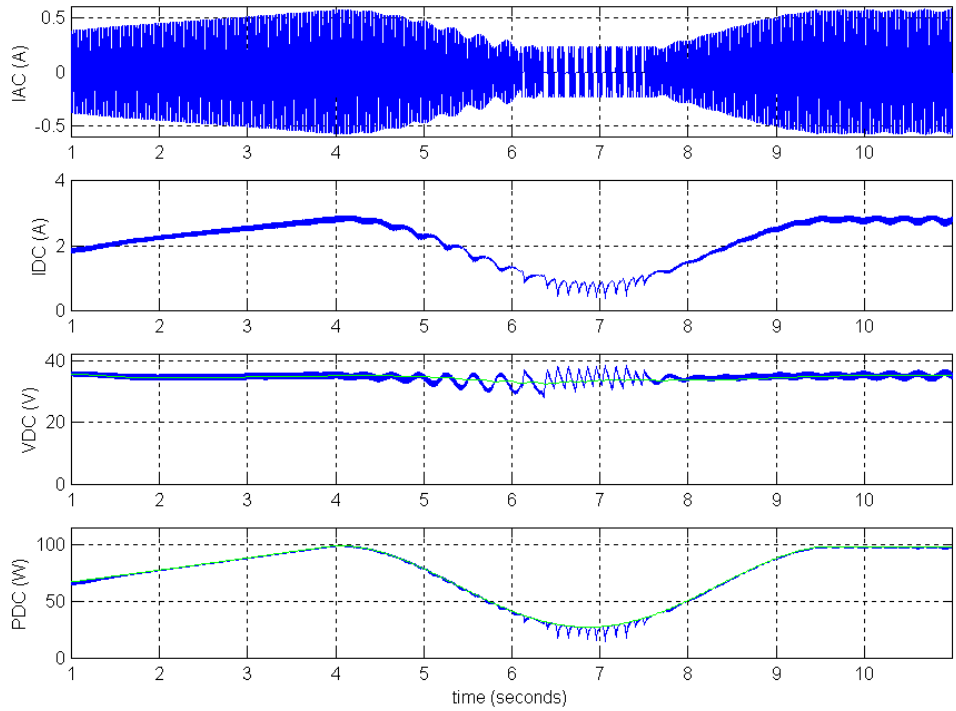


Figure 27: simulation result: sinusoidal variation of solar irradiance

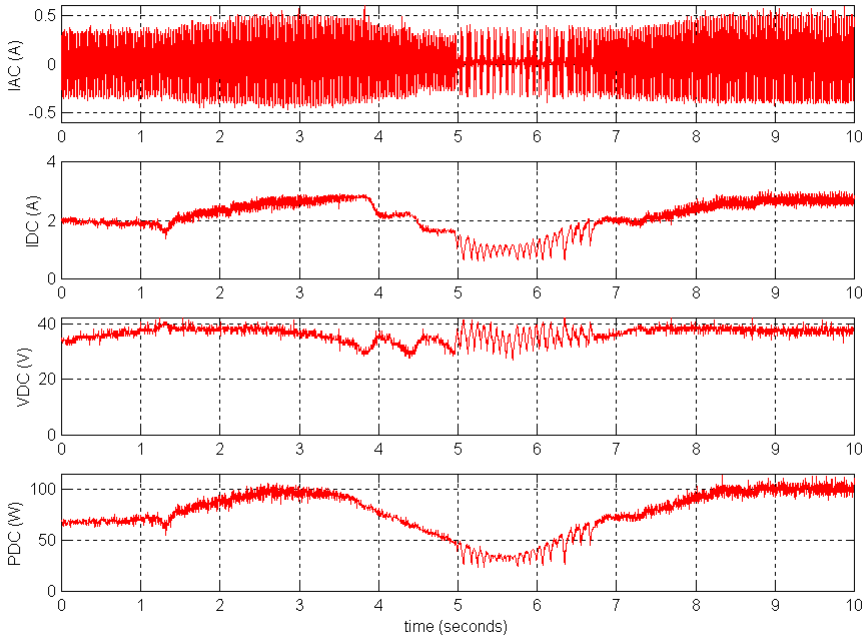


Figure 28: test result: sinusoidal variation of solar irradiance

8 Controller implementation in ASIC technology

The controller was implemented in ASIC technology by IMEC in Leuven. A PCB was designed to accommodate the ASIC and its socket together with the other components that make the controller print as shown on the picture of Figure 29.

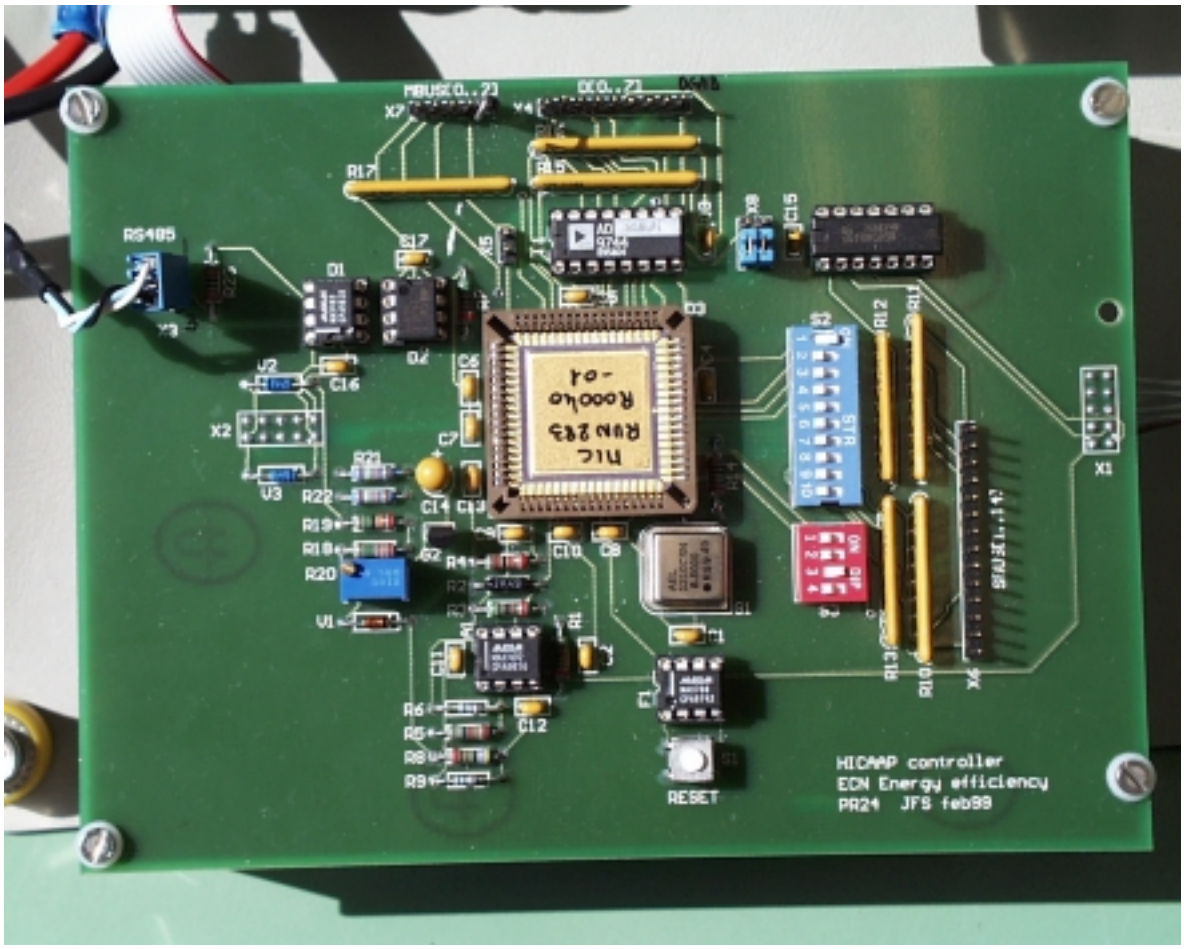


Figure 29: picture of controller PCB with ASIC

In the middle the ASIC in a 68-pins ceramic J-leaded Chip Carrier (JLCC) package sits in his socket. X2 (left) is the connector for the input-signals of the DC voltage, DC current, temperature, AC voltage and the supply voltage. X1 at the right hand side is the output connector for the safety signal, the AC current setpoint and the gate signals of the power-electronic switches on the AC-side.

The bulk of the components visible on the picture are merely for testing the various ASIC functions and fine-tuning the control algorithm. The RS485 connection to the PC together with the MAX483CPA IC (upper left corner) are necessary for modifying the parameters of the controller in the 'on-board' EEprom of the ASIC. The numerous resistor arrays and dip switches and measurements pins are incorporated to enable testing of the different operation modes of the controller and visualizing the in- and output signals on an oscilloscope. Leaving out all these components, the surface area of the controller PCB can be reduced by approximately 70%. Especially since all indispensable components are available in SMD technology.

9 Test results

Functional tests

First a series of functional tests were performed to verify the interconnections on the PCB and the proper operation of the basic functions of the controller:

- test of PCB lay-out, connections and the supply voltages
- test of the ASIC boot procedure
- test of the communication of the ASIC with a PC through the RS-485 interface
- test of the measurement and scaling of the input signals V_{DC},I_{DC}, V_{AC} and Temp
- tests of the ASIC clock frequency
- test of the operation and threshold levels of the safety shut-downs signals (grid frequency, grid voltage amplitude, over temperature, AC-side short-circuit protection
- test of the threshold levels of the 'islanding protection'
- test of the scaling and timing of the output signals (gate signals and AC current setpoint)

The timing of the gate signals of the output semi-conductor switches O1 and O2 is checked by plotting the signals together with the AC voltage (Figure 30) and on the same plot (Figure 31).

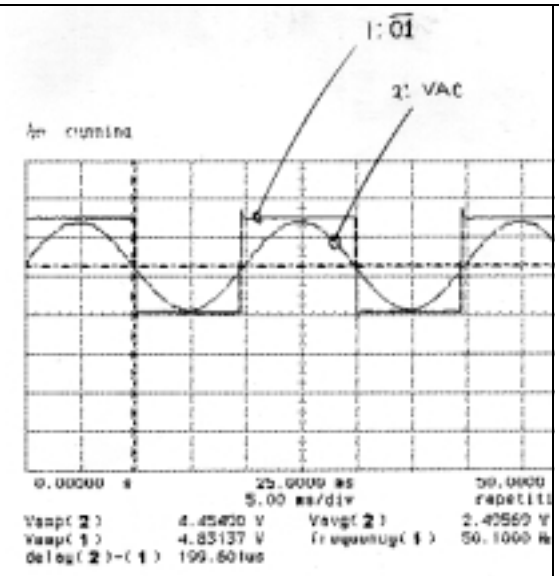


Figure 30: gate signal O1 with AC voltage

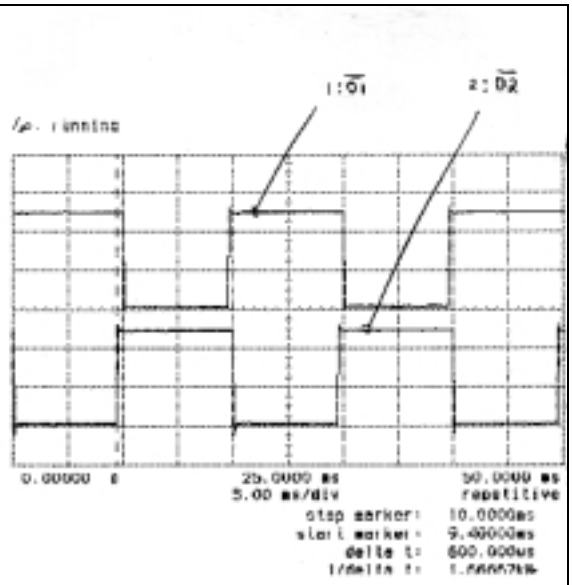


Figure 31: both gate signals O1 and O2

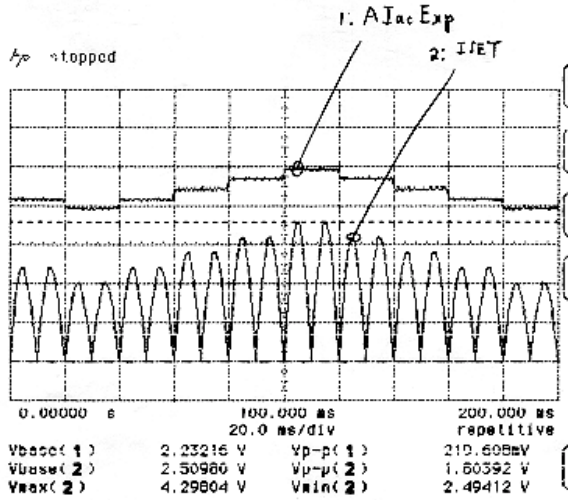


Figure 32: AC current setpoint signal

The AC current setpoint signal I_{set} was measured and plotted (Figure 32) with a simulated varying input DC power level: it can be seen that the amplitude of the AC current setpoint (AIacExp) only varies at the beginning of every grid cycle (20ms). Note that the I_{set} signals is the rectified signal of the actual 'target' grid current.

Once these tests were performed the controller was tested together with the power circuit PCB.

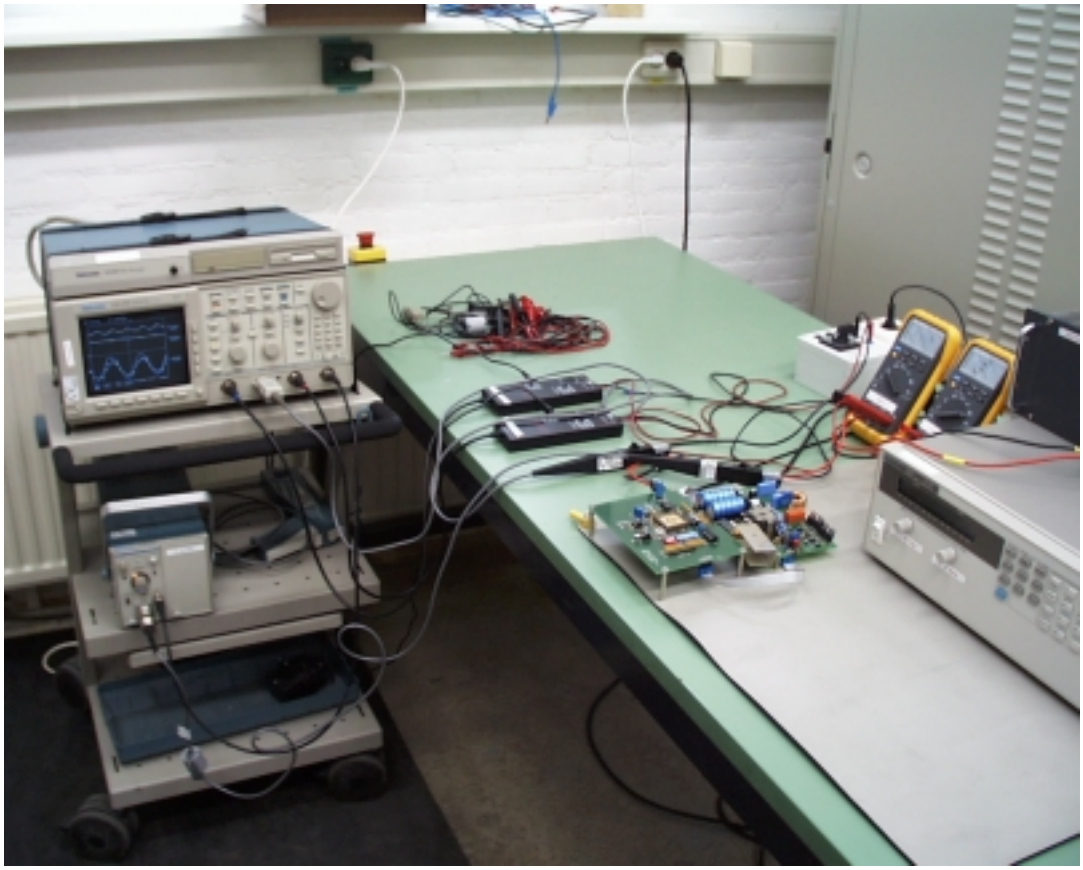


Figure 33: Laboratory set-up of combined controller-power circuit test

Connections between the two boards were made and real signals were supplied to the input connector of the controller PCB. Figure 33 shows the laboratory test set-up: the PV panel was simulated by means of a PV-array simulator and an ideal grid was supplied by a 4-quadrant switched power supply with adjustable voltage amplitude and frequency.

Fine-tuning of the control parameters

The next task was to fine-tune the control parameters. It was shown before that the simulation tool provided a fairly accurate prediction of the 'real world' behavior. However the total gain of the current control loop is also affected by the power circuit. Hence the default values of the control algorithm parameters will have to be changed for optimal result.

The following table lists the parameters of the control algorithm, their address in the ASIC EEprom, default value and the value after optimization:

ASIC address (decimal)	*name*	*function*	*Default value digital: MSB…..LSB decimal value*	*Modified?*
Control algorithm				
13	V_{min1}	lower DC voltage threshold before shut-down	0100 0000 1.25V	
15	$\Delta V1$	voltage hysteresis bandwidth during burst mode	0000 0010 0.039V	
16	$\Delta V2$	voltage hysteresis bandwidth of transition burst-continuous modes	0010 0000 0.625V	
17	$\Delta V3$	voltage hysteresis bandwidth during continuous mode	0000 1000 0.157V	
18	$AI_{ACburst}$	amplitude of AC current during bursts	0010 0000 = 32 *	
19	I_{ACmin}	minimal amplitude of AC current setpoint	0001 1000 = 24 *	
20	I_{ACmax}	maximal amplitude of AC current setpoint	0010 0100 = 36 *	
21	I_{Pvmin}	PV current lower threshold during burst mode	1000 0000 1/2 of full scale	
22	$\Delta I2$	current hysteresis bandwidth during continuous mode	0000 1000 = 8 *	
23	Nb	maximal number of consecutive bursts	0000 0100 = 4	
24	I_{oc}	minimal current level at start-up in open-circuit condition	0100 0000 1/4 of full scale	
25	K_p	proportional gain of DC voltage error in AC current setpoint increment $\Delta I1$	0100 0000 0.125	Yes 0.03125

* the scaling of the current levels is done after multiplication with the sine-wave

MPP Tracker				
53	SF	determines V_{MPP} setpoint at start-up	1100 0000 $0.74*V_{OC}$	
54	$V_{MPP\ min}$	lower threshold V_{MPP} setpoint	0100 0000 = 64	
55	$V_{MPP\ max}$	higher threshold V_{MPP} setpoint	11000 0000 = 192	
56	$V_{MPPfactor}$ (K1)	determines slew rate of VMPP setpoint ($V_{MPP}=K_1*V_{DC\_maxP}+ (1-K_1)*V_{MPP\_old}$)	0000 0001 1/2	Yes 1/32=0.03125

In addition the following parameters of the safety watchdogs can be set:

Anti-islanding protection				
41	Tmax	determines the over-temperature protection threshold	1100 0000 3/4 of full scale	
43	NrOfCKSMinL	determines maximum frequency threshold of anti-islanding protection	1110 0111 50.5Hz	
45	NrOfCKSMaxL	Determines minimum frequency threshold of anti-islanding protection	0001 1001 49.5Hz	
46	RMSmin	determines minimum voltage threshold of anti-islanding protection	0011 1100 $V_{AC,nom}$-20%	
47	RMSmax	determines maximum voltage threshold of anti-islanding protection	0100 1110 $V_{AC,nom}$+6%	

Initial adjustments were made to the gains of the operational amplifiers that translate the current signal of the AC current setpoint into a voltage signal: increasing the gain was necessary to achieve an adequate amplitude of the control signal. During the laboratory tests most attention was paid to the optimization of the dynamic behavior of the controller-power circuit combination in the continuous mode. This was done by comparing the response of the inverter to various patterns of fluctuating solar irradiance. Finally, an averaged optimal setting was chosen for the parameters K_p (current control loop feedback gain) and K_1 (slew rate of VMPP setpoint).

A more detailed and comprehensive optimization of the control algorithm parameters is certainly going to improve the performance of the controller. Especially further investigation of the best settings for the threshold levels that dictate the transitions from one state to another will enhance its capability of maintaining the operating point in the MPP of the PV module.

Plots of Test results

The following plots illustrate the performance of the controller when tested together with the power circuit under laboratory conditions.

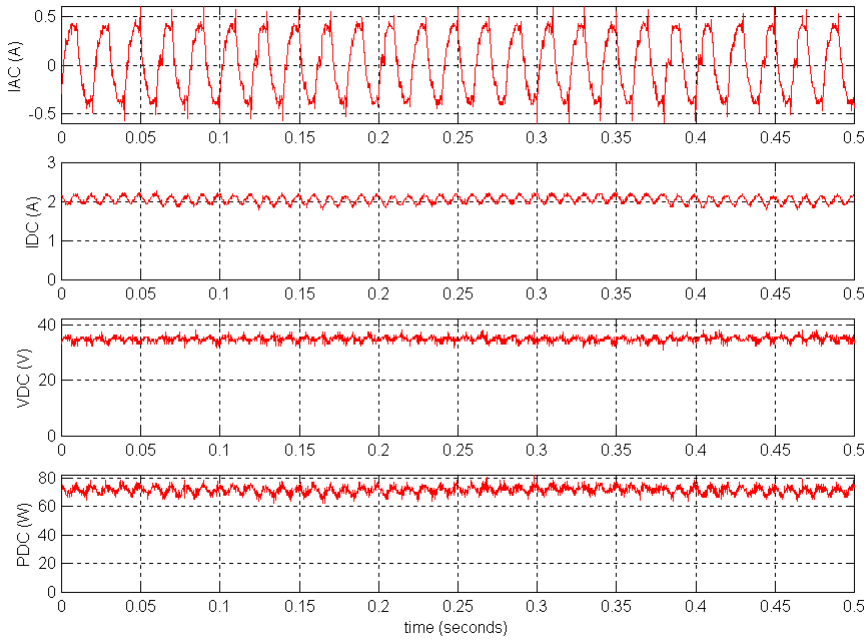


Figure 34: steady-state operation (constant solar irradiance)

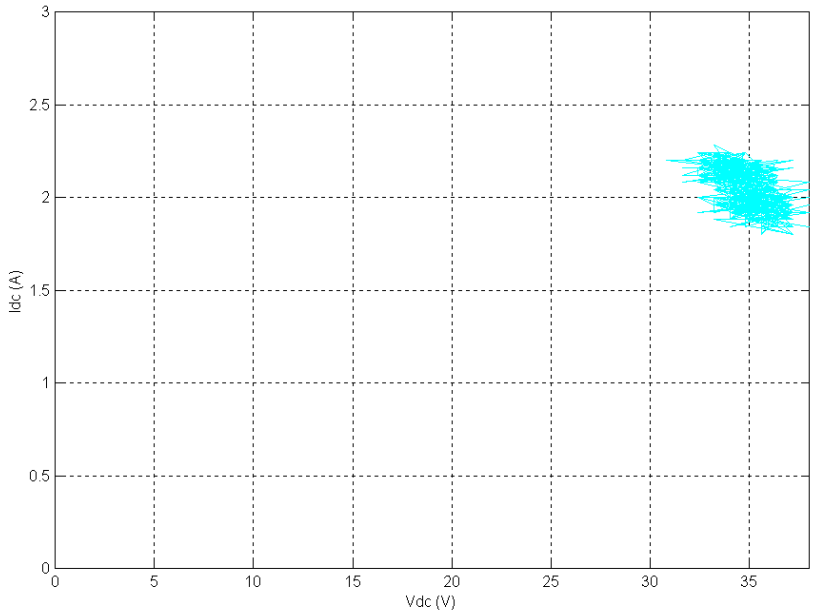


Figure 35: operating point trajectory in the I,V plane during steady state behavior

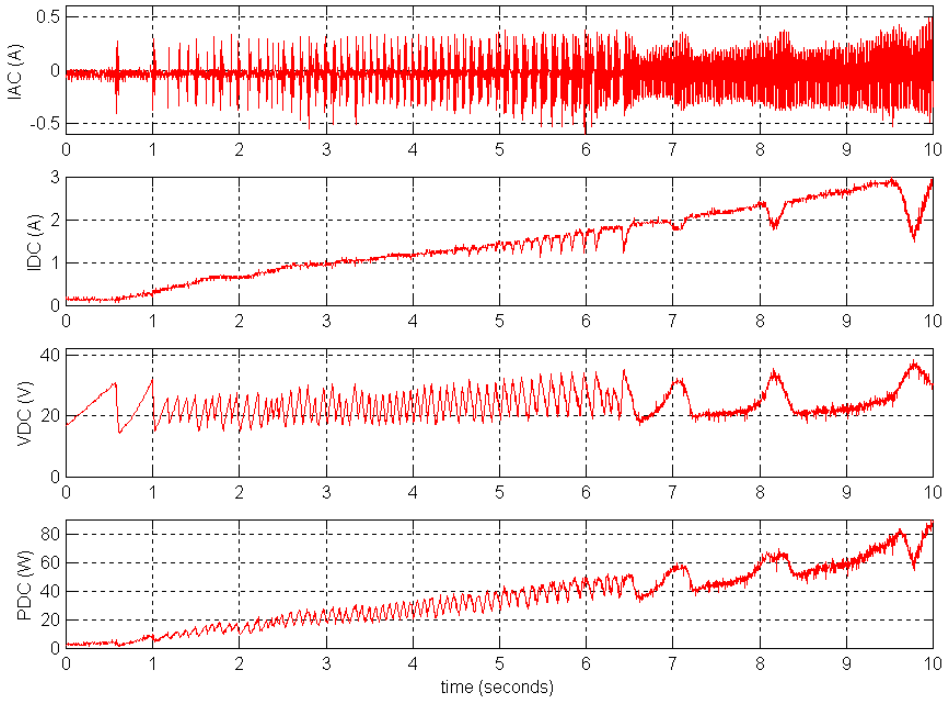


Figure 36: increasing solar irradiance

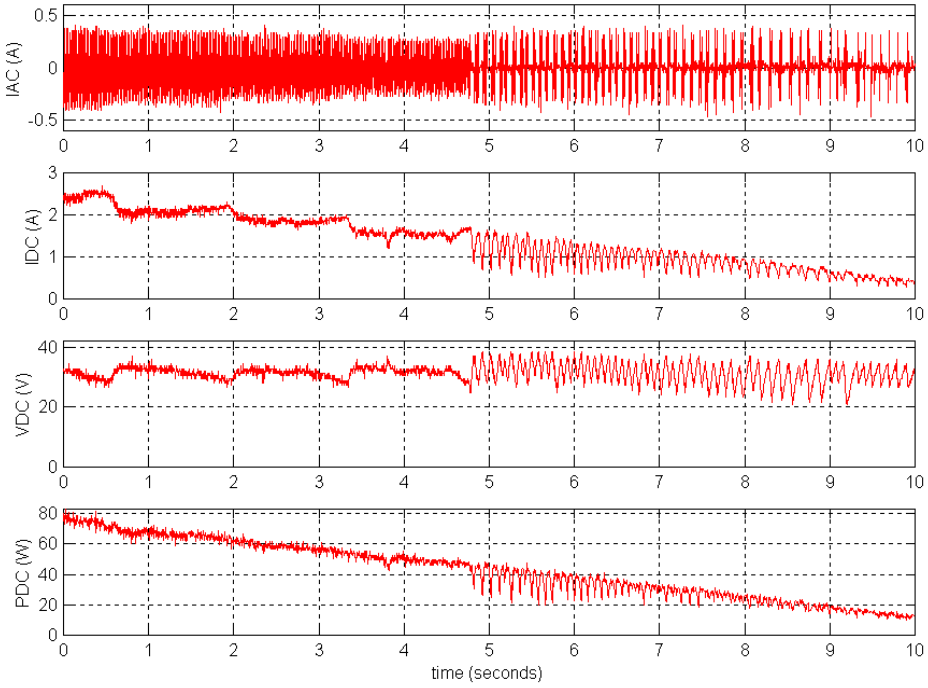


Figure 37: decreasing solar irradiance

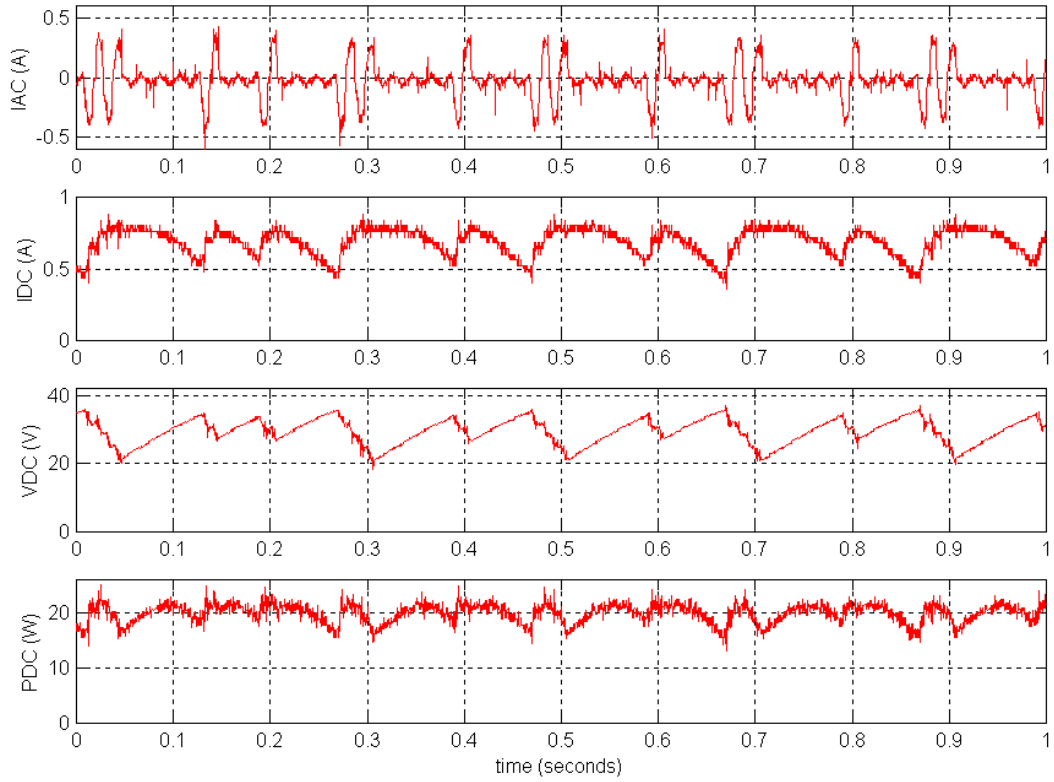


Figure 38: burst mode operation

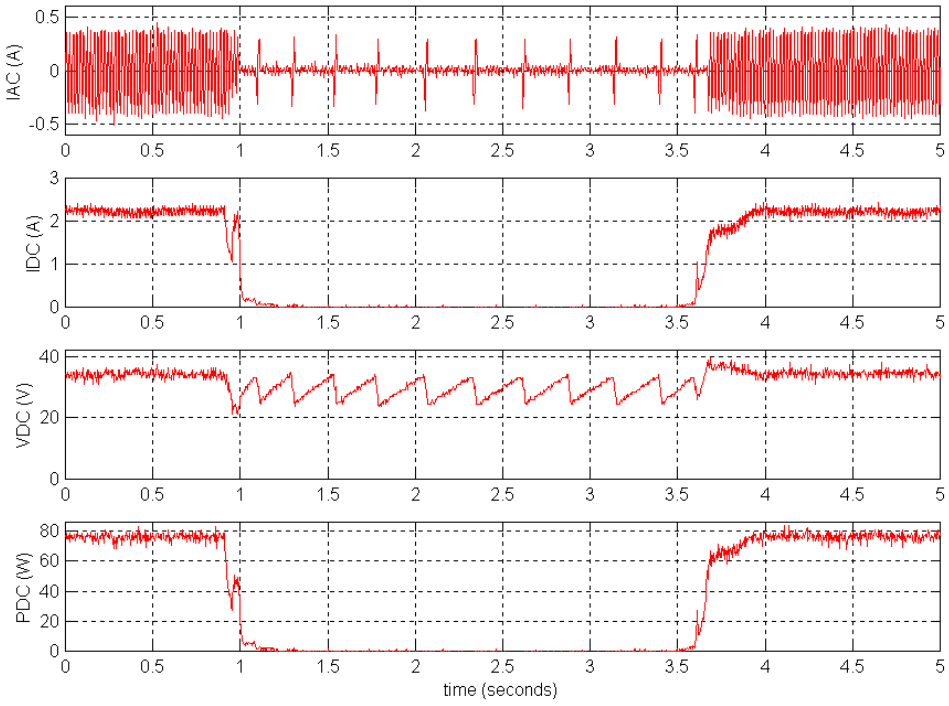


Figure 39: 'white clouds' day

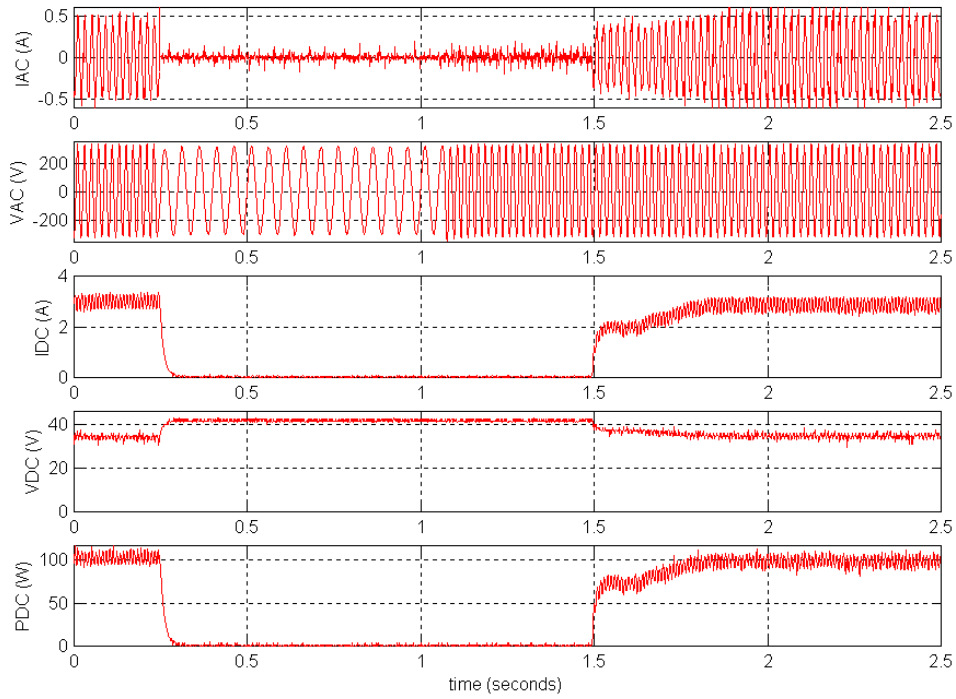


Figure 40: anti-islanding protection: grid frequency

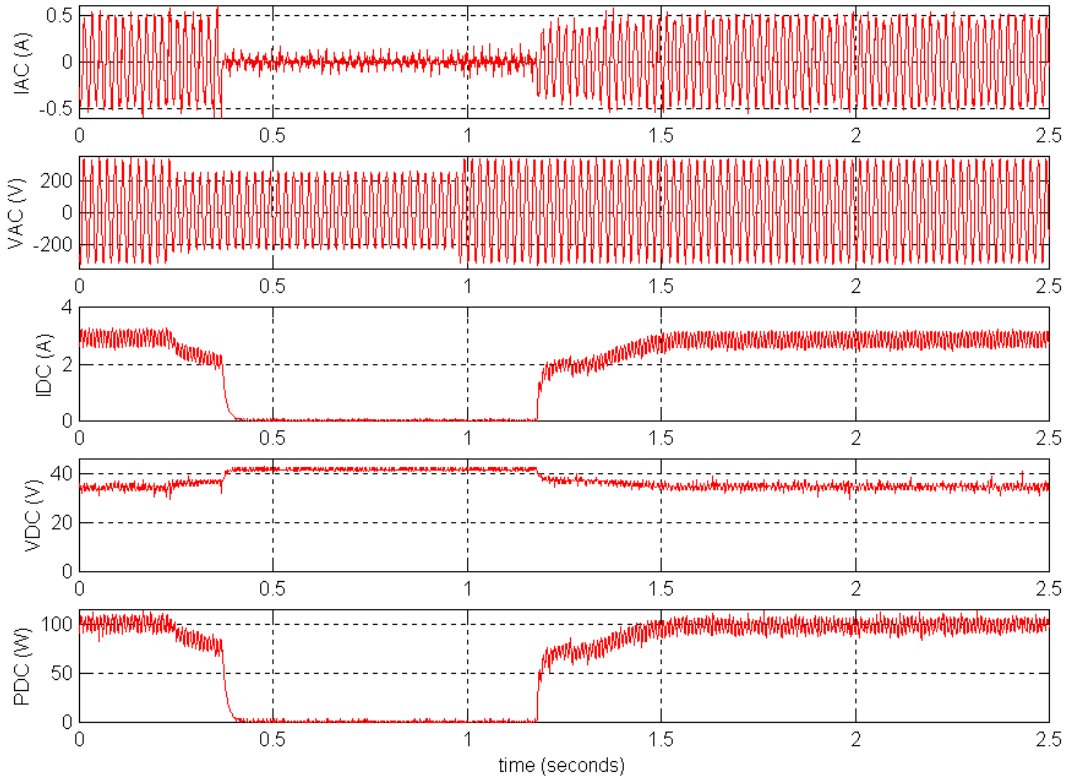


Figure 41: anti-islanding protection: grid voltage amplitude

Figure 34 shows the time series of AC current, DC current and voltage and DC power during steady state operation (i.e. constant solar irradiance) over a period of 25 grid cycles. The prototype of the power circuit used during the tests lacked an output filter: in the final design the spikes in the AC current will be suppressed. The 100Hz ripple in the DC quantities is clearly visible. Figure 35 shows the trajectory of the operating point in the I,V plane of the -simulated- PV module. The inverter operates around the 'knee' of the I,V curve where the MPP is located.

Figure 36 and Figure 37 illustrate the operation of the inverter when the solar irradiance gradually increases (Figure 36) or decreases (Figure 37). In both cases the transition from burst mode to continuous mode is characterized by an increase (decrease) of the number of bursts until the irradiance level is sufficiently high (low) to start (halt) the continuous power delivery to the grid. Note that at low solar irradiances the DC voltage level is kept above $20V_{DC}$ to ensure the power supply of the control circuit.

Figure 38 zooms in on the burst mode operation: the solar irradiance and thus the available DC power is such that the inverter is alternating bursts of one and two grid cycles. Every other time the electrolytic capacitor is discharged twice as long and hence the DC voltage decreases to a lower value. The number of grid cycles during which power delivery is omitted is either 2 or 3.

Figure 39 is the result of a brief 'outdoor' test: the inverter was connected to a PV module sitting in the sun outside the laboratory building. It was a bright sunny day with no clouds. To simulate the effect of a white cloud suddenly blocking the sunlight, someone stepped in front of the module and covered most of the cells with his shade. The plots show how the inverter reacts to the sudden drop in input power by instantly decreasing the DC current to almost zero. The small current caused by indirect sunlight or the cells that were not completely shaded, then charges the DC capacitors. As soon as the DC voltage reaches a threshold, the controller commands to inject current into the grid for one complete grid cycle. As soon as the person stepped away from the module, the controller establishes the operating point again at the MPP.

Figure 40 is the reaction of the inverter to a abrupt decrease in grid frequency: it can be seen that the anti-islanding protection works correctly and shuts down the inverter immediately. A drop in the voltage amplitude to 70% of its nominal value triggers an inverter shutdown within 7 grid cycles (140ms). This is compliant with the most rigorous requirements of the utility companies and with the IEC standards.

Acknowledgements: The authors wish to thank Carel Frumau and Jan Secker for designing the analog signal processing circuitry and Tim van Engelen for translating the simulation model in C code.

Part D: ASIC Design and Functionality

10.1 ASIC functional specifications

A summary of the ASIC functionality is listed below:

- System interface
- Drive the rectifier switches for the power electronics part synchronously with the grid voltage
- Generate the current set-point proportional to the amount of power to be transferred
- Sampling and filtering of the analogue inputs
- Implementation of the safety routines
- Programmable minimum and maximum grid frequency
- Programmable minimum and maximum RMS value
- Programmable maximum temperature
- Maximum power point tracking
- Implementation of a algorithm which transfers the power in bursts in case of low-level irradiation to minimise losses in the system.
- kWh counter
- Feature to the customer to monitor the kWh produced by the module.

10.2 ASIC block diagram

The ASIC has been implemented by way of a number of finite state machines running in parallel. Most of the units run at a slow 12.8 kHz (256 samples in a 50Hz period) while only a few units run at 8 MHz which is indicated in the block diagram below. The ASIC is started by an external reset signal after which the parameters plus the previous value of the kWh counter are transferred from the EEprom into the ASIC. After this the A/D is started and the filtered signals are processed by the Safety Check unit and by the Grid Synchronisation unit. When the conditions are safe the MPPT tracking and the master controller starts driving the PCC and the MDAC. When the safety conditions are not met or when the DC power becomes too low the updated kWh counter is transferred again to the EEprom and the power transfer is completely stopped.

The drawback of a fixed architecture in the ASIC is partially compensated by adding a large number of parameters in the ASIC which are loaded at start-up from an EEprom. This together with some additional test logic to monitor some internal busses and a PC interface to modify the parameters gives the flexibility which is needed for the prototype.

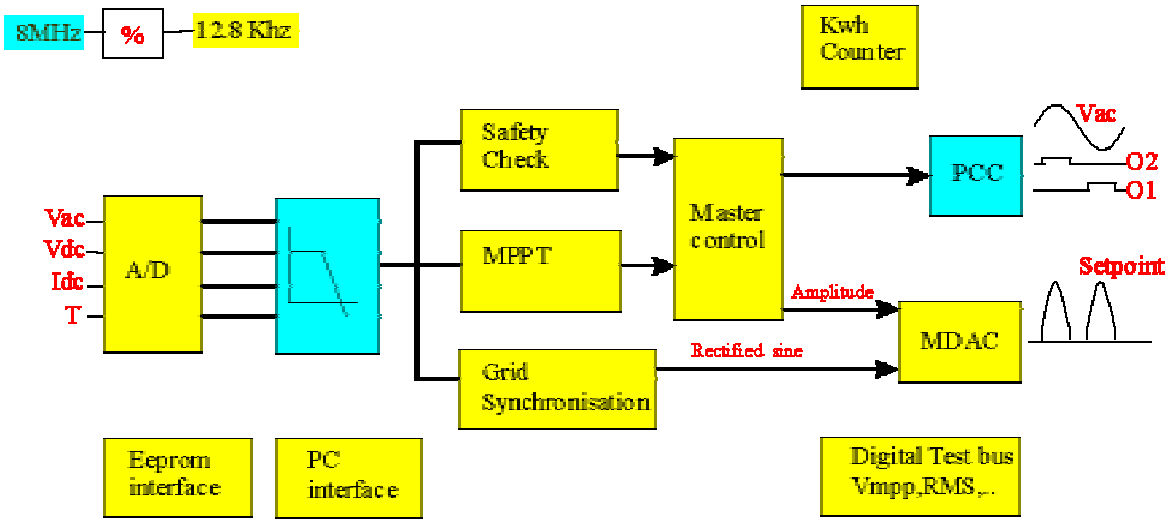


Fig. 42: ASIC Structure

11.1 Front end units

11.1.1 Sample system

The A/D converter has a maximum clock frequency of 500 kHz which means that 3 out of the 4 analogue signals can be sampled in one 12.8Khz period. The grid voltage and the dc current are always sampled while the dc voltage is always sampled except once every 10ms when the temperature is sampled instead.

11.1.2 Filtering

Since the grid synchronisation is based on zero-crossings of the grid voltage a 2nd order low pass Butterworth filter is implemented to avoid any jitters on this zero-detection. Some characteristics of this filter implementation are :

Coefficients : 16 bit, intermediate results 24 bit

Rounding, no clipping

Multiplications are implemented in a serial way

Bypass of the filter possible

In combination with this Butterworth filter it is also possible to integrate up to 8 samples and to base the zero-detection on the sign inversion of this integrated value.

For the dc current and voltage a simple filtering is implemented :

VdcFil = (7*VdcFil(N-1) + VdcSam(N))/8

IdcFil = (7*IdcFil(N-1) + IdcSam(N))/8

Also these filters can be bypassed.

11.2 Core units

11.2.1 Grid synchronisation

The synchronisation to the grid is not based on a kind of PLL but on a circuit which runs on the fixed 12.8 kHz clock. The principle is that a prediction is made for the next zero-crossing and the deviation between the real zero-crossing and the measured zero-crossing is used to compensate during the next half period as indicated in the figure below. Half of the deviation is corrected when the sine reaches its maximum or minimum while the other half is corrected at a zero-crossing. When a zero-detection occurs outside the predicted window or when no zero-detection occurs within the window the inverter will be temporarily switched off till the zero-detection is in the window again. The width of this window is a parameter which is stored in the EEprom.

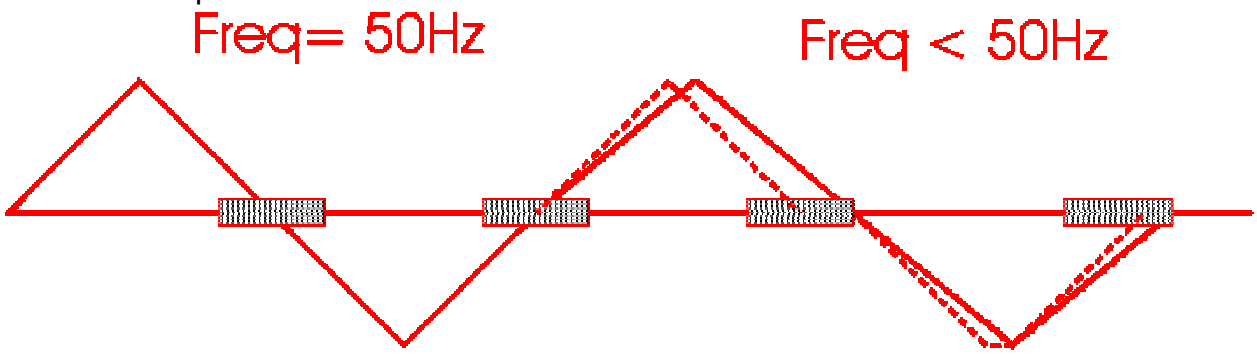


Fig. 43:

The phase delays of the grid voltage added by e.g. the filtering and integration can be compensated.

11.2.2 Safety checks

Frequency check

The frequency of the grid voltage is checked by measuring the number of clock periods between a programmable number of zero-crossings(1-255). By selecting the number of zero-crossings it is possible to exchange measurement speed by accuracy.

RMS check

Since the grid voltage is a sine the RMS is approximated by 1.11 x average of ABS(Vac). The ABS(Vac) is accumulated during a programmable number of zero-crossings(1-8) and divided by the number of clock periods. The same remark for speed and accuracy as for the frequency check applies here.

Temperature check

This is a simple check where the temperature input is compared with a programmable maximum.

When any of the above checks fail the master controller will stop the power transfer at the next zero-crossing of the grid voltage.

11.2.3 MPPT and master controller

These units are described in the part written by ECN

11.2.4 kWh counter

The kWh transferred to the grid is calculated from the dc inputs taking the efficiency of the inverter into account. The formula implemented is: $P_{ac} = K*(P_{dc}-P_o)*(1-C*P_{dc})$ where $P_{dc}=I_{dc}*V_{dc}$ and K,C and P0 are parameters which have to be measured.

Two more parameters have been added to this unit :

- the value representing a 10Wh equivalent
- the number of 10Wh increments which are needed before transfer to the EEprom (at shutdown the kWh counter is always transferred to the EEprom)

11.2.5 Multiplying DAC

This analogue unit multiplies the amplitude of the current set-point created by the master controller with the sine wave produced by the grid synchronisation. It produces a current synchronous with the grid and proportional to the amount of power to be transferred. Around the zero-crossings this current will be zero as shown in the next figure.

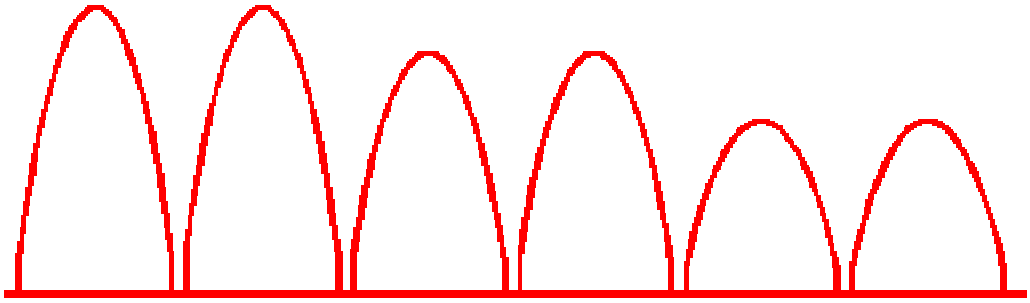


Fig. 44: MDAC Output to the Power Electronics, Synchronous to the Grid

11.3 Interfaces

11.3.1 PC interface

The ASIC contains an interface which can drive an RS485 transceiver. The commands which are recognised by the ASIC are Reboot, Read kWh counter, Read a parameter from ASIC or EEprom and Write a parameter directly to the ASIC or to the EEprom. The protocol contains an ASIC identifier allowing 255 units to be connected to the same PC.

Some characteristics of the implemented interface are :

rate : 1200 bits/second

data length : 8 bit

1 start and stop bits

no parity, but checksum

communication : half duplex

11.3.2 EEprom interface

A standard I2C bus interface has been implemented. The clock frequency equals 12.8KHz/4 = 3.2KHz, resulting in a total booting time of 250 ms. The flexibility of the ASIC is mainly obtained by the introduction of parameters in the EEprom. A grab of some parameters stored in the EEprom is listed below:

Idnr	ID number used by PC-interface
kWhGen	kWh counter Increment & store increment Efficiency curve parameters
Master control	e.g. Amplitude in burst mode
PCC	Switch-off delay for the MOSFETs (125 ns resolution)
Synchronisation	14 parameters e.g. phase delay to be compensated Window around zero-crossings
Safety checks	8 parameters e.g. minimum and maximum frequency
MPPT	4 parameters
Vac filter	10 parameters

11.4 Test modes

For testing the prototype several extra test pins and modes have been inserted. The most important test features are :

Test	mode	
00	normal	Normal operating mode
01	scan	Scan configuration
10	analogue	Check AD and DAC
11	Bypass AD	Apply digital instead of analogue inputs

By setting some test inputs it is also possible to :

- Bypass the clock divider
- Bypass the safety routines
- Directly control the power transfer

11.5 Layout

The ASIC has been processed in a 0.7µ process.
Package : JLCC68

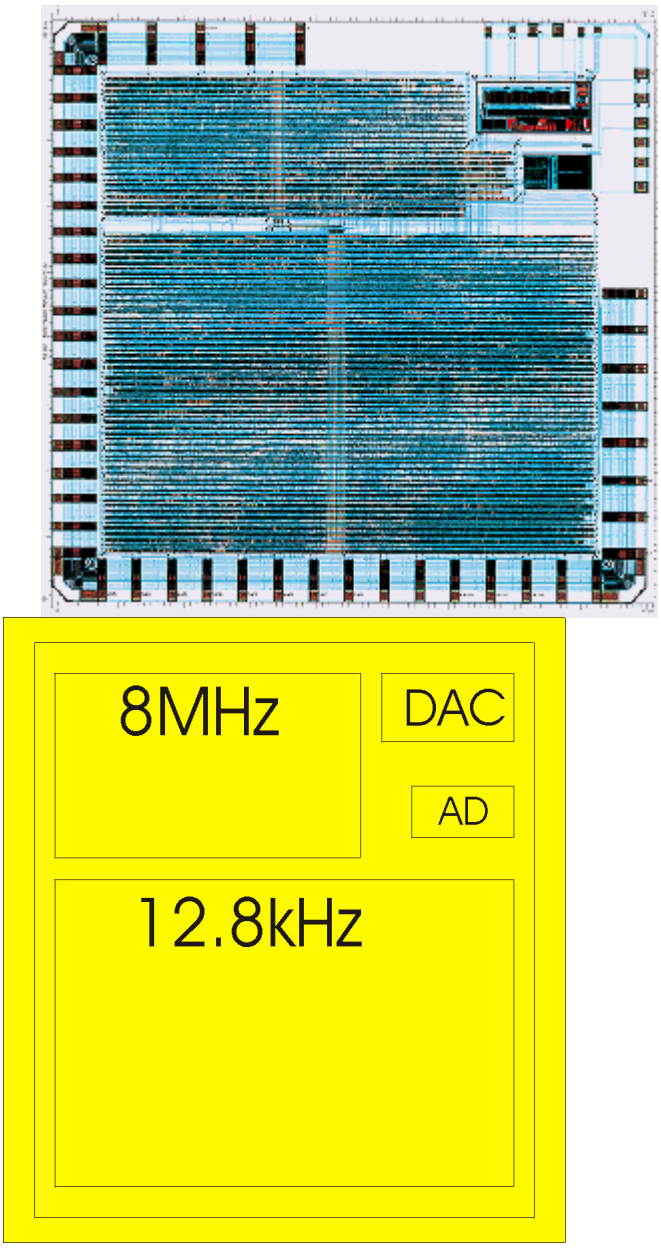


Fig. 45: ASIC Chip Apportionment

Only 28 pins are functionally needed, all other pins have been added to test the prototype. Test results

Power consumption : 255 mW

Functional tests

EEprom interface :	ok
RS485 interface :	ok
AD and DAC :	ok
Safety routines :	ok
MPPT tracking and global control :	ok
Complete system (PV-ASIC-power_electronics) :	ok

Part E: Thermal Design, Lifetime Optimisation and Integrated Magnetic Component Design

12.1 Structure and mode of operation of the MIC

The block diagram in Fig. 46 illustrates the structure and components of the MIC. The topology used in the design of the MIC has very good efficiency in partial load range. It has been selected out of 36 available topologies, which are discussed in [2]. The solar module on the left generates a maximum power of 110 W at a voltage between 26 V and 37 V. The DC-filter capacitor (1) is used to filter the 100 Hz pulsation of the power typical for single-phase applications. The resonant converter (2) consists of a single half-bridge, resonant circuit and transformer. In order to increase the efficiency and decrease the required size of the converter the resonant inductance and capacitance are integrated in the transformer and the half-bridge respectively. The switching frequency of converter MOSFETs is up to 500 kHz. The controlled rectifier (3) is realised as diode half-bridges which are alternatively switched on and off by MOSFETs switching with 50 Hz. The AC filter (4) ensures compatibility with the EN standards. The control unit (5) includes the fast control and trigger equipment for the resonant converter, the control for the rectifier and the supervisory control, which is responsible for maximum-power-point tracking and the unity power factor operation of the MIC. Also some safety issues like the monitoring of the MIC's internal temperature are carried out by the control.

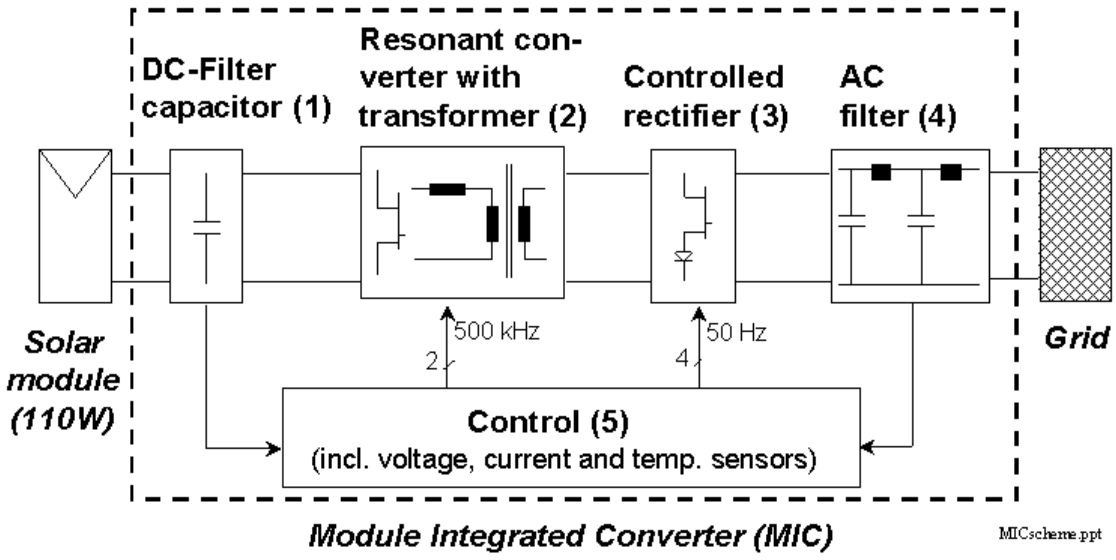


Fig. 46: Schematic of the Module Integrated Converter.

13 Power electronics packaging of the MIC

Why "Low Profile" MIC Design ?

The back of the solar module gives a relatively large area for mounting a MIC and it seems to be no direct need for miniaturisation of the entire MIC. However, it is

proposed to target a “low profile” MIC design with a high power density for the following reasons:

1. the simplified thermal model [7] shows that a decreased height of a MIC leads to reduced component temperatures and consequently to a higher reliability of the MIC;
2. the MIC can be mounted easily to the frame of the solar module and due to the reduced weight, the mechanical connection is more reliable and cheaper;
3. the power density of power supplies is commonly used as a general measure of technical advancement; a comparison of power densities of MICs in [8] shows that the first generation MIC prototype has twice the power density of commercially available MIC while having a similar footprint;
4. a smaller amount of potting material required for encapsulation (reduced costs).

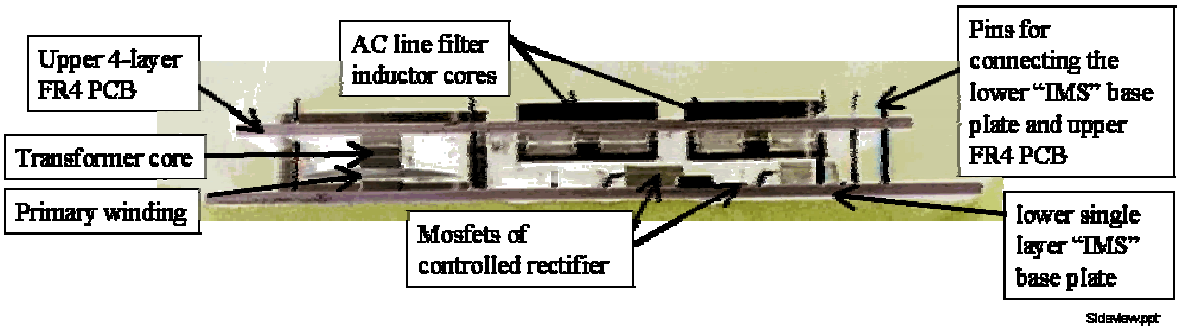


Fig. 47: Side-view of the 1st generation prototype of a Module Integrated Converter for PV application (height 1.5cm).

13.1 Internal packaging concept of the MIC

The physical realisation of the electrical circuit and the arrangement of the main components in the 1st generation “Low Profile” prototype of a MIC are shown in Fig. 47 to Fig. 49. The side view in Fig. 47 shows that circuitry of the MIC is spread over two circuit boards. The lower board (shown in Fig. 48) is the Insulated Metal Substrate (IMS) with a single conduction layer, containing all power dissipating components such as MOSFETs and diodes as well as the magnetic components. The upper substrate is realised as a 4 layer Printed Circuit Board made of FR4. The FR4 board (shown in Fig. 49) contains the windings of the transformer and the inductors of the AC line filter as well as the control and measurement circuitry. Through-hole components (e.g. DC capacitors) are also connected to the FR4 board. This “Double Decker“ design (Fig. 49) leads to a very good thermal behaviour of the MIC due to the excellent thermal conductivity of IMS, combined with the opportunity to build the control circuit on both sides of a 4 layer PCB and to integrate the windings of the planar magnetic devices into this PCB. Two rows of pins are used for the electrical and mechanical connection of the upper FR4 board at a clearance of 7.5 mm above the lower IMS board.

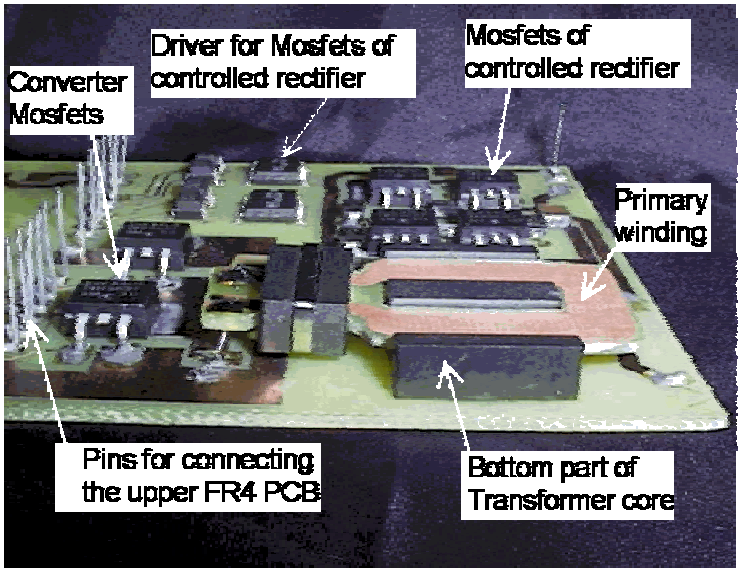


Fig. 48: Top-view of IMS base plate of the 1st generation prototype of the MIC (upper FR4-PCB removed).

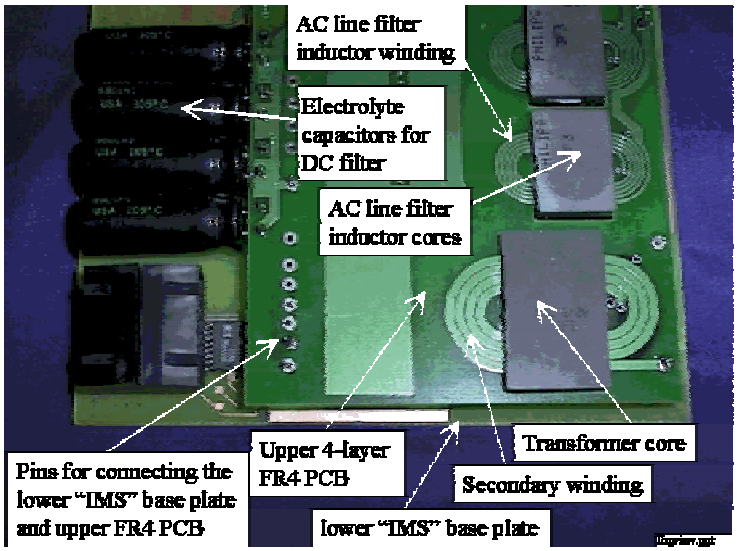


Fig. 49: Top view of the 1st generation prototype of the MIC (width 13cm, length 9.5cm).

13.2 Exterior packaging

Fig. 50 (a, b) shows the schematic of the exterior packaging concept of the MIC. Assembled MIC is covered with a plastic lid and encapsulated in epoxy. The use of encapsulation materials has a number of advantages. On the one hand encapsulation provides global protection from the surrounding environment: chemical (moisture etc.), thermal (temperature extremes) and mechanical (dust etc.). On the other hand the encapsulant can be used to improve thermal performance of the MIC. Packaging for outdoor application is often rated with IP65. That means all components in the exterior (potting lid, cables, grommets, connectors, adhesive) have to ensure total protection against dust and low-pressure water jets from all directions as stated in [9]. Adhesive material should have good adhesion to solder

mask of the IMS substrate and potting lid. Potting material should put very little or no thermo-mechanical stress on the internal electronic components and ensure uniform heat distribution in the bulk due to power losses in the components (eliminate hot spots). More detailed investigation on the use of potting materials for outdoor application is presented in [10].

The overall height of the MIC is 1.5 cm. To ensure better thermal behaviour, the MIC should be mounted with one side of the IMS to the aluminium frame of the solar module.

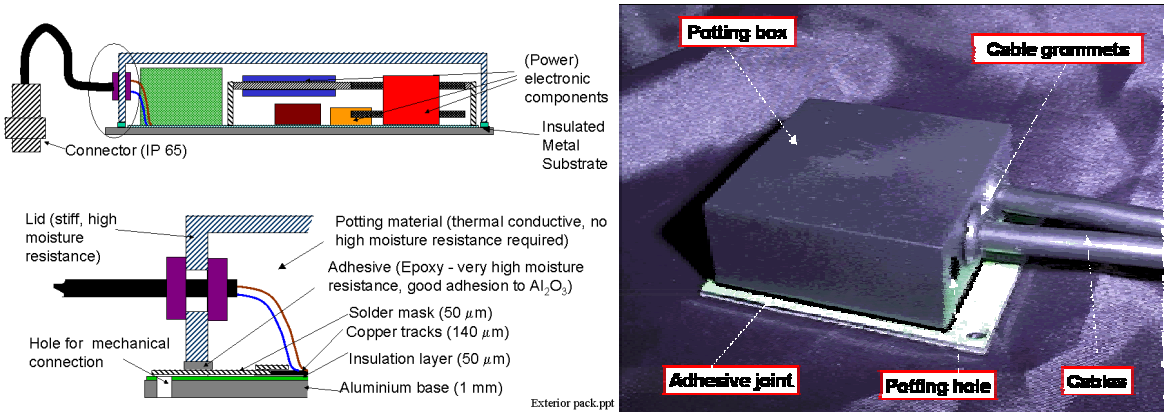


Fig. 50: Exterior packaging concept for the MIC.

14 Thermal simulation of the MIC

14.1 Motivation, assumptions

Recent investigations [7] have shown that the lifetime of a commercially available MIC is not sufficient for photovoltaic application. The crucial components in terms of the highest failure rate are the aluminium electrolytic capacitors of the DC-filter and the MOSFETs. The lifetime of electronic components is mainly determined by their temperature. Thermal simulations have been carried out to determine the influence of different design possibilities according to their impact on the resulting temperature of these crucial components.

Apart from these design possibilities, it is also possible to increase the lifetime of a MIC by reducing the converted power at very high ambient temperatures. This leads to lower losses, reduced temperature rise and thus to a higher lifetime of the MIC. For this purpose the internal temperature of the MIC has to be monitored.

Thermal analysis of solar module and MIC (modelled as a box) showed that the heat dissipated by convection and radiation is about 10% of the overall heat. Therefore all simulations described in the following are based on conductive heat transfer. The heat dissipation by convection and radiation is taken into account by assigning a constant heat flux value through the surface of the MIC. As thermal behaviour of the MIC is mainly conductive, the temperature inside the MIC has nearly linear dependency on the frame temperature. That means the frame temperature is only an offset value for the component's temperature.

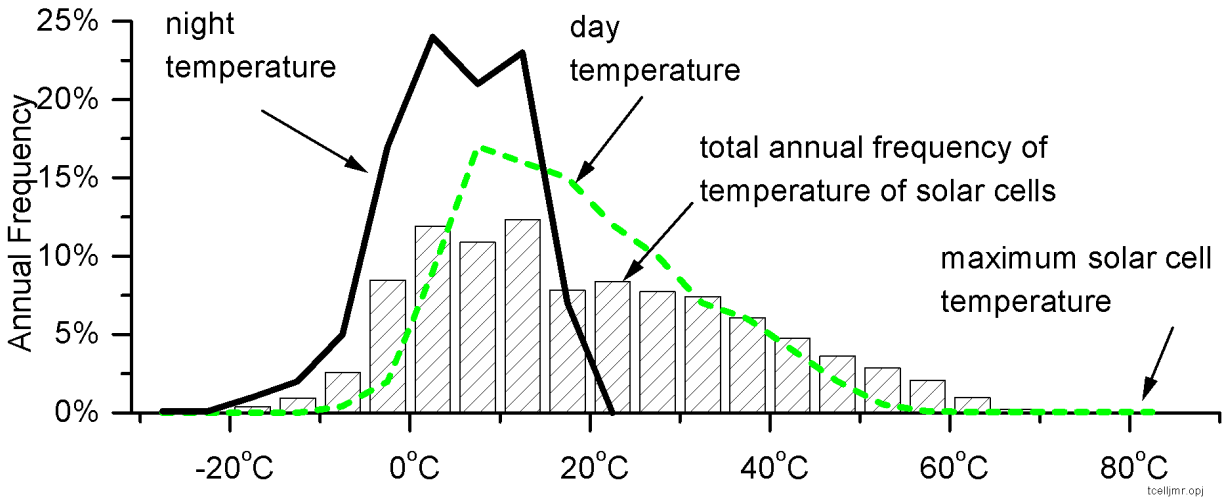


Fig. 51: Temperature frequency distribution of solar cells measured on the back of a solar module during one year of operation.

14.2 Thermal evaluation of a solar module

For the detailed simulation of the internal temperature of the MIC, a simplified thermal model of the solar module can be used. These investigations showed that the heat flux running from a MIC mounted to the frame of the solar module has a negligible effect on the frame's temperature. Therefore the frame of the solar module on which the MIC is mounted can be modelled by a heat sink with constant temperature. The temperature of the frame of the solar module depends on the method of mounting the solar module (e.g. thermal resistance of solar module stand or mounting structure). Since the efficiency of solar modules depends very much on the temperature of the solar cells, measurements presented in the literature always refer to the solar cells' temperature measured at the back of the solar module. Fig. 51 shows temperature frequency distribution for solar cells during one year of operation. This frequency distribution is based on measurements taken in Hanover and Munich published in [11] and [12]. Measurements of the frame temperature are not available. However, the frame temperature will always be lower than the solar cells' temperature. Therefore a maximum solar module frame temperature of 75°C is taken as a worst case estimation based on measurements presented in [13].

14.3 MIC modelling

The MIC is simulated with the thermal simulation program Flotherm by Flomerics. The model is based on the physical structure of the MIC described in section 3.1. The only components modelled on the IMS layer are those which produce significant heat as well as the constructive components which direct the heat flux (e.g. the pins). The drivers and measurement circuitry as well as the terminals have been neglected.

DC-filter capacitors

The most important part, the capacitors are modelled as shown in Fig. 52. Since the program Flotherm is not capable of modelling circular components, the capacitors are cuboid. Two resistive and one very conductive layer simulate that the capacitors

have a direct connection to the IMS only along one line. Modelling the inside of the capacitors is based on a cross-section of a real one. The aluminium case is covered with a plastic layer except one end. The surface of this square model is about 30% larger than the real capacitor. However, this has little impact due to the very low thermal conductivity of the plastic layer. The terminals of the capacitors have been neglected.

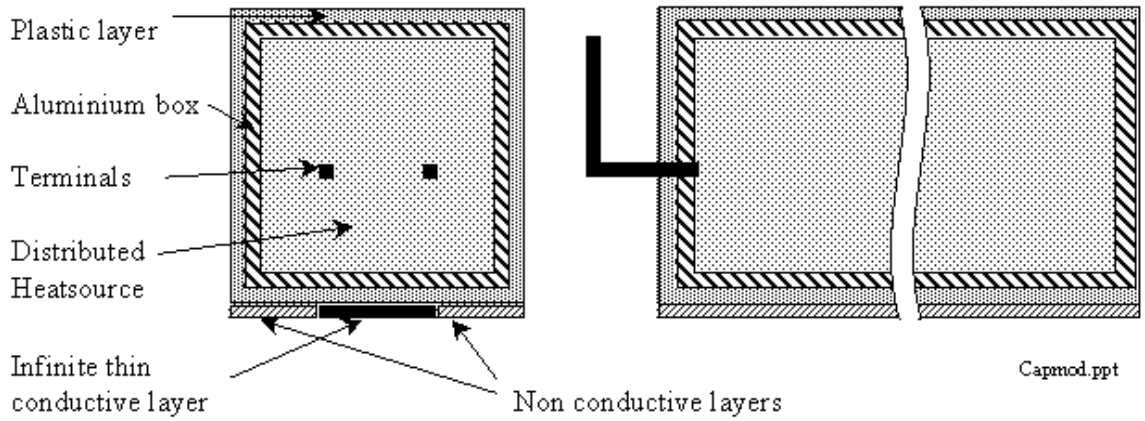


Fig. 52: Cross-sections of the capacitor model.

Lower IMS layer, MOSFETs and pins

The IMS is modelled as an aluminium block with a thin dielectric layer on top of it. The MOSFETs have the same overall size and, more importantly, the same thermal resistance between the junction and the case as in the data sheets. They produce the losses in the circuitry. The rows of pins are modelled as walls with an equivalent thermal conductivity.

Transformer

The transformer consists of an EE-core, primary and secondary windings. The core is modelled with five cuboid blocks. Each block produces the same heat per volume. The windings produce the heat equal to their copper losses.

Upper FR4 board, control unit and inductors

The FR4 Printed Circuit Board is thermally anisotropic and has an in-plane conductivity which depends on the number of layers and thickness of the copper tracks. This conductivity can be up to twenty times as high as the nominal conductivity. Therefore it is modelled as a cuboid block with the high in-plane conductivity and a resistive layer in the middle to reduce the normal conductivity.

The cores of the inductors on the top of the FR4 are modelled in the same way as the transformer. The inductor windings produce an amount of heat equal to the copper losses.

The control circuitry is a thin cuboid block, which produces the losses equally distributed over the area used by the control components.

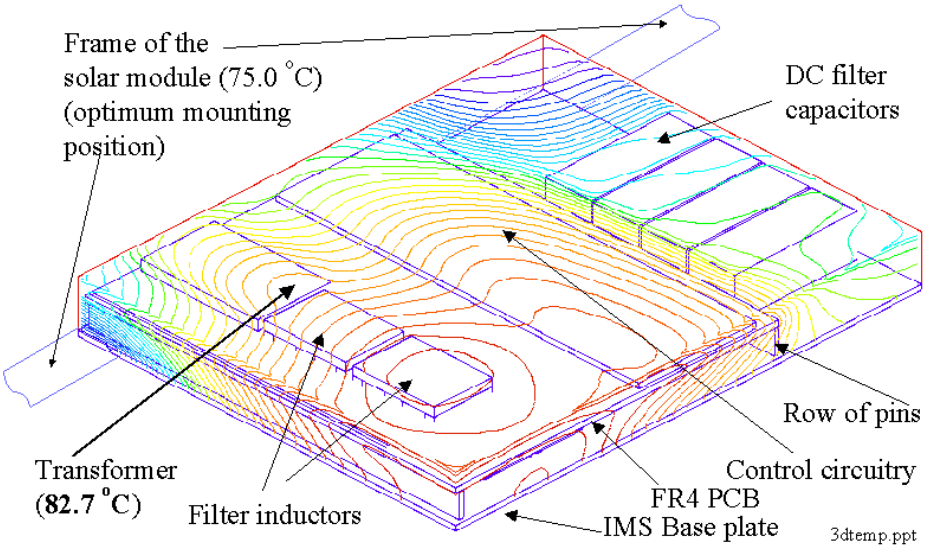


Fig. 53: Temperature distribution at the surface of the MIC.

14.4 Temperature of the optimised MIC design

In this section the results of the 3D simulation of an optimised packaging design (see section 3.1) for the MIC are presented. Fig. 53 shows the hot spot temperature distribution of the components crucial to reliability issue and control circuitry (including temperature sense). The MIC is assumed to be operating in rated mode i.e. temperature of the frame of solar module 75°C, DC-power 110 W, MIC efficiency 87%. The hot spot temperatures of the components are determined using 2D plots of temperature distribution (Fig. 54). It can be seen from the diagram in Fig. 55 that all reliability crucial components - especially the electrolytic DC capacitors - have a very small temperature rise (less than 11 K). For operation at rated power the temperature rise of the transformer is 7.5 K. The hottest spot of the entire MIC is the core of the AC inductor filters with a temperature rise of 12 K.

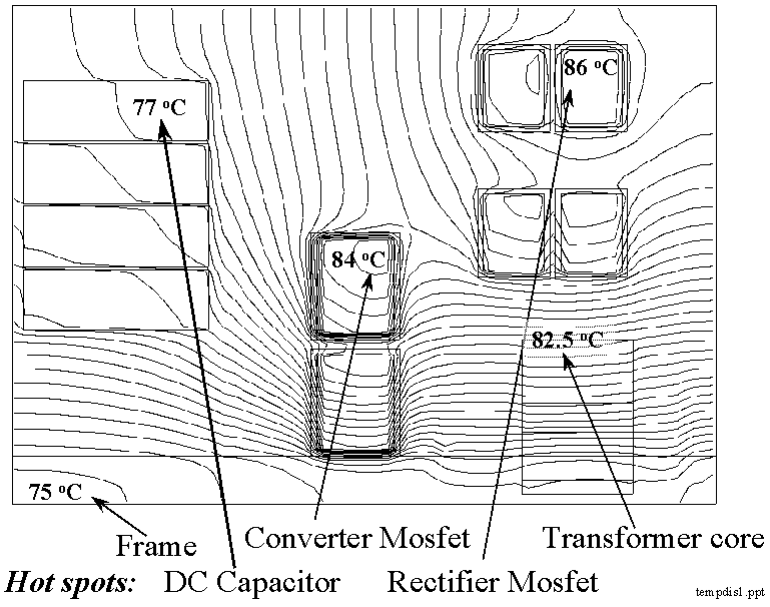


Fig. 54: Temperature distribution inside the MIC at the junction temperature of the MOSFETs.

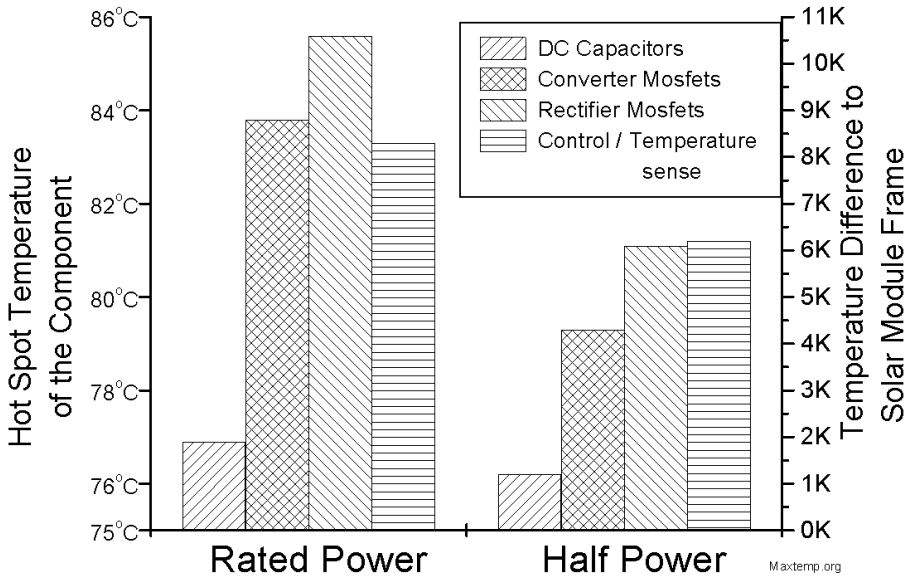


Fig. 55: Hot spot temperature of the components (T_{Frame} = 75°C) and temperature difference to solar module frame for operation at the rated power and half power.

14.5 Impact of the MIC design on the temperature of the components

To assess the improvements achieved by the optimised design of the MIC, a commercially available converter has been simulated as well. The model used is shown in

Fig. 56. The main differences between both designs are the increased height of the commercially available MIC (3 cm instead of 1.5 cm) and the application of a FR4 substrate (instead of IMS) for attaching the heat dissipating components (MOSFETs, transformer). All other parameters such as encapsulation material or orientation are the same as in the optimised design. The heat transfer through the commercial

converter box is very good due to the high thermal conductivity of aluminium. The problem occurs in the heat transfer from the MOSFETs through the FR4 to the box because of the very bad thermal path between FR4 and box resulting from the low thermal conductivity of FR4. According to **Fig. 57**, the components of the commercially available MIC show a temperature increase of 10 K to 20 K in relation to the optimised design. This corresponds to the temperature values that can be found in [14].

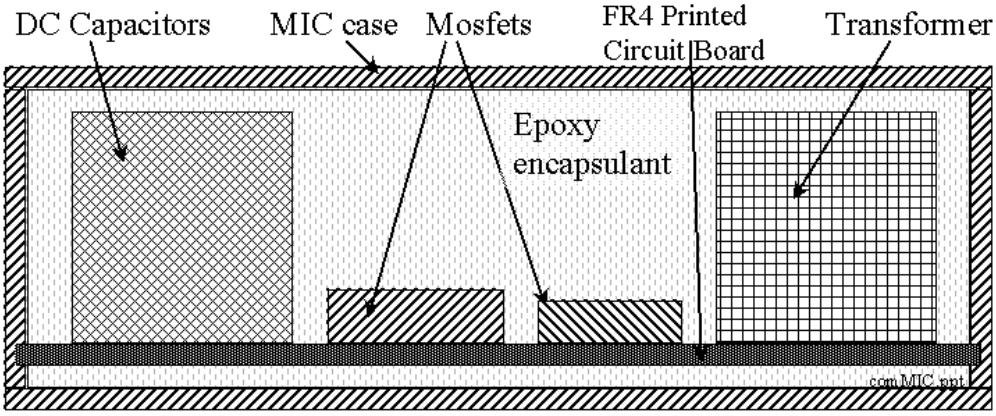


Fig. 56: MIC design based on a simplified structure of a commercially available MIC (with FR4 base plate).

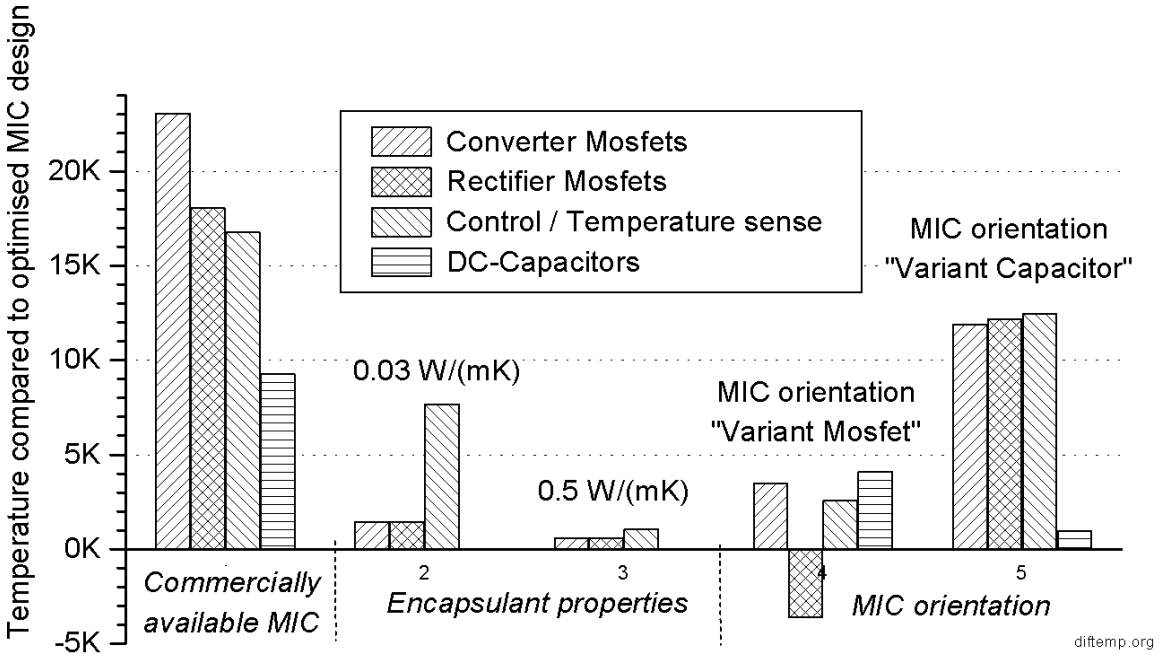


Fig. 57: Impact of different design features on the component temperature in relation to the optimised design.

14.6 Encapsulation materials

The optimised design employs a very good thermal conductive epoxy encapsulant with a thermal conductivity of 1 W/(m K) to achieve a good heat transfer between FR4 and IMS which leads to a low temperature of the control circuitry on the FR4. Encapsulation materials with a good moisture resistance usually have a lower thermal conductivity (down to 0.03 W/(m K)). For that case where the final design of the MIC demands a moisture resistant encapsulant, the results in **Fig. 57** show that the impact on the crucial components is marginal if epoxy with a thermal resistance of 0.5 W/(m K) is used.

14.7 Impact of mounting position of the MIC on the component temperature

Apart from the design of the MIC, the mounting position on the solar module has a large impact on the internal temperature of the MIC. **Fig. 58** shows the optimum position for mounting the MIC on the frame of the solar module and two alternative possibilities ("Variant Capacitor" and "Variant MOSFET").

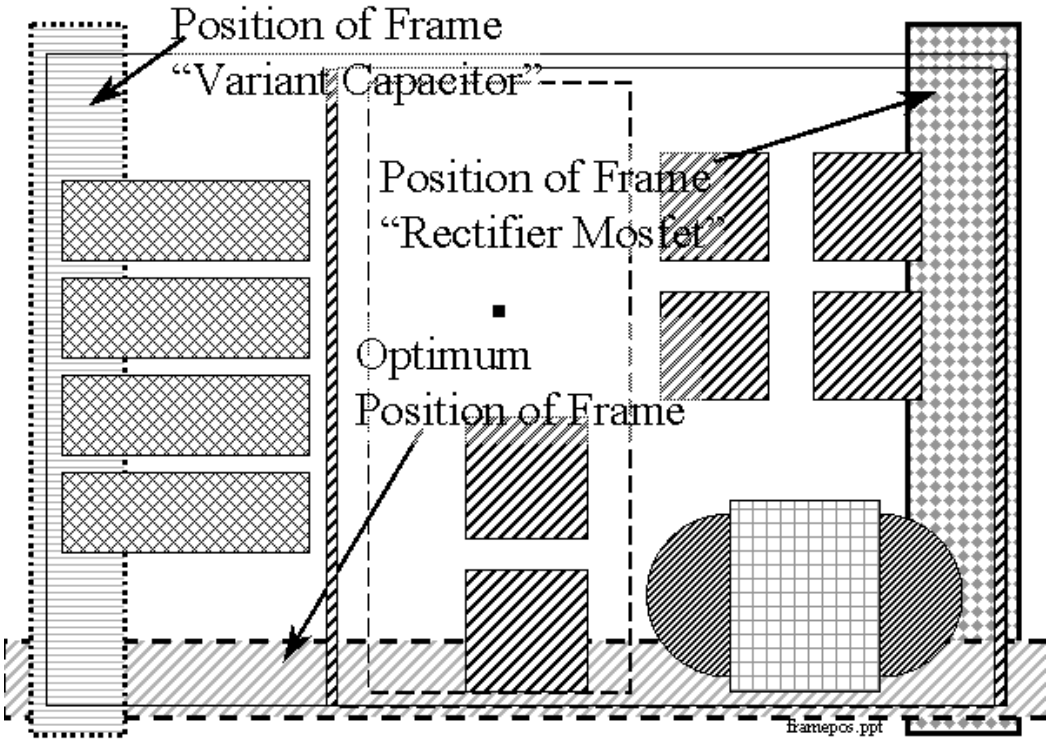


Fig. 58: Different frame positions for MIC mounting.

If the MIC is mounted to the frame in the "Variant Capacitor" position the DC-capacitors are very close to the frame, which operates as a heat sink. But the results of the thermal simulation illustrated in Fig. 57 show that for mounting position "Variant Capacitor" the DC-capacitors are hotter compared to the optimum position. The reason for that is the heat flux running from the MOSFETs towards the frame of the solar module.

Simulation results in Fig. 57 show a decreased temperature of the rectifier MOSFETs, if the MIC is mounted to the frame in the "Variant MOSFET" position,

where the rectifier MOSFETs are very close to the frame. On the other hand the temperature of the DC capacitors is increased due to the larger thermal resistance.

The optimum position of the MIC on the frame is such that the MOSFETs and the DC capacitors are thermally in parallel. In this case capacitors are very close to the frame and the heat flux from the transformer, inductors and MOSFETs does not flow through the capacitors.

15 Reliability

This section gives an overview on the effects and factors that have an influence on the lifetime of the MIC.

15.1 Status of reliability of the MIC

Recent technology and design is already capable of guaranteeing the lifetime of solar modules for 15-20 years of continuous operation. Being a part of the whole PV system, the MIC should have similar lifetime. The reasons are quite obvious. In order to maximise the energy yield of the whole PV system all parts should be equally reliable. Economical and environmental aspects play a very important role in it, for the production company as well as for the user. Manufacturers must guarantee a minimum lifetime of 15 years for the MIC to win market share and reputation. Unfortunately, they state just *expected* values so far. Calculations based on statistical models (i.e. handbook [15]) represent just a very rough theoretical value. Some calculations based on accelerated lifetime tests cover particular aspects like high temperature and humidity. The electronic components of the MIC are exposed to extreme environmental conditions. High thermo-mechanical stress has a very large impact on the lifetime of the MIC. But this is only one aspect of reliability. In practice, there are many more factors that have a complex impact on the lifetime of the MIC. The final demonstrated values are only half of those calculated (8 years). This shows that the reliability issues should be treated seriously today. Only *demonstrated lifetime* is of value. It is still a major challenge for the design of the MIC.

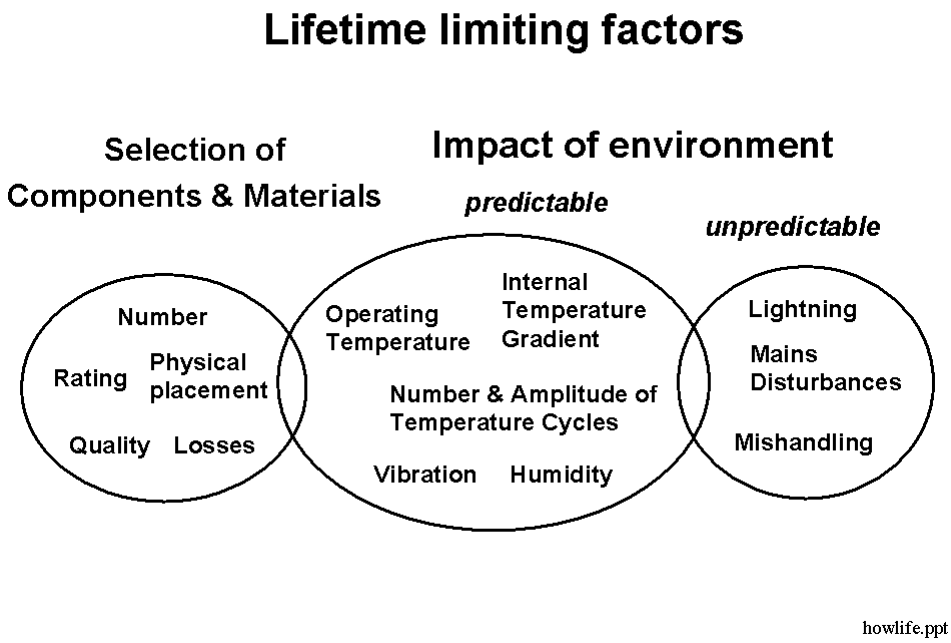


Fig. 59: MIC lifetime limiting factors.

15.2 Lifetime limiting factors

In general the lifetime of a MIC is limited by a number of factors (Fig. 59). The failures can be categorised into design related failures and those which are triggered by operational conditions (environmental impact). In most cases failures are caused by a combination of both factors. Design related factors are: selection of components and materials, number, rating and physical placement of components. Failures related to operational conditions of the MIC are either of deterministic or unpredictable nature. The maximum absolute temperature, the number and amplitude of temperature cycles as well as humidity are very much predictable. Whereas the electrical disturbances coming from the mains or in the case of lightning strikes on the solar module are less predictable since they are caused by the weather or other stochastic events in the electric grid (e.g. failures in other appliances connected to the same grid).

15.3 Consequences of the design

The main motivation for the detailed thermal simulation was to find a MIC design optimised for improved reliability. The failure rate has been calculated based on the procedure described in Military Handbook 217E [15]. The results presented in Fig. 60 are rated to the failure rate of the optimised design. For the comparison of the failure rates of different designs the same converter topology was considered (see fig. 46). According to Fig. 60, the MIC with optimised design shows the minimum failure rate with the lifetime approx. 70% longer than for the design similar to a commercial product. In all cases the DC electrolytic capacitors cause more than 50 % of all MIC failures.

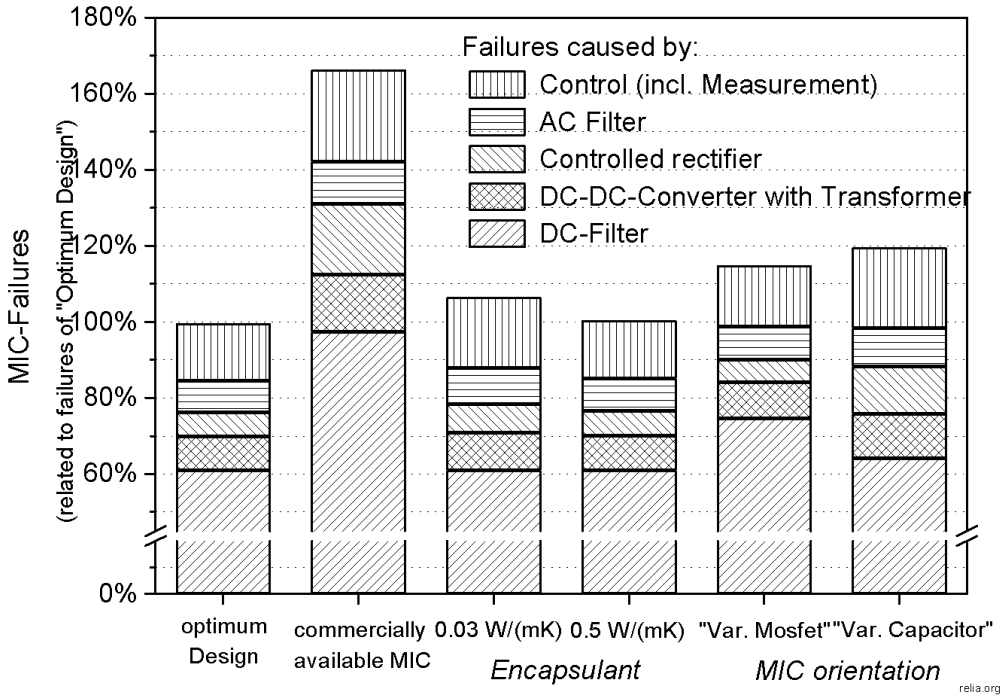


Fig. 60: Impact of different design features on the failure rate of the MIC (failure rate of MIC with “optimised design”: 35.7 failures/10^6 h operation time).

15.4 Methods to increase the lifetime of aluminium electrolytic capacitors

The lifetime of aluminium electrolytic capacitors is influenced mainly by these 3 parameters:

- Internal temperature (hot spot temperature) of the capacitor;
- Voltage stress (ratio of applied voltage to rated voltage);
- Current stress (ratio of applied ripple current to rated ripple current).

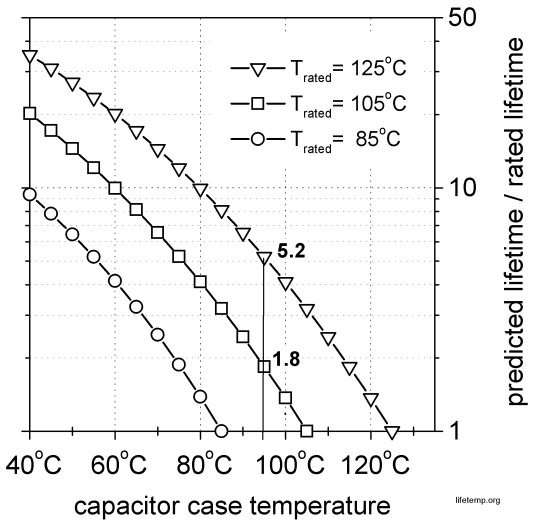
The impact of temperature and voltage stress on the lifetime of aluminium electrolytic capacitors is illustrated in Fig. 61 a -b.

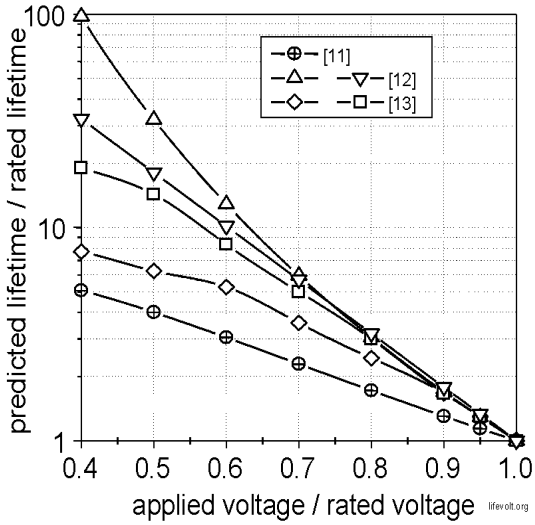
The *internal temperature* of aluminium electrolytic capacitors is the main factor which has the biggest influence on their lifetime. Therefore the lifetime can be increased by reducing the operating temperature (case temperature) or using capacitors with higher rated temperature. As shown in Fig. 61 a, the lifetime of the DC-filter operating at 95°C can be increased by a factor of 3 if a 125°C capacitor is used instead of a 105°C capacitor. But the size of the DC-filter would then be doubled (increased cost).

The *voltage stress* (Fig. 61 b) of the capacitors also has a big influence on their lifetime. According to the publications [15], [16] and [17], lifetime can be increased by a factor of 4 to 30 by limiting the capacitor’s voltage stress to 0.5.

Reduction of the *current stress* increases lifetime up to 25 % [12] because of lower internal losses and lower hot spot temperature of the capacitors.

The disadvantage of all three possibilities is that they lead to higher costs and increased size of the DC-filter and the whole MIC. The best way to extend the lifetime is achieved by decreasing the internal temperature using a proper thermal design.





a) b)

Fig. 61: Influence of temperature and voltage stress on the lifetime of aluminium electrolytic capacitors.

16 Conclusions and further work

The presented “Low Profile Design” of a Module Integrated Converter (MIC) for Photovoltaic applications has double the power density compared to commercially available MIC. Encapsulation materials have positive impact on the thermal behaviour of the MIC as well as the whole concept of the exterior packaging. The internal temperature of aluminium electrolytic capacitors is the main factor which influences their lifetime and the lifetime of the whole MIC. The design of a MIC was optimised according to reliability issues. This was achieved by a detailed 3D thermal simulation of the MIC and the solar module.

Future investigations will compare the simulation results with measurements of the MIC’s internal temperature. Further steps will be taken to miniaturise the magnetic components. The different design possibilities presented in the paper will be compared according to cost and manufacturability issues. The influence of encapsulation materials on the reliability of the MIC will also be investigated.

17 Magnetic components for the Module Integrated Converter

17.1 Introduction

One of the tasks of the NMRC in HICAAP was the design and test of the magnetic components of the module integrated converter. The topology of the MIC's power train developed by ISET included the following components: Transformer, Resonant Inductor, Current sense, DC Inductor, AC Inductor, Common Mode Inductor.

The investigations on reliability of the MIC [H] showed a substantial reduction of the failure rate (and therefore increase of lifetime) if a "Low Profile" design is chosen for the MIC. Consequently "Low Profile" or Planar Magnetic Components would have to be used. These planar magnetics are commonly used in conventional power supplies. They offer the possibility to integrate the windings of the magnetic components into a multi-layer Printed Circuits Board (PCB) which is anyway necessary for high density interconnection of the components of the control circuitry.

Usually the performance of the planar magnetics with PCB integrated windings in relation to conventional wire wound parts improves with increasing operation frequency. The operation frequency of the MIC at the moment is only 250 kHz, which is relatively low compared to commercial power supplies in that power range (300 kHz – 600 kHz). Therefore the performance of the components designed by the NMRC might be worse than the comparable wire wound parts.

However following the common trend towards of reduction in size of power supplies one major pillar in order to achieve the intended miniaturisation and integration of Module Integrated Converters is an increase of switching frequency. According to the results of a study [A.] initiated by the Power Sources Manufacturers Association and carried out by PEI Technologies, Ireland surprisingly an increase in switching frequency has been observed to lead to increased efficiency of the power supplies.

The next section deals with the design of discrete realisations of Transformer and Resonant inductor. Following a new method of an integrated of inductor/transformer patented by the NMRC [B] is presented and compared with the properties of the discrete realisation. The final chapter deals with realisation of functional integration of inductor, transformer and current sense, which is being investigated at the moment (Summer 1999) by the PEI Technologies group of the NMRC, Ireland.

17.2 Design of discrete inductor and transformer

In the resonant converter specification, there are two magnetic components required – a 500 nH series inductor, and a 1:17 step-up transformer. Specifications for the transformer are given in table 4.

Table 4: Transformer specifications for the converter design

P_{out}	220W
V_{pri} (pk)	17V
I_{sec} (rms)	1.1 A
V_{sec} (rms)	200 V
f	250kHz

The transformer can be realised in a planar construction using an EE38 core (3F3 material from Philips Components [C]) with 1 primary turn and 17 secondary turns. The 17 secondary turns are constructed from a 4 layer PCB with the single primary turn constructed on a separate single layer PCB. The construction of the primary and secondary windings on separate PCBs allows the use of a thick copper layer to carry the high primary current. This construction also allows the leakage inductance of the transformer to be adjusted by varying the separation between the windings. However the maximum leakage inductance which can be achieved from this transformer realisation is approximately 90 nH obtained with the maximum separation between primary and secondary PCBs. Thus, is this case the required 500 nH series inductance must be achieved by using a separate discrete inductor. This inductor can be realised by using a single turn planar E22 core with a gap of 280 μm to achieve an extra 410nH inductance (again using 3F3 ferrite material from Philips Components) in series with the primary winding of the transformer. Fig. 62 shows a picture of the final discrete inductor and transformer design.

The following section investigates the realisation of this transformer and series inductor in a single integrated component introduced in [B].

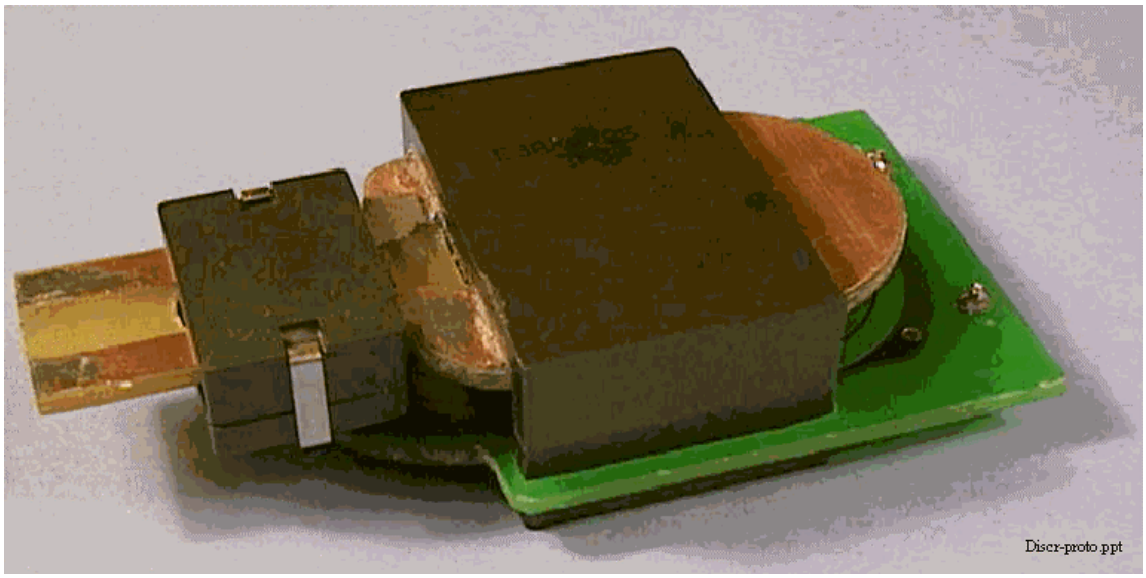


Figure 62: Picture of the discrete and integrated inductor and transformer design.

17.3 Integrated inductor-transformer realisation

For the transformer design described above, a reluctance model presented in [D] is applied to predict the properties of magnetic short layer required to produce a leakage inductance of 500nH in an EE38 core. Results are presented in fig. 63 for three different short materials, with permeability values of 25, 80 and 140. Short thickness values of up to 4 mm are considered, and corresponding values of magnetising inductance are also presented.

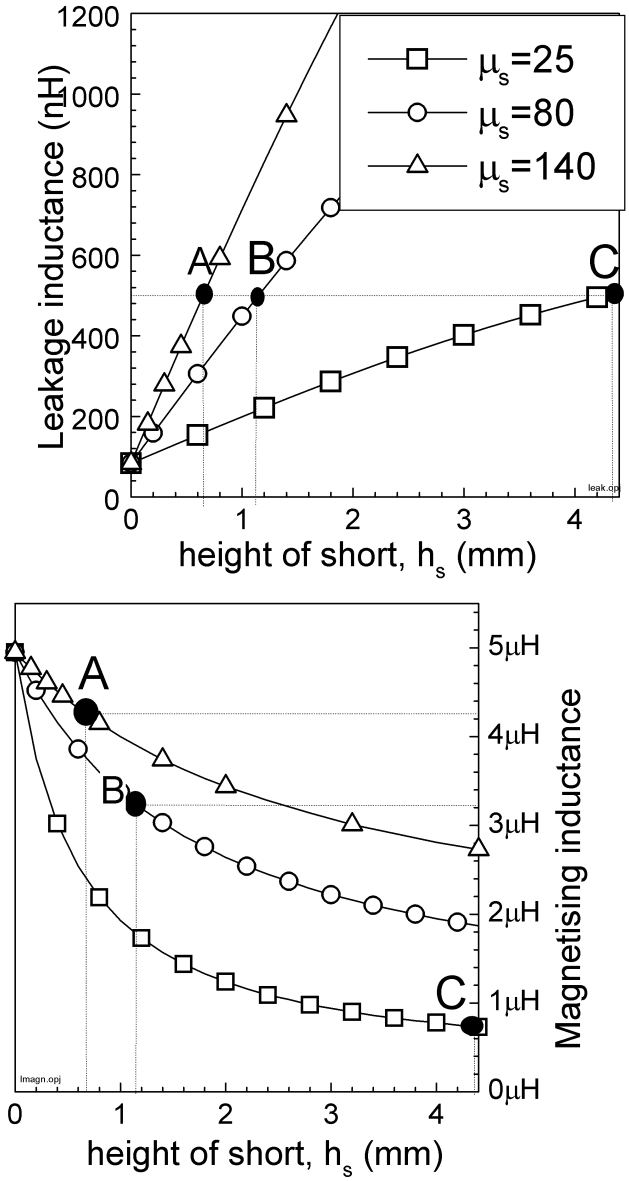


Fig. 63: Leakage and magnetising inductance of EE38 core for different magnetic short designs

For each material, it is seen that a different thickness of magnetic short is required to provide the required level of leakage inductance. As before, leakage is shown to depend on the product of μ_s h_s [E]. Therefore, while 4.3 mm thickness of material with μ_s=25 provides a leakage of 500nH in design A, only 0.6 mm of material with

μ_s=140 is required to produce the same value for design C. However, while the three short designs, have the same value of leakage inductance, very different values of magnetising inductance are produced. The curves in Fig. 63 correspond to magnetic short materials with relative permeability values of 25, 80 and 140. These correspond to the ferrite materials listed table 5 below, which are supplied by Philips Components for a range of standard core shapes [C].

Table 5 Magnetic properties of ferrite short materials

Material	Permeability, μ_s	B_{sat} (mT)
4E2	25	300
4F1	80	320
4M2	140	300

The materials are intended for used in high power applications. For the purposes of this work, customised slabs of each of the materials were obtained for use as magnetic shorts in the new integrated inductor-transformer structure. The thickness of the slabs is 1 mm in all cases. With these restrictions on permeability and thickness the closest to the 500 nH leakage inductance can be achieved in the new integrated inductor-transformer design using the 4F1 material. Thus the integrated inductor-transformer consists of a planar EE38 core (the same as for the discrete transformer) with a 1 mm thick slab of 4F1 material inserted between the two core halves. For this particular construction the open circuit ($L_{oc} = L_m + L_{lp}$) and leakage inductance ($L_l = L_{lp} + L_{ls}$) predicted by the reluctance model is compared to measured values in Table 6.

Table 6: Comparison of modelled and measured inductance values for the integrated component (Version B).

	Model	Measured
L_{oc}	3.9 μH	4.2 μH
L_l	460 nH	500 nH

The measured results and those predicted by the reluctance model agree very well. The differences are due to the difficulty in predicting the inherent air gap which occurs at the core faces due to the surface roughness of the core. This gap is accounted for in the reluctance model but the value used can be adjusted to fit the measurements. In the following section the performance of this component is compared to the discrete inductor and transformer. In some cases results for a magnetic short of 4E2 (μ_s=25) and 4M2 (μ_s=140) material are included for comparison.

17.4 Comparison of discrete and integrated components

17.4.1 Size

The main aim in integrating an inductor and transformer in one structure is to reduce the overall size of the magnetic components. As shown in Figure 64 the footprint of the integrated device is smaller than the discrete device, due to the elimination of the area required for the discrete inductor winding and core. In the application considered here this reduction in footprint area is approximately 20%. The height of the integrated device is larger than the discrete transformer by an amount which equals the height of the magnetic shorting layer; i.e. the integrated part is higher only by 1 mm in this case. By using the integrated approach the overall volume of the inductor-transformer combination is reduced by an amount approximately equal to the difference in volume between discrete inductor core volume and the volume of the magnetic short. In the case of the application considered here, this reduction in volume is approximately 8%.

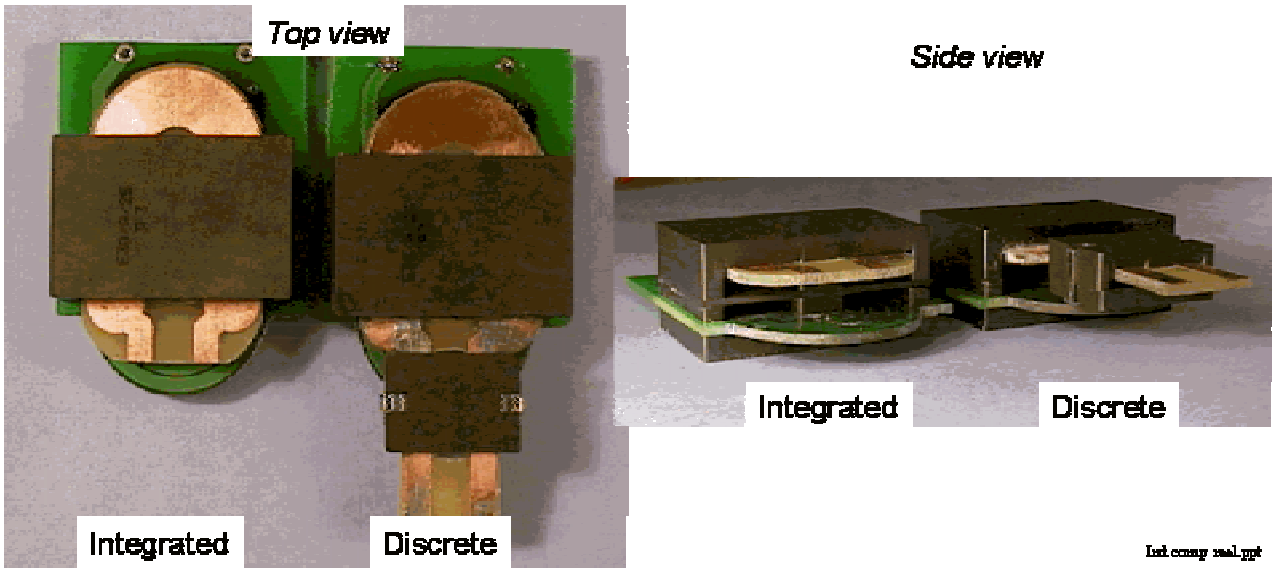


Figure 64: Picture of the discrete and integrated inductor and transformer design.

17.4.2 Circuit response

The performance of the integrated inductor-transformer may be investigated in terms of the simplified circuit model shown in Figure 65. The corresponding model for the discrete realisation is shown below in Figure 65 Both models are applied to investigate the impact of the load impedance on the circuit response for a given applied voltage (V_{in} = 19.5V). For the case of the discrete realisation, components of L_l and L_m for the transformer are given in previous section, while the inductor is assigned with a constant 410 nH.

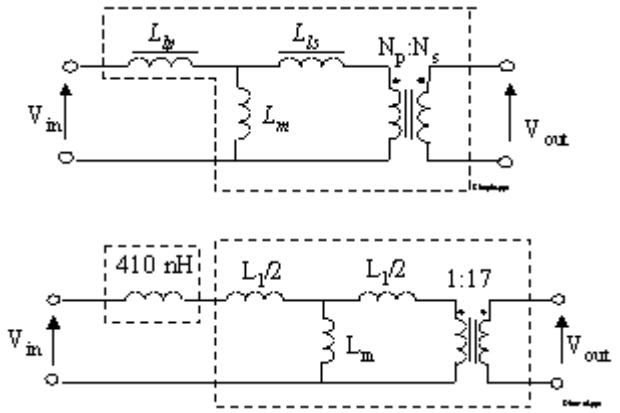


Figure 65: Simplified circuit model of integrated and discrete realisation of inductor and transformer

For comparison with the integrated device, the voltage ratio is given in terms of input voltage, V_{in}, applied to the series connection of inductor and transformer. Components of L_l and L_m for the integrated device are marked in the graphs of Fig. 63 for the different materials. Results of V_{out}/V_{in} are compared in Figure 66 below for a range of load impedance values. An operation frequency and a load power factor of 1.0 are assumed in all cases.

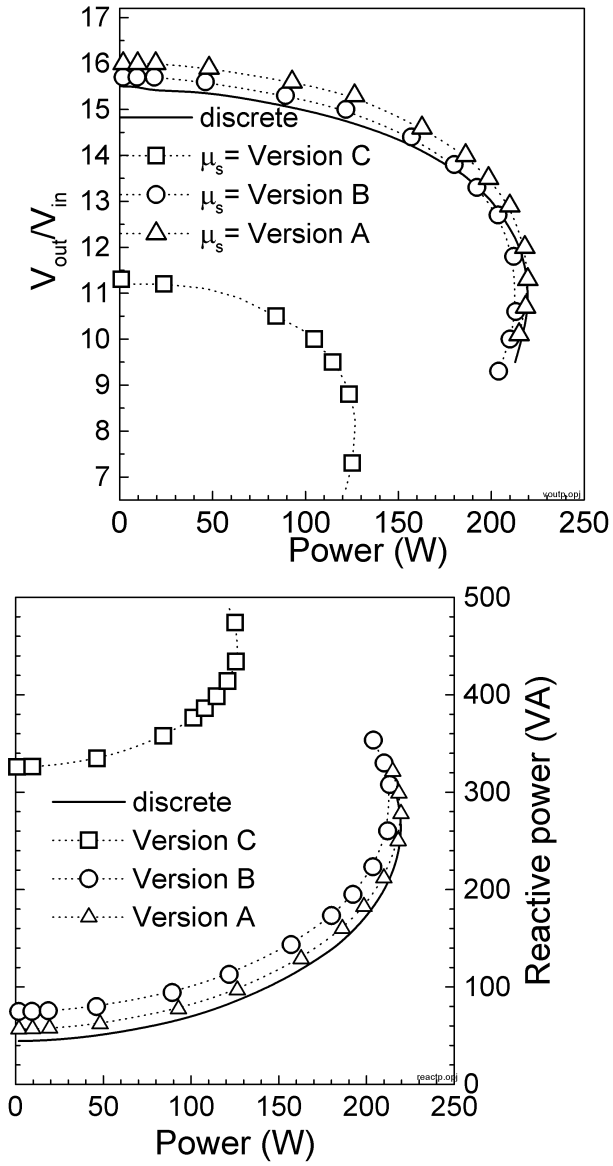


Figure 66: Comparison of V_{out}/V_{in} and reactive power for discrete and integrated inductor-transformer combinations

As shown, for short design A (material 4M2, μ_s=140, h_s = 0.65 mm) and B (material 4F1, μ_s=80, h_s = 1.1 mm), the circuit response matches that predicted for the discrete inductor and transformer combination. However, for the case of design C (material 4E2, μ_s=25, h_s = 4.35 mm), the voltage transformation ratio is greatly reduced from the discrete solution. This is caused by the reduced magnetising inductance of the transformer, as shown in the results of Fig. 63. For the same reason, the reactive power required by the integrated structure is much larger for material 4E2 than for materials 4F1 and 4M2 - also shown in Figure 66.

17.4.3 Flux density levels

Another consideration with this design is that the magnetic short does not saturate when the transformer is loaded. The plot of the magnetic flux density in the shorting layers as a function of power levels are given in Figure 67.

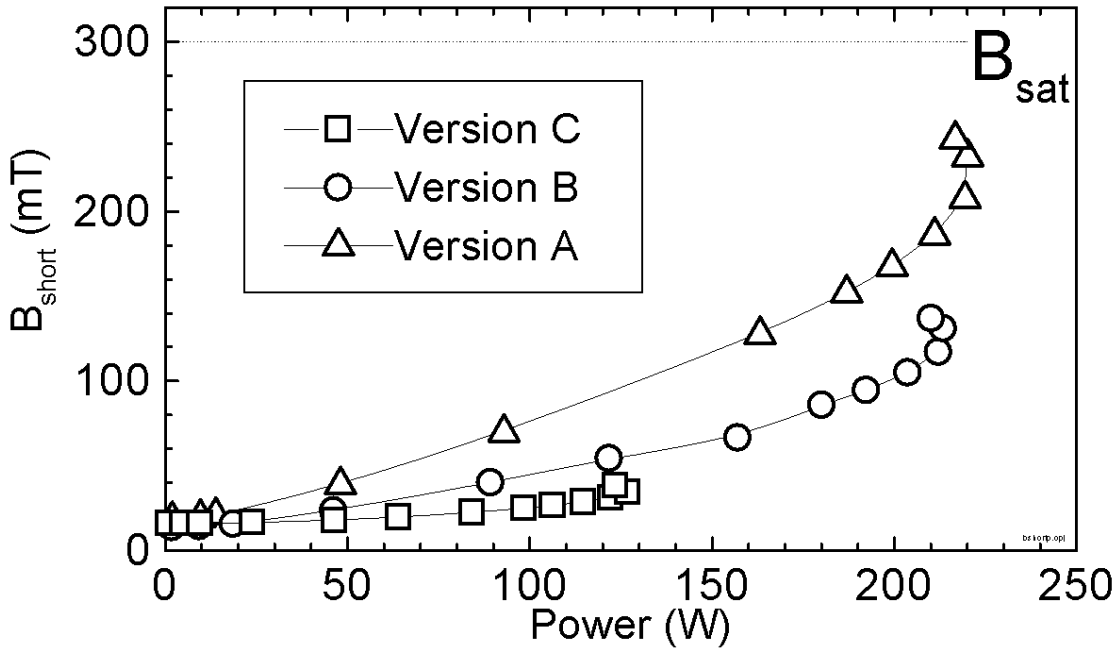


Figure 67: Magnetic flux density for different short designs as a function of output power at unity power factor.

The largest levels of magnetic flux density are predicted for case A, the short using material 4M2, which has the largest value of magnetic permeability and the smallest thickness. As the output power increases, the flux density tends towards the saturation flux density for a typical ferrite material, but remains below saturation for all loads with unity power factor. The operation of the transformer under other load conditions is investigated in more detail below. Corresponding losses in the shorting material are also compared later.

In a resonant converter topology, the output power is controlled by varying either the input voltage level or the power factor of the load. This is achieved by varying the duty cycle or the switching frequency of the converter [F]. Here the effect of varying load power factor on the magnetic flux density of the shorting layer is investigated for a rated output power of 220 W. Results are presented in Figure 68 for flux levels in the magnetic short and in the EE38 core for a variation between ±0.6 ($\phi = \pm 53.1^{o}$) of the load power factor.

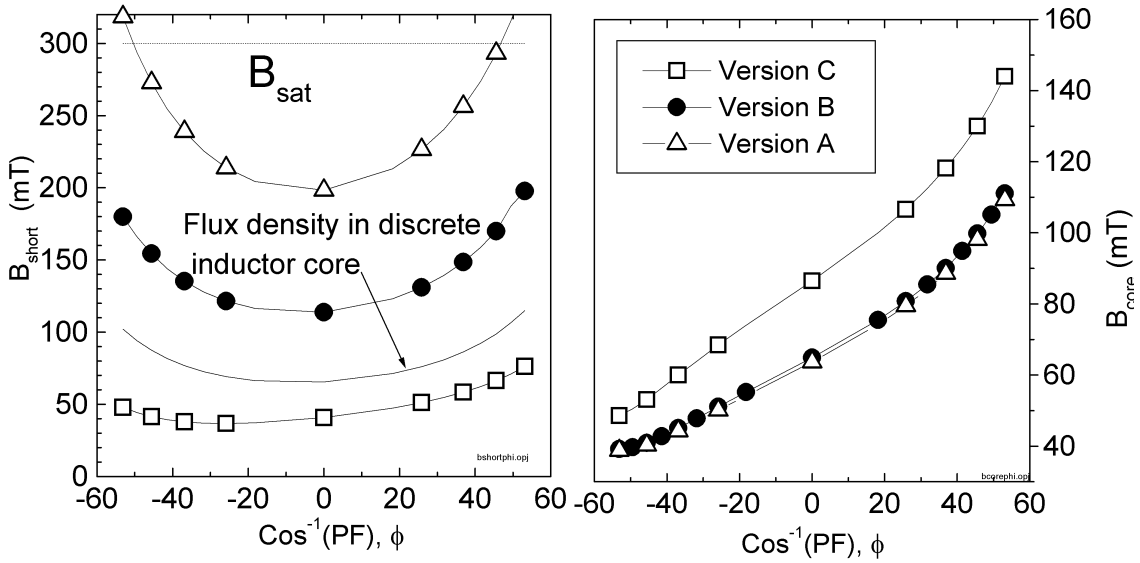


Figure 68: Magnetic flux density levels in (a) magnetic shorting layer and (b) transformer core versus load power factor

In this case, the resistive load of the transformer is constant, and the input voltage is varied to provide a transmitted power of 220 W for different values of load power factor. Values for the flux density level in the discrete inductor core is also included in the graph for comparison.

For the shorting layer the flux levels are larger than those which would occur in the discrete inductor core for all designs except for case A. For this design (material 4M2, μ_s = 140, h_s = 0.65 mm), the shorting layer is driven into saturation for the extreme load power factors of ±0.6.

The flux density levels in the transformer core are below the saturation value over the entire range however the important consideration here is the impact of the increasing flux density on core loss in the transformer. This is computed later for the case of unity power factor.

17.4.4 Losses

In this section the losses for both the discrete component and the integrated component are compared for the rated operating conditions, i.e. 220 W power output (unity power factor) and an input voltage (V_{in}) of 20 V, and a switching frequency of 250 kHz. The losses consist of the two components – winding loss and core loss.

The winding loss at 250 kHz is determined from a 2D Finite Element Analysis (FEA)[G]. Simulations are performed for both the discrete inductor and transformer and the integrated inductor-transformer.

The core loss (P_{core}) is calculated from the commonly used core loss equation,

$$P_{core} = V K f^{\alpha} B_m^{\beta} \quad (4)$$

where V is the effective volume of the core, f the frequency, B_m the peak flux density in the core and K, α and β are the core loss coefficients given by the

manufacturer for the particular material. The peak flux density in the core, B_m, may be taken directly from the curves in Figure 67 and Figure 68, i.e. the reluctance model may also be used to predict core losses. However as a further check on the validity of the reluctance model the flux density has also been determined from 2D FEA of the integrated inductor-transformer geometry. The comparison of the flux levels predicted by the reluctance model and those determined from the FEA are given in Table 7.

Table 7: Comparison of the peak flux density levels predicted by the reluctance model and determined from FEA.

	Reluctance Model	FEA
B_{core}	120 mT	113 mT
B_{short}	65 mT	68 mT

As can be seen the values agree very closely and further verify the accuracy of the reluctance model. The bar chart in Figure 69 compares the losses in the discrete inductor and transformer to those in the integrated component. (for the integrated component the inductor core refers to the magnetic short).

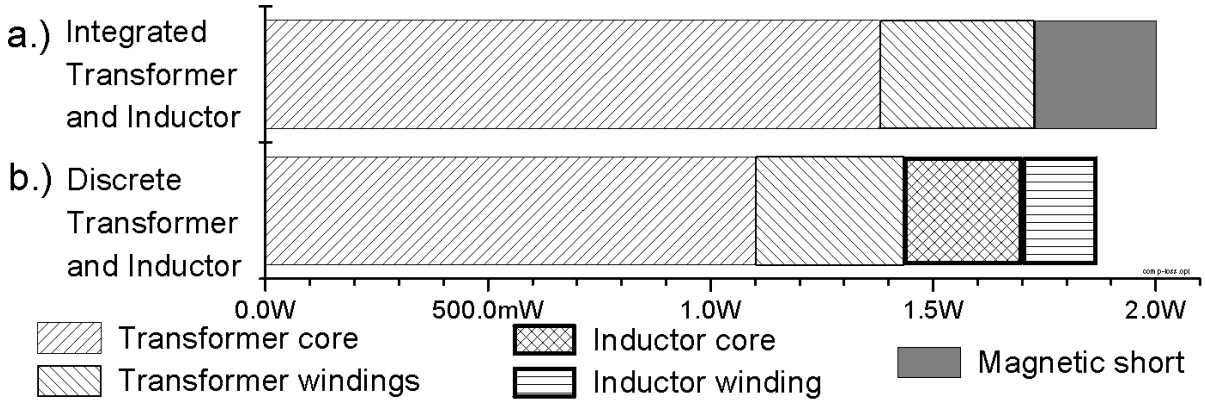


Figure 69: Comparison of the losses for 220W load, PF=1, for the discrete realisation and the integrated component (design B).

The winding loss for the integrated solution is less than that for the discrete solution due to the elimination of the discrete inductor winding. However this reduction is winding loss is offset by an increase in the core loss for the discrete realisation. Overall the total losses for the integrated component have increased by approximately 7%. This increase in core loss is due to two factors; - extra losses incurred in the transformer core and the loss in the magnetic short.

The extra loss in the transformer core is due to a slight increase in the core flux density. This is caused by the increased magnetising current which is required because of the reduced magnetising inductance as predicted by the results in Fig.

63. The increase in flux density is approximately 8% however it is sufficient to cause an increase in transformer core loss of approximately 25%. In general there will always be a slight increase in the transformer core loss due to the reduced magnetising inductance.

As can be seen from the bar chart the loss incurred in the magnetic short is approximately equal to the loss incurred in the discrete inductor core. In order to calculate the losses in the magnetic short the loss coefficients for the 3F3 material was used as the losses for the actual short material 4F1 were not available at 250kHz. In general the losses in the magnetic short will depend very much on the value of leakage inductance required, and on the material used for the magnetic short. Ideally the material used in the magnetic short should have loss characteristics optimised for the required operating conditions.

17.5 Conclusions

A new method has been presented for the integration of a series resonant inductance and transformer into a single component. The main motivation for the use of the integrated component is to achieve a reduction in component size by the elimination of the discrete resonant inductance. For the particular application presented the integrated component achieves a reduction in footprint area of 20% and a reduction in volume of approximately 8%.

The detailed comparison between this new integrated component and the discrete realisation of inductor and transformer shows that in terms of circuit performance, the integrated component is very similar to that of the discrete realisation. The analysis of the losses in both components shows that although the losses associated with the discrete inductor are eliminated by the new approach, this reduction is offset by extra transformer core losses which are generated in the integrated device. In this particular application total losses were increased by approximately 7%. However in general it cannot be concluded that losses are increased by using the integrated component; - the relative increase or decrease in losses will be application specific. It is also worth noting that losses in the shorting material could probably be reduced if a wider range of suitable short materials, which were optimised for the application were available.

17.6 Future work - Functional integration of Inductor, Transformer and Current Sense

For the control of a resonant converter very often a current sense sensing the current of the resonant circuit is used. For these purposes current transformers or low inductive current shunts are commonly used. Drawbacks of both possibilities are the losses associated with sensing the current, size of current sense and additional costs.

Figure 70 shows a possible realisation of three discrete components using planar magnetics.

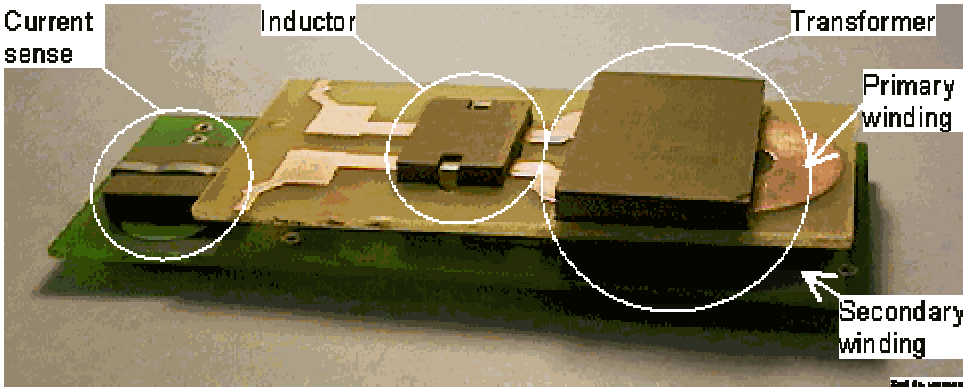


Figure 70: Prototypes of a “Low Profile” discrete Inductor, Transformer and Current Sense (with windings integrated into PCB)

As shown in Figure 67 the flux in the magnetic short placed between the E-cores of the transformer in order to increase the leakage inductance of the transformer is nearly proportional to the load current. This fact can be utilised in order to create a “lossless” current sense [B] by winding turns around the mentioned magnetic short as shown in Figure 71 in order to create a sense winding. The possibilities of this very promising structure are being evaluated at the moment by the Magnetics Group of PEI Technologies, Ireland. Figure 72 shows the picture of a first prototype of a fully functionally integrated component.

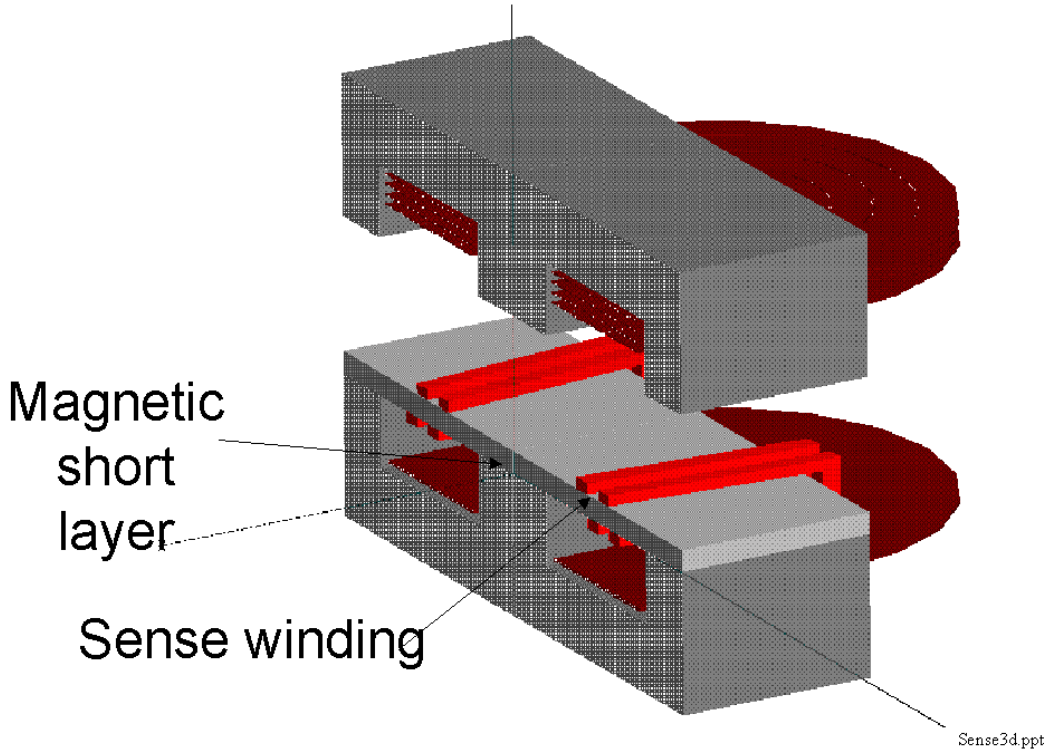


Figure 71: Principle of an integrated Inductor, Transformer and Current Sense.

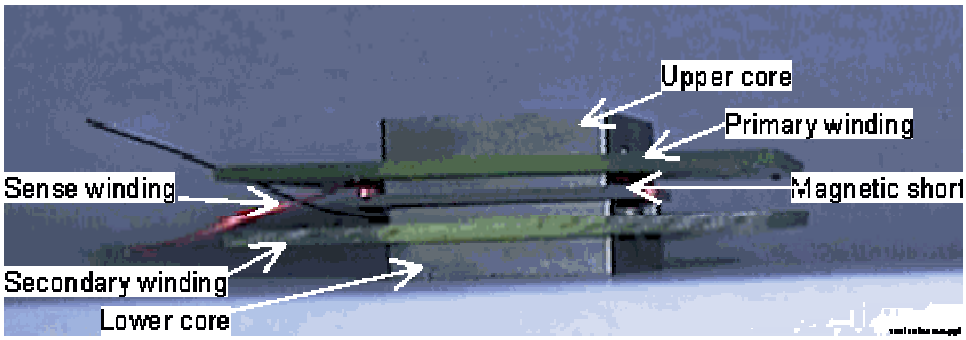


Figure 72: Prototype of a “Low Profile” integrated Inductor, Transformer and Current Sense

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