European
manufacturing platform
for Photonic Integrated Circuits

Deliverable Report (WP7, D7.11)

Final Publishable Summary Report

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Table of abbreviations

The material InGaAlAs.	Al(Q)
Application Programmers interface	API
Application specific PIC	ASPIC
Arrayed Waveguide Grating	AWG
Building Block	BB
CMOS	Complementary Metal-Oxide-Semiconductor
Composite or Circuit building block	CBB
Multi-mode interference device	MMI
Multi-Project Wafer Run	MPW
Photonic Integrated Circuit	PIC
Photonic Design Automation Flow	PDAFlow
Research and Development and Manufacturing	R&D&M
Semiconductor Optical Amplifier	SOA
SME	Small to medium (sized) enterprise

1. Executive Summary

The EuroPIC project was set up to facilitate access by small companies to cost-effective Indium Phosphide based Photonic Integrated Circuit (PIC) manufacture in Europe. Its objective was no less than to effect a fundamental change in the way applications based on photonic integrated circuits (PICs) are designed and manufactured in Europe. This was to be achieved by developing a generic technology that is capable of realizing complex PICs from a small set of basic building blocks; a production model well known in micro-electronics where complex electronic circuits are built from standardized transistors and a small number of other elements.

The programme adopted a holistic approach, addressing the whole production chain from idea, via proof of concept, design and prototype to product and application. Research has been carried out into manufacturing methods and high-throughput processes, which will lead to an open-access industrial generic foundry production capability for Europe. The EuroPIC generic platform for manufacturing of PICs is based on InGaAsP materials technology (generally referred to as "InP technology") which gives access to operating wavelengths typically used in telecommunications ~1.3µm - 1.55µm. EuroPIC has both set up the first generic foundry for InP-based PIC production in an industrial environment; and demonstrated its viability for SMEs. It has demonstrated the potential of the generic approach by fabricating a number of Application Specific PICs (ASPICs) concurrently on the same wafer- with high levels of complexity and performance, for a wide range of applications in telecommunications, sensors, data communications, medical systems, metrology and consumer photonics.

The completion of the EuroPIC programme heralds the start of a new chapter in the production of photonic integrated circuits. EuroPIC has not only successfully undertaken the first generic foundry run based on industrial (commercial) fabrication facilities at Oclaro (in the UK) and at FhG-HHI (in Germany), but also put in place most of the other elements of the production chain required to deliver it, and this for the first time.

Further, EuroPIC has built a strong User Group, many of them SMEs, with committed users from different application fields, who will be actively involved in introducing cost-effective ASPICs in a variety of novel applications in the future, providing Europe with a competitive advantage over the US and the Far East.

Today, Europe's lead in this branch of photonics is clear, and InP-based PIC technology stands ready for full commercialization.

2. A summary description of project context and objectives.

Context

The EuroPIC project aimed to facilitate access by small companies to cost-effective InP-based Photonic Integrated Circuit (PIC) manufacture in Europe by setting up a generic fabrication platform based on industrial fabs.

At the beginnings of EuroPIC it could be observed that despite large investments through national and international projects in Europe, America and the Far East, integrated photonics had far from fully redeemed its promises. The problem which EuroPIC set out to address was that the dominant working method in photonics was to develop optimized fabrication processes for each and every application, starting from the specifications of the product. As a result of this approach, there exist now almost as many fabrication technologies as applications. Due to this huge fragmentation in fabrication processes in relation to the associated market sizes, the cost price per product is far too high for a successful and sustainable introduction of products based on or including photonics components. In particular, the cost of entry is too high for most businesses. In order to create the breakthrough of photonics in a wide variety of application fields both the development cost and the unit cost need to be brought down by at least an order of magnitude.

The EuroPIC response was to create generic integrated technology for the research, development and manufacturing of Application Specific Photonic ICs (ASPICs). Instead of optimizing the fabrication technology for every specific application, the product design would be adapted to the capabilities of available, mature, high performance fabrication processes. This solution seems obvious in retrospect; we should introduce the same methodology to photonics that allowed micro-electronics to change the world since the eighties with CMOS technology.

CMOS, where a huge number of functions is reduced to a few elementary functions, which are performed by elementary building blocks like transistors, diodes, resistors and capacitors fabricated in a generic process, supports integration of these elementary building blocks in large numbers and in different circuit topologies. Therefore CMOS is capable of realizing a wide variety of functions (chips) for a very broad range of applications. The fabrication processes can be made available via foundries to a large number of designers who use powerful design kits that allow fast and accurate design of the chips. In this way the large investments in development of the high-performance foundry processes can be shared by a large number of applications, resulting in a low cost price per product, thus enabling the current ubiquity of electronic integrated circuits.

Competing technologies for photonic integration have also advanced over the four years since the EuroPIC objectives were written; notably Si-photonics and the passive dielectric platform TriPleX. With differing strengths and weaknesses, our current assessment of the capability of three different approaches is summarised in Table 1. Silicon based Photonics for example has demonstrated several key building block developments in the last few years using various technologies, but integration of these into the same CMOS compatible platform remains a significant challenge as does the provision of an on-chip optical source with reasonably high output power. The InP platform remains in a strong competitive position, and has high complementarity with the capabilities of Triplex.

	Performance		
Building block	InP	Si	TriPleX
Passive components	●	●●	●●●
Lasers	●●●	o	o
Modulators	●●●	●●	●
Switches	●●●	●●●	●
Optical amplifiers	●●●	o	o
Detectors	●●●	●●●	o
Footprint	●●	●●●	●
Chip cost	●	●●	●●
CMOS compatibility	oo	●●	●
Low cost packaging	o	o[1]/●●[2]	●●

Performance	
●●●	Very good
●●	Good
●	Modest
o	Challenging
oo	Very Challenging

[1] Endfire coupling (low refl.)

[2] Vertical coupling (med. refl.)

Table 1 Technology comparison

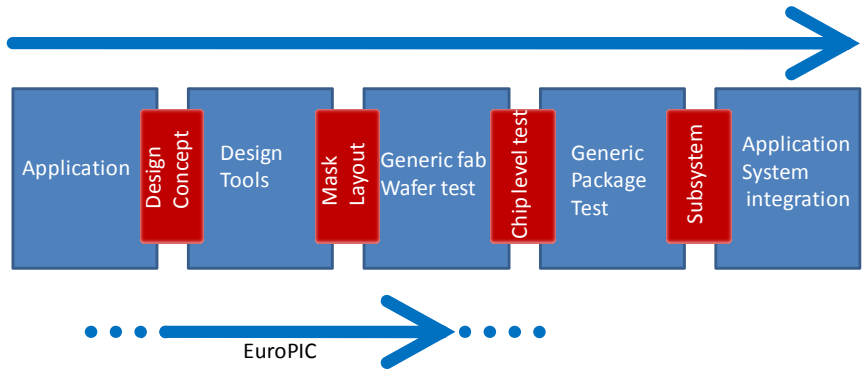

Figure 1 End to end generic process chain

Dissemination level		
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Generic Process

The process chain to PIC production is shown schematically in Figure 1. EuroPIC has addressed core aspects of this process chain, ranging from PIC design to consideration of approaches to generic packaging.

The methodology the consortium has applied to reach its project goals is:

- To decompose the functionality of complex photonic micro-systems into a small set of basic functions.
- To develop a Building Block for each of the basic functions and to develop production processes that are capable of integrating the basic Building Blocks in any arbitrary combination and number.
- To develop a dedicated design kit that contains an accurate model of the performance of the basic Building Blocks and that can simulate the response and the performance of complex circuits built from these building blocks as well as generate the mask layout.
- To develop dedicated measurement tools and vehicles for testing the quality and performance of the basic Building Blocks, in such a way that testing the performance of complex circuits is reduced to proper testing of the basic Building Blocks.
- To test the foundry concept with examples of high complexity ASPICs
- To develop a small set of generic packages that can be used for a broad class of PICs, by introducing standardization in the positions of optical and electrical connections, in chip dimensions and positioning of heat generating elements, which allows designers to work with them to work seamlessly in the design environment.

This methodology has been applied to two platforms, based on PIC fabrication, at the Fraunhofer HHI, Berlin and at Oclaro, UK respectively. It has delivered a ***generic integration technology*** at both.

Objectives

The project has achieved (√), or made significant progress (❑), in all aspects of its initial objectives. In summary the project aimed to:

❑ To bring the application of photonic integrated micro-systems with a high added value in advanced products within reach for a broad class of SMEs by reducing the entrance costs dramatically by more than one order of magnitude.

✓ To enable the emergence of a new field of research in circuit-based photonic devices with ever increasing complexity and performance. To demonstrate this, a number of target application PICs were produced, some constituting “hero” experiments in the technology, with a record combination of complexity and performance realized in a vastly reduced development time.

- ✓ To investigate novel technologies for extending the functionality supported by a basic manufacturing process.
- ✓ To shorten the R&D cycle time significantly by developing a software design kit with accurate models of the basic building blocks and their performance.
- ❑ To develop a generic test methodology that allows for a significant reduction of the effort required for testing and qualification, by testing the basic building blocks rather than specific PICs.
- ❑ To develop a generic packaging approach that allows for packaging a variety of different PICs with a small set of standardized packages.
- ❑ To develop a business model for a rapid but evolutionary introduction of the generic foundry approach in a number of application fields, mainly by and for SMEs.

Status

EuroPIC has not only successfully undertaken the first generic foundry run based on industrial (commercial) fabrication facilities at Oclaro (in the UK) and at FhG-HHI (in Germany), but also put in place many of the other elements of the production chain required to deliver this capability, and this for the first time. It has investigated new process methodologies and technologies capable of platform introduction in the future and new routes to generic packaging, going on to fabricate ASPICs of significant complexity and performance.

The Application Specific PICs (ASPICs) which result can take many forms, from a few basic building blocks such as waveguides, detectors, amplifiers and phase modulators to complex photonic chips with hundreds of building blocks can be designed and fabricated. The example in ***Figure 2*** is of a data serialiser chip realised at Oclaro, designed for application in KM3NeT (cubic kilometre neutrino telescope).

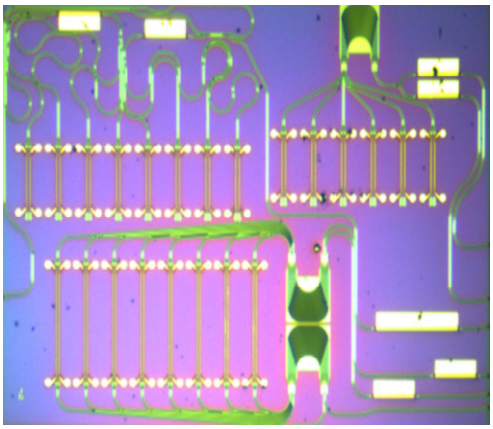

Figure 2 An ASPIC designed for application in KM3NeT - it is scalable, it can take data from 8 detector modules and load them onto one fibre output. Operating at an aggregated rate of 32GBits/s, it contains ~50 Building Blocks.

3. Technical Achievements

State of the art (start of project)	EuroPIC target	Progress
Developing specific manufacturing technology for each new PIC application	Demonstration of the feasibility of a *generic integration technology* that allows for R&D&M of ten integrated micro-systems with a high added value for application in advanced photonic products	√
Chip development costs in multi-M€ range even for relatively simple devices	Generic integration methodology to allow chip development cost reduction by at least one order of magnitude	√
Chip development timescales of several years	Put in place design tools and methodology to allow chip development times less than one year	√
PIC applications mainly in telecoms	Broaden applications to sensors, health, datacom, instrumentation, signal processing, and more	√
Few SMEs involved in new Photonic device development	100 SMEs involved in design and development of products containing novel photonic devices	100 - strong user group (Not all SMEs)
Technology development slow despite large investment	Acceleration of technology development speed because of focussed investment on a small set of broadly applicable technologies	√

Table 2 Advances beyond state-of-the-art

Objectives

EuroPIC has been successful or made significant progress against all of its objectives. The project has

- Successfully established the software-design-foundry work flow chain
- Software design kit built to support generic platform operation. The design kit features physical layer models and mask layout software. Integrated BB descriptions
- Platform supported by *Design Manual* for InP photonic circuits.
- Circuit models ported through an API between different elements of the design toolkit.
- Carried through the first generic platform run for InP PICs in Industry – a key enabling step to achieve the programme objectives discussed above.
- ~20 different ASPIC designs realised on the platform with state-of the art complexity, plus 5 external user designs. Application level exploitation and demonstration of technology access for SMEs.
- Demonstrated full BB transfer cycle onto the platform for AWG technology (both at FhG-HHI and Oclaro). Another key objective for the project opening the path for future platform transfers. The project has also advanced several other technologies towards platform status; a theme which is expanded upon below.
- Worldwide awareness of photonic foundry operation raised significantly

But further technical work remains to be done to bring the platform to commercial realisation.

- Wafer validation (establishing the compliance of the finished wafer with accepted platform performance standards) - methodology not yet fully established.
- BB design data is still sketchy in places - more detailed and comprehensive building block characterization is required.
- Generic test. Approaches to bar level test developed at Oclaro Technology have not yet worked through to full measurement data sets.
- Generic Packaging –chip – daughterboard approach demonstrated. Generic design rules established. Performance (alignment accuracy) not yet established. Daughterboard – motherboard integration (should be the simpler step) not yet demonstrated.
- Procedural/organisational aspects of the generic fab

Generic fab concept

EuroPIC has created for the first time a foundry process for InP based photonic integrated circuits using industrial InP fab processes. A crucial aspect for photonic circuit designers has been to put in place a *Design Environment* to support easy access to the platform technology. In this technical report we outline the technology which makes the InP based generic fab a reality.

Multi-Project Wafer runs

The methodology the consortium has applied is:

- To decompose the functionality of complex photonic micro-systems into a small set of basic functions.
- To develop a Building Block for each of the basic functions and to develop production processes that are capable of integrating the basic Building Blocks in any arbitrary combination and number.
- To develop a dedicated design kit that contains an accurate model of the performance of the basic Building Blocks and that can simulate the response and the performance of complex circuits built from these building blocks, as well as supporting mask layout.
- To develop dedicated measurement tools and vehicles for testing the quality and performance of the basic Building Blocks, in such a way that testing the performance of complex circuits is reduced to proper testing of the basic Building Blocks.
- To test the foundry concept with examples of high complexity ASPICs

This methodology, which has been applied to two platforms, based on PIC fabrication at the Fraunhofer HHI, Berlin and at Oclaro, UK, has delivered a ***generic integration technology***[1] at both. At the conclusion of EuroPIC[2] the HHI supported process is a receive side platform with passive components and a 40GHz detector capability. The Oclaro platform meanwhile has a full transmit/receive capability but at 10GHz.

Decomposition of the foundry process into elementary building blocks, and some more complex composite blocks, enables different ASPIC designs to be easily designed on the same platform and compiled into a single run – a multi-project wafer run. The developed

1 M. Smit X. Leijtens, E. Bente, J. Van der Tol, H. Ambrosius, D. Robbins, M. Wale,N. Grote and M. Schell. (2011) '*Generic foundry model for InP-based photonics. IET Optoelectronics*', pp.187-194.

[2] Second generation technology developments at both fabs will see demonstration of Rx/Tx platforms with 40GBit/s capability at the end o f the PARADIGM project.

design environment, including all the software developments and definition of building blocks based on generic photonic integration technologies, has been extensively used and tested in such multi-project wafer runs (MPW run) and more than twenty different designs have been successfully created, originating from a wide variety of users, ranging from SMEs, research institutes, universities and large companies, and fabricated in separate runs by Oclaro and HHI.

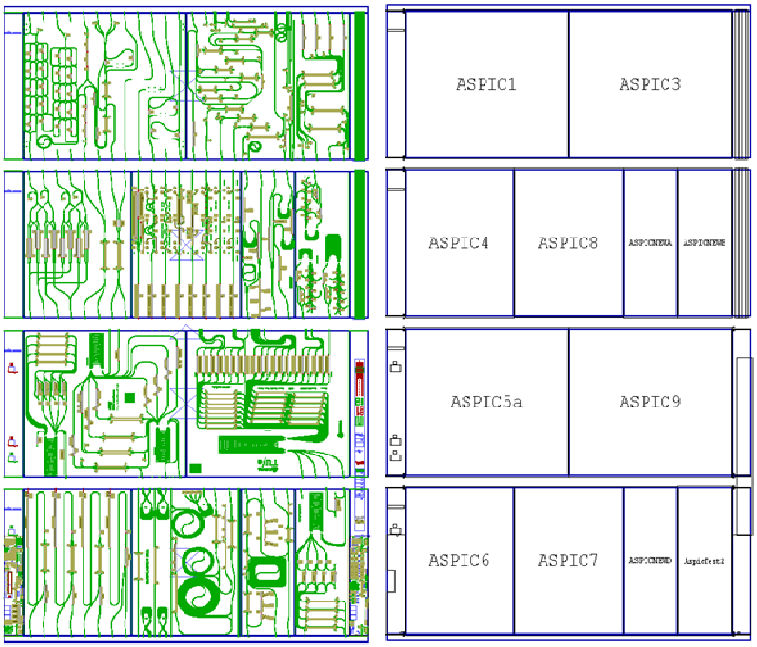

Figure 3 ***Shows an MPW layout realised in the project at Oclaro, with a representation of the reticle layout for the ASPICs on the left and the matching layout by ASPIC on the right. Each reticule is repeated many times on a 3" wafer.***

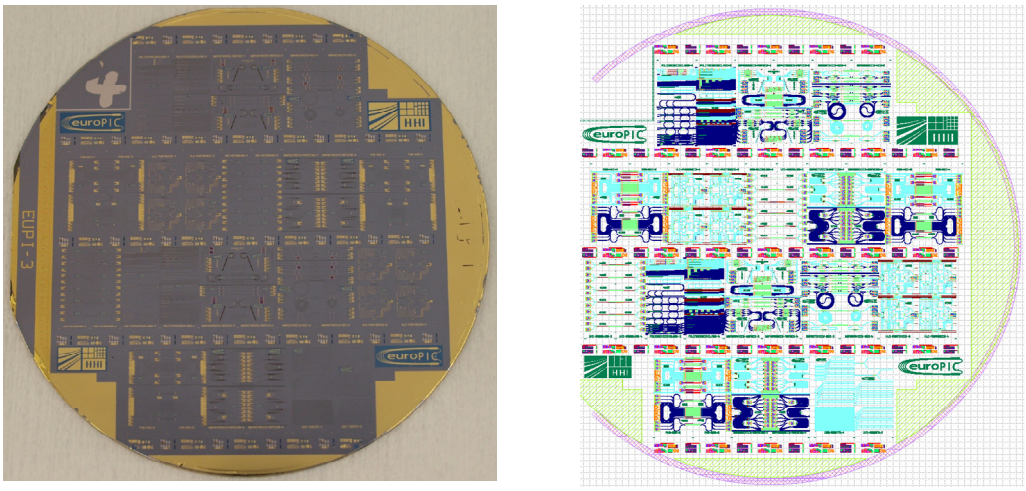

Figure 4 Shows an MPW layout realised in the project, with a representation of the reticle layout ***on the right and a photograph of the resulting processed wafer on the left. Each reticule is repeated several times on a 3" wafer***

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EuroPIC Design Environment

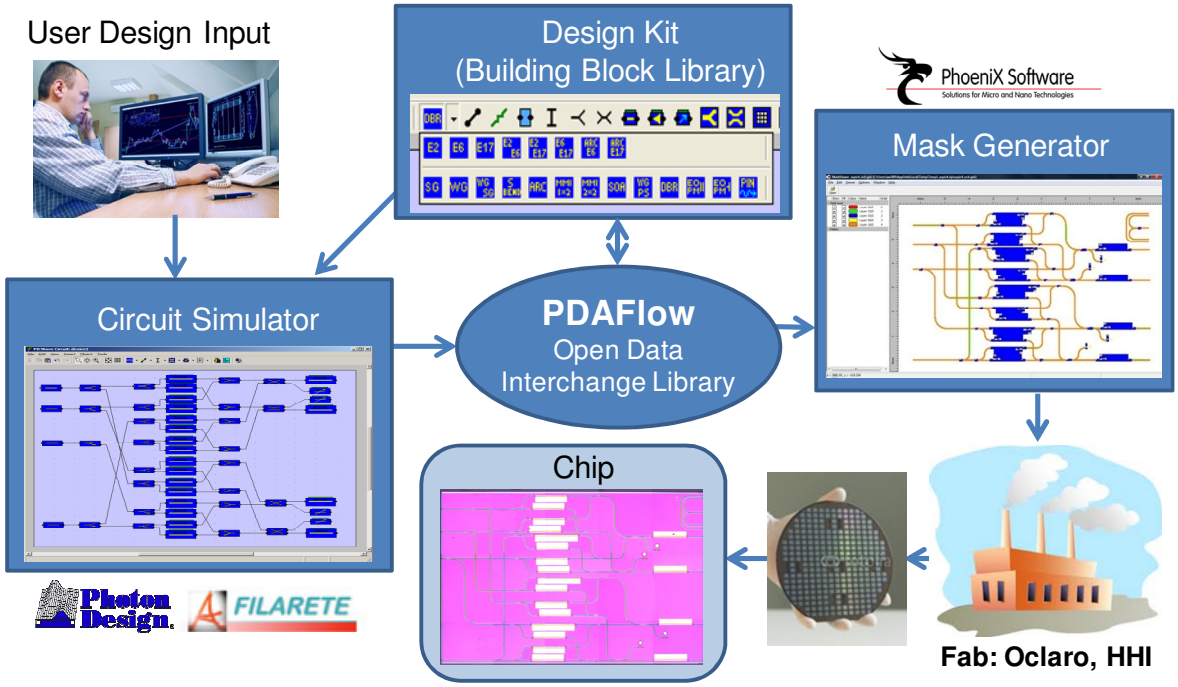


Figure 5 shows schematically how the different software elements link the designers to the fab at HHI and Oclaro. *The key enabler is the PDAFlow with its data interchange library.*

Central to the operation of the design environment is the PDAFlow API (Photonic Design Automation Flow API - Application Programmers Interface). The API created by EuroPIC contains the interface elements which enable physical layer design tools, such as Aspic from Filarete and PICWave from Photon Design, to work together with PhoeniX design tools and mask layout tools as if they were all part of an integrated package. The PDAFlow library also contains the calibrated building block descriptions for each platform.

The Design Environment.

The *Design Environment* comprises the Software Environment, the Design Manual and the technology specific Design Kits. In the EuroPIC project, Multi Project Wafer (MPW) runs for PICs fabricated in Indium Phosphide have been successfully implemented with the support of a design environment as created by partners Photon Design (UK), Filarete (Italy) and PhoeniX (Netherlands). The software partners have developed a common platform to define

photonic libraries and adopted their software solutions like *PicWave*, *Aspic* and *MaskEngineer* to be able to use these libraries or Design Kits for above named manufacturing sites. This has been done in close collaboration with the InP foundries at Oclaro and HHI.

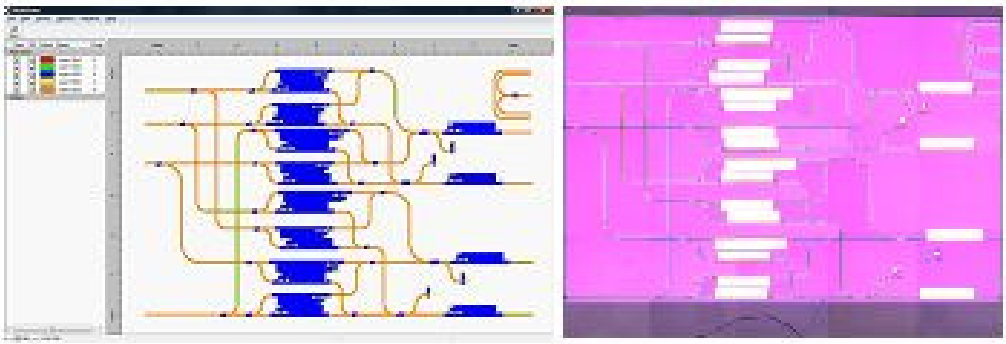


Figure 6 An example of what can be achieved with the design kit; the left half of the figure *shows the mask level information, the manufactured die is photographed on the right (Design: University of Cambridge, Fab: Oclaro. See Proc OFC 2012 for more details)*

The Design Kits contain all relevant information for designers to create a photonic integrated device or circuit within the capabilities of the fabrication processes. Users benefit from this by having immediate access to mature and proven building blocks, ensuring functional devices.

PDA Flow API

One of the key aspects of this development has been to achieve interoperability of the software elements within the design environment. In the EuroPIC Design Kit, rather than having one very large and inflexible single piece of software, the unique properties and advantages of the different software packages are maintained. This allows for easier extension towards new software partners and also provides for a robust future proof approach. The required new approach is therefore that of being able to have the software elements "talk together"; in software terminology an *Application Programmers Interface*, or API for short.

Although the concept of an API is well established, both in general software engineering and applied in micro-electronics software tooling, this was not yet the case in micro-photonics. The EuroPIC project partners have developed a photonics domain specific API, called the PDAFlow-API. After the EuroPIC project end, this API has been be transferred to the ICT

project PARADIGM[3] (FP7 ICT Project No 257210) for further development and in the near future it will be made available as a de-facto standard to interested parties through an independent foundation.

Design Kits

Building blocks containing the geometrical information such as parameters, boundaries, design rules, IP-rights, simulation settings, mask information, and release version, have been created within the project. These building blocks give a designer the capability to design at a high abstraction level by using these "standard" elements, provided by the manufacturing parties. In addition one can add additional constraints to this design, for instance by adding the boundary conditions imposed by the allowed chip sizes, package templates or packaging method. These building blocks are provided to the designers within the Design Environment, consisting of the Software Environment, the Design Manual and the technology specific Design Kit.

Design Manual

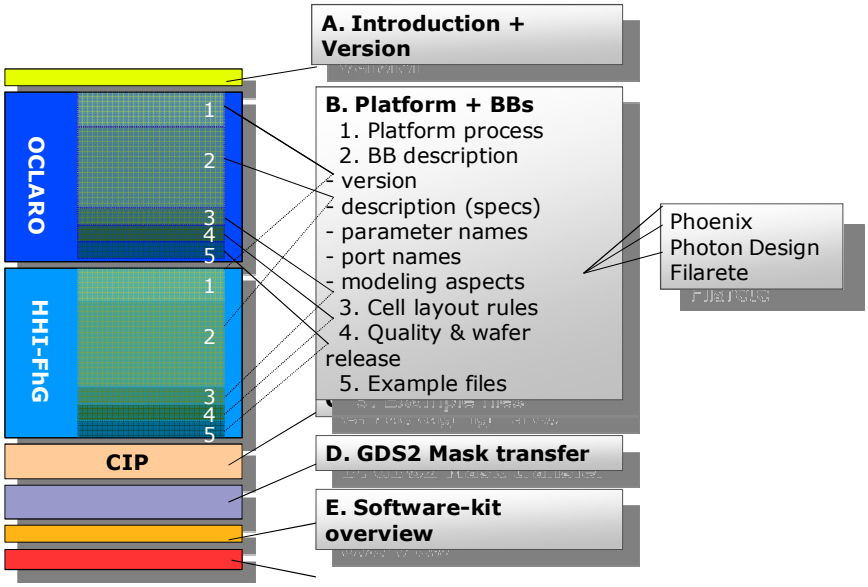


Figure 7 Design Manual Make up

An essential ingredient in the process flow is the design manual which enables the designer to access quickly the building blocks available in the platform. Design rules and standardised

[3] http://paradigm.jeppix.eu PARADIGM (ICT Project 257210) *Photonic Advanced Research and Development for Integrated Generic Manufacturing.*

templates for packaging layouts are all supplied in the design manual and configured in the design tools for ease of use.

The design manual is one of the most critical achievements of the project. It encapsulates the foundry processes in a way which makes the technology immediately accessible to PIC designer, it has already been instrumental in enabling groups independent of EuroPIC to design onto the platforms.

API Legal

During the EuroPIC project a clear interest from groups outside the consortium was already visible and the results obtained within the project indicate the usefulness of the developed API for the future.

To optimally exploit the developed capability, use of the API will be extended as widely as possible within the photonics community, and since multiple definitions and/or multiple competing APIs would, if such existed, hinder the development of a successful photonics eco-system, the three key software parties in the consortium, Filarete, Photon Design and PhoeniX Software have fixed upon the creation of a single legal entity to control the development and licensing of the PDAFlow API. A not for profit organisation will be created, structured as a legal entity in the Netherlands, a so called "Stichting". It is expected that the finalisation of the set-up of this "Stichting" will take about four months from the end of the EuroPIC project. Contacts have already been established with potential partners both inside and outside the photonics field, which will allow a quick uptake into the academic community as well as with commercial software groups worldwide. At the time the legal entity is finalised, announcements will be made to the photonics community and one-on-one communication with relevant parties continued and new discussions initiated.

InP Platform Technology

EuroPIC has two InP fab partners, Oclaro and FhG-HHI, prepared to take up the challenging task of platform development. FhG-HHI can rely on a long-standing broad expertise in InP photonics technology. In particular, it reported the world's first fully integrated heterodyne receiver PIC as early as in 1994: at that time it was the most complex PIC ever made. FhG-HHI is now a world leader in high-speed receivers, amongst others. Oclaro has also long been a leader in this field, having published many innovative PIC designs and research results going back to the early 1990s, and many of Oclaro's advanced telecommunications products presently incorporate InP PIC technology.

Process research and exploitation in InP-based photonics requires access to world class fabrication facilities and these partners have opened up access to their production lines for this project.

Oclaro's clean rooms support a full-scale manufacturing facility at Caswell, UK, offering 57,000 ft^2 (19,000 ft^2 at class 10/100) of process space dedicated to a 3" InP process capability with a capacity exceeding 6000 wafers/year. The Caswell fab is one of the largest and best-equipped facilities worldwide dedicated to optoelectronic devices and circuits. Amongst the various process tools we may note six multi-wafer MOVPE reactors, e-beam lithography, plasma etch and deposition tools and extensive on-line control and diagnostic facilities.

FhG-HHI has successfully developed a wide range of different photonic devices (amongst them various types of laser diodes, ultra-fast photo-detectors, high-bit rate modulators, components for all-optical signal processing), in many cases in close cooperation with domestic and foreign SMEs. In offering PIC foundry developments and trial services FhG-HHI, through its Photonic Components department, brings into the project its entire R&D InP processing line comprising amongst many others such expensive equipment as a newly installed multi-wafer MOVPE reactor (8 x 2"- 4"), and a high resolution electron beam lithography apparatus.

(Composite) Building Blocks	Oclaro	HHI
substrate	N^+-InP 3-inch	s.i InP:Fe 3-inch
waveguide, ridge type weak and strong guiding	X	X
waveguide transition elements	X	X
waveguide crossings		X
isolation slots	X	
curved waveguides, S-bends	X	
circular arc	X	X
Y-coupler		X
metal interconnect incl. WG crossover	X	X

(Composite) Building Blocks	Oclaro	HHI
waveguide spot size converter	X „3 µm" spot	X „10 µm" spot
phase shifter	X current inject.	X thermo-optic
EO-phase modulator	X reverse bias	
pin-PD	X dc...10 GHz	X 40 GHz
balanced pin-PD		X 40 GHz
MMI coupler	X 1x2, 2x2	X 1x2, 2x2, 1x4
SOA	X	
tunable DBR grating	X	

Table 3 Building Blocks Available at Project End.

The building blocks available on the platforms at the end of the project are summarised in the Tables below. In addition other composite elements are available such as AWGs. In this

project there has been a strong focus on compatibility between building blocks in order to build optical circuits.

While both of the two platforms of Oclaro and FhG-HHI use 3" InP wafer technology, there are to-date still distinct technological differences; whereas Oclaro's platform builds on electrically conductive n^+-substrate starting from their established and world-leading tunable laser and electro-optic modulator technology, FhG-HHI is using semi-insulating substrates (InP:Fe) starting from their proven high-speed waveguide-integrated photodetector technology. Accordingly the former platform mainly supports transmit and lower-frequency receive functions (10GHz), whereas HHI's platform is focused on receiver-type PICs capable of 40 GHz bandwidth.

The following figures give examples of such building blocks:

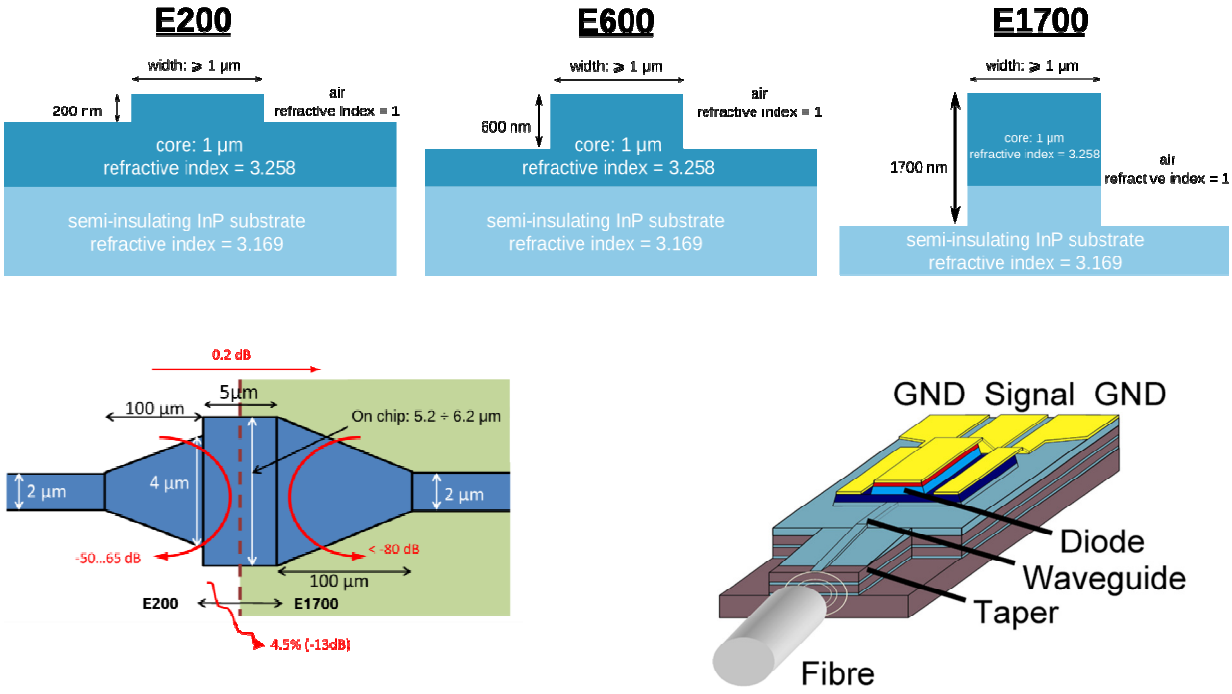


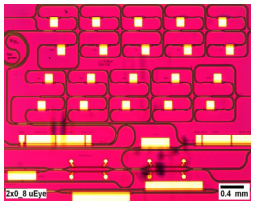
Figure 8 Building blocks of HHI platform: 3 variants of passive ridge waveguide (top); *transition between waveguides (bottom left); and 40 GHz waveguide-integrated photodiode (bottom right)*

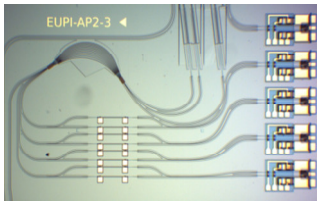
Application Specific Photonic Integrated Circuits Realized

It was the aim of the project to validate the generic foundry approach by testing the whole production chain; the functionality and performance of the building blocks, the software design tools, the generic packaging and the viability of a set of challenging applications. With that aim two so-called Multi-Project Wafer (MPW) runs have been scheduled in the

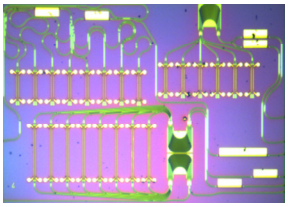
project, one halfway and one at the end of the project. They have been carried out in the generic integration processes developed by EuroPIC partners Oclaro and Fraunhofer-HHI. MPWs are wafers on which a large number of Application Specific Photonic ICs (ASPICs) are combined in a single mask set and processed in a single wafer run. This concept, which is well known in micro-electronics, leads to a large reduction in R&D and product entry costs.

ASPICs from the first MPW-run became available in 2011. First results were very encouraging and have been published at a number of conferences (OFC 2012, ECIO 2012, CLEO 2012). A second MPW run, which contained both new ASPICs and improved redesigns of a number of the original ASPICs, has just completed fab at the end of the project. With these MPW-runs, which are the world's first InP-based generic foundry runs, EuroPIC has demonstrated the potential of the generic foundry model to bring Photonic ICs within reach for many SMEs and large companies, by a dramatic reduction of the entry costs for developing complex Photonic ICs.

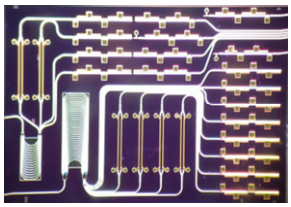

ASPIC 1: Brillouin strain sensor readout chip

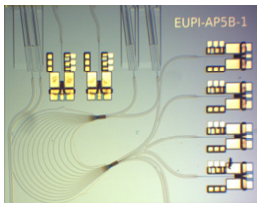


ASPIC 2: Fibre Brag Grating strain sensor readout chip


ASPIC 3: Pulse serialiser for KM3NeT Neutrino Telescope


ASPIC 4: Fast 4x4 switching matrix


ASPIC 5a: WDM-transmitter for FTTH



ASPIC 5b: WDM-receiver for FTTH


ASPIC 6: Variable repetition rate pulse laser


ASPIC 8: Tunable laser with integrated 10 Gb/s MZI modulator

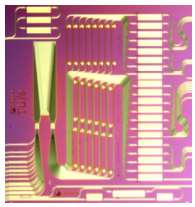

ASPIC 9: Pulse shaper for bio-imaging

Figure 9 ASPICs Fabricated *in the project*[4]

[4] B. Huiszoon, K. Ławniczuk, R.L. Duijn, M.M. de Laat, R.G. Broeke, X.J.M. Leijtens and G.N. van den Hoven, *Application Specific Photonic Integrated Circuits for FlexPON: Progress of the EuroPIC Project*, Invited paper for the 14th International Conference on Transparent Optical Networks (ICTON 2012), 2-5 July 2012, University of Warwick, Coventry, United Kingdom.
S. Stopiński, M. Malinowski, R. Piramidowicz, M.K. Smit and X.J.M. Leijtens, "Integrated optical serializer designed and fabricated in a generic InP-based technology", Proceedings of 16th European Conference on Integrated Optics, Barcelona-Sitges, 18-20 April 2012,
K. Ławniczuk, M.K. Smit, X.J.M. Leijtens, M.J. Wale, R. Piramidowicz, P. Szczepański, *Photonic integrated multiwavelength transmitters for Fiber-To-The-Home networks*, in Proceedings of 16th International Conference on Integrated Optics (ECIO 2012), 18-20 April 2012, Sitges-Barcelona, Spain.

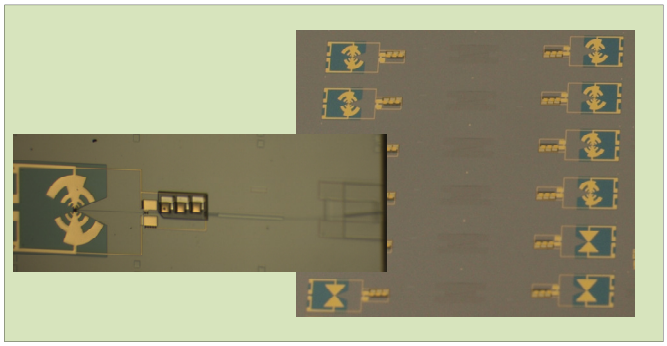


Figure 10 ASPIC 10: Opto-electronic microwave convertor fabricated at HHI.

A subset of what has been achieved in terms of ASPICs is shown in Figure 9 and

Figure 10 above. All of these ASPICs were fabricated in MPW Runs in the project, ASPIC 2, 5b and 10 at FhG-HHI, and the other ASPICs at Oclaro. These chips are amongst some of the most complex photonic integrated circuits ever fabricated in InP.

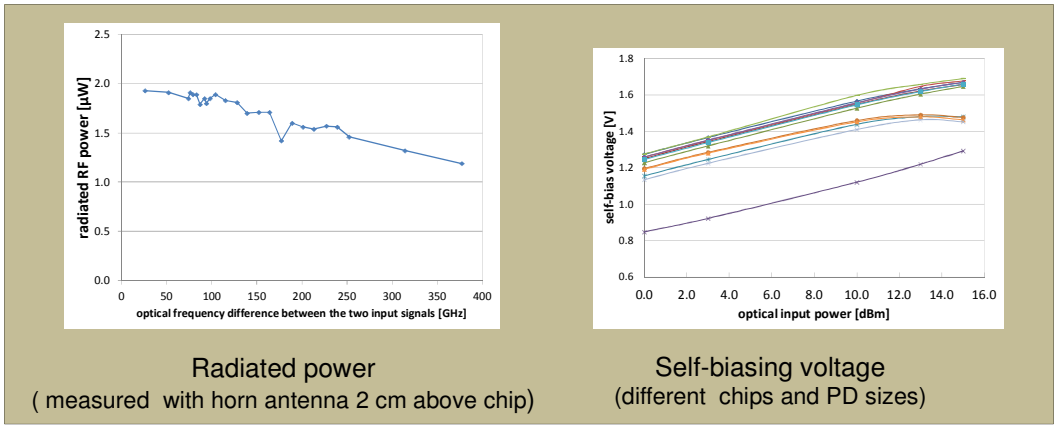


Figure 11 Performance results of ASPIC 10

M.S. Tahvili, X.J.M. Leijtens, P.J. Williams, M.J. Wale, M.K. Smit, and E.A.J.M. Bente, "*Design and Fabrication of a Monolithically Integrated AWG-based Optical Pulse Shaper*," in Proc. European Conference on Integrated Optics, pp., Sitges-Barcelona, Spain, April. 2012.
K Wang, A Wonfor, R V Penty and I H White, "Active-passive 4 x 4 SOA-based switch with integrated power monitoring", OFC 2012, Los Angeles, 2012
"X Guo, A H Quarterman, V F Olle, A Wonfor, R V Penty and I H White, Variable repetition rate monolithically integrated mode-locked-laser-modulator-MOPA device", ISLC, San Diego, 2012 **– accepted**
Robert F. Klein Breteler, Jos J. G. M. van der Tol, Manuela Felicetti, Bart Sasbrink, Meint K. Smit, 'Photonic integrated Brillouin optical time domain reflection readout unit', SPIE, Optical Engineering, Vol. 50(7), July 2011

Generic Packaging of ASPICs in EuroPIC

Generic technology at the chip level requires a generic packaging approach which can accommodate most of the requirements set by chip designers for dc electrical, RF and optical I/O. In EuroPIC our approach has been based on the use of CIP's Hyboard^{TM} approach. Hyboard uses a patterned daughterboard made of silicon to carry the InP chip which is then positioned on a motherboard containing silica waveguides. The parts are then aligned passively. The fabrication of motherboards and daughterboards uses CIP's standard etching techniques for the daughterboards and flame hydrolysis deposition of silica on silicon for the motherboards. The designs have been developed in close collaboration with the InP PIC designers. They are used to package InP chips in the following way: the InP chip is flip chip bonded to the daughterboard, and this is then flipped again on to the motherboard. All the electrical connections are handled by the daughterboard, while all the optical interfaces are handled by the motherboard. The motherboard and daughterboards have been designed to be generic for all InP chip designs, provided a set of design constraints is followed. The exception to this is that the daughterboard metallisation is specific to a chip design, and is therefore laid out by the InP chip designer using a set of design rules to make it compatible with the daughterboard.

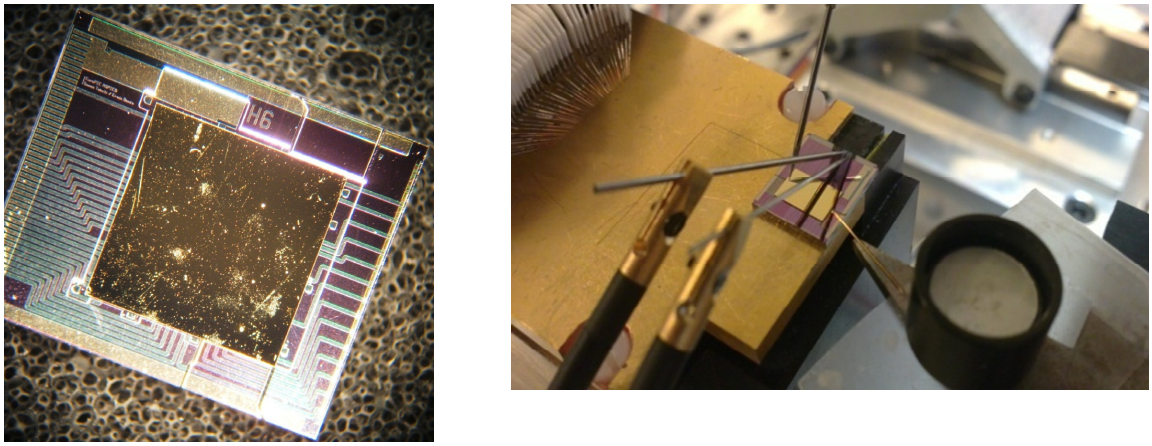
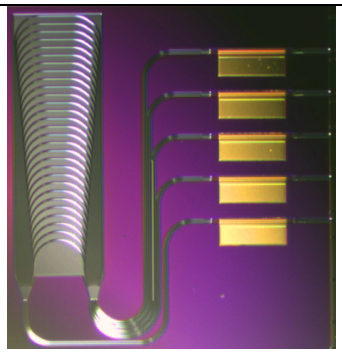
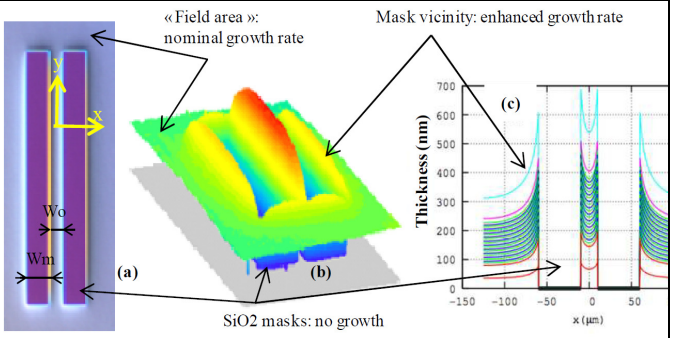


Figure 12 An ASPIC designed at TU-Eindhoven mounted on daughterboard and ready for electrical testing. The chip is mounted upside.

New Semiconductor Technology Development

The generic platform technology must not be frozen in time, but should develop alongside the requirements of the users. EuroPIC has identified several technologies valuable in platform enhancement. The project has investigated the transfer of technology (building blocks) from an R&D base onto the platforms both at HHI and Oclaro in a number of specific cases. One can identify six "maturity levels" in new technology introduction onto the platform.

1. No established technology position in consortium
2. Demonstration at a Technology house in the consortium
3. Technology assessed as ready to transfer as a building block
4. Demonstration of the building block in the platform process
5. Use in an ASPIC design by a circuit designer
6. ASPICs fabricated and tested using new BB

Building Block	**EuroPIC start**	**EuroPIC end**	
AWG technology BB	Level 2	Level 6	
Selective area growth (SAG)	Level 1 for Al(Q)	Level 3 continuation of technology platform introduction within PARADIGM. project	

Dissemination level		
PU	Public	**PU**

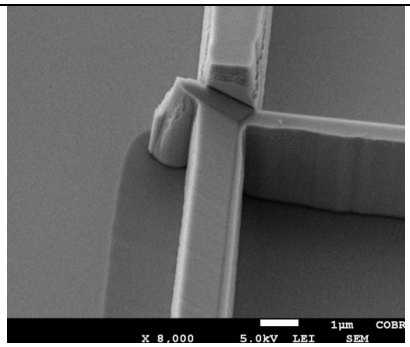
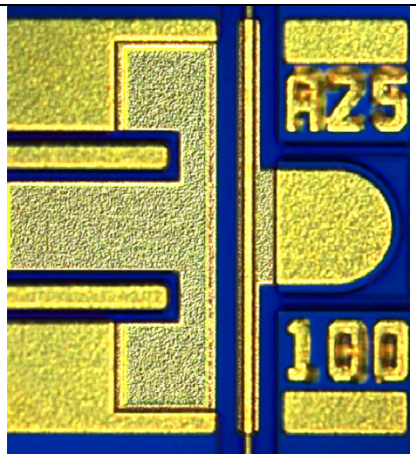
Use of Al(Q) material	Level 2	Level 4	Use of Al(Q) for improved temperature performance will become standard in future platform releases.
Low PDL SOA based on Al(Q)	Level 1	Level 3	Source material demonstrated which can be fed into the platform at process start.
Polarisation Rotators	Level 2	Level 2/3 – continu-ation of technology develop-ment within the PARADIGM. project	
Lasers on SI substrates (at HHI)	Level 1	Level 4 (Full platform intro-duction of the laser building block is an important part of the PARADIGM programme at HHI	

Table 4 New platform technologies studies under EuroPIC.

Development of the platform at circuit level

Platform technology is multi-layered. New building blocks can be transferred into the platforms by the fab specialists whilst designers, independent of the underlying fab technology, can develop their own IP on the platform through the development of not just ASPIC designs, but also new building blocks, composites and photonic circuit libraries within

the design environment. A good example of such a development within EuroPIC concerns the Arrayed Waveguide Grating based devices.

Arrayed Waveguide Filters and Multiplexers

A very important component in integrated optics is the Arrayed Waveguide Grating (AWG). This component, effectively a prism, spatially (de)multiplexes light of different wavelengths in a Photonic Integrated Circuit. The large number of constituent parts in AWGs and the required uniformity makes them very complex (circuit level) components.

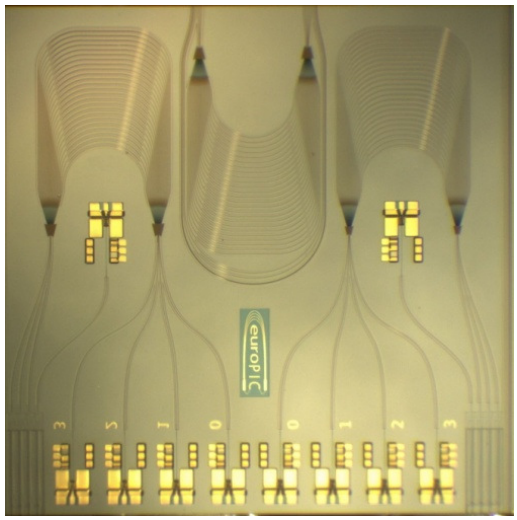


Figure 13 Photograph of AWGs incorporated into a receiver circuit (HHI platform)

The TU Eindhoven group has a long history with AWGs, dating back to their invention, and a lot of experience in the design and manufacture of this component. Within the EuroPIC project, a transfer of those capabilities to the Oclaro platform was achieved. In addition, the now commercially available BrightAWG module was successfully ported and tested in EuroPIC on the Oclaro and HHI platforms (it is also compatible with Silicon on Insulator (SoI) technology), and the resulting composite building block implemented in the design manual to allow easy access for designers. The result was excellent components that have already found their way into over 20 ASPIC designs within the EuroPIC project.

New Business Model

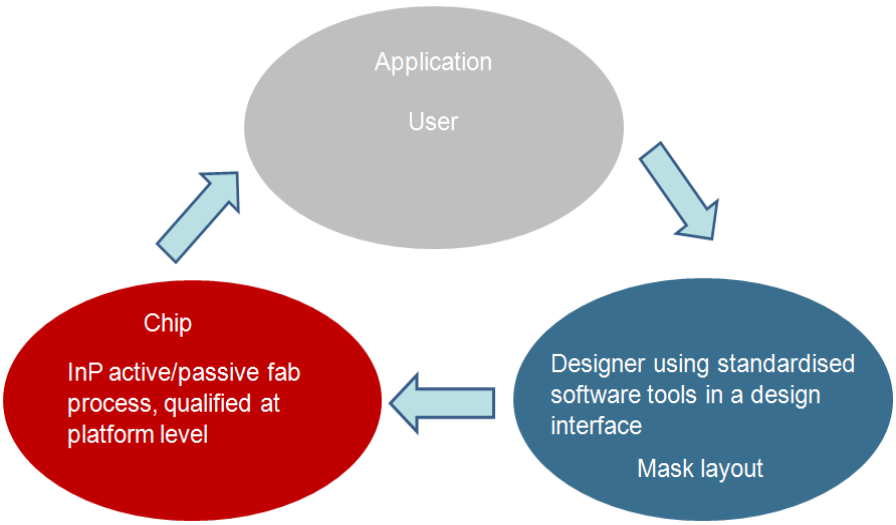


Figure 14 The generic fab eco-system

The separation of function with the generic fab leads to a new business model with the added advantage of clarification of legal responsibilities and IP ownership. Chip technology remains clearly owned by the fab and embedded calibration data can be hidden from the user in the software tools if necessary. Equally the fab can be *application blind* and as long as a circuit is platform compliant it can be fabricated without the fab having specific knowledge of its function. For immediate use EuroPIC has developed an NDA; a one-to-many agreement, for use between the consortium and interested platform users.

New Technology

Platform technology cannot stand still; it should evolve alongside the requirements of the user community. Major revisions and releases of new fab technology can occur on an occasional basis according to the platform roadmap (this point is covered in the subsection below). However, EuroPIC has also explored how new composite building blocks can be developed from existing ones (such as AWGs from passive waveguide building blocks) and how new technology building blocks can be introduced into the platform on a more evolutionary basis. Starting from a different technology provider partner there is a link formed with a fab partner to establish if a new BB can be platform compatible, and to fully characterize it. In addition those responsible for the software design kits need to integrate the new capability into the design environment to make it available to the designers. A good

example of such a development is the work on selective area growth which can extend the platforms to cover new wavelengths or extended wavelength ranges on a wafer.

Roadmaps

Working through JePPIX a roadmap for the generic fab development has been published for 2012[5].

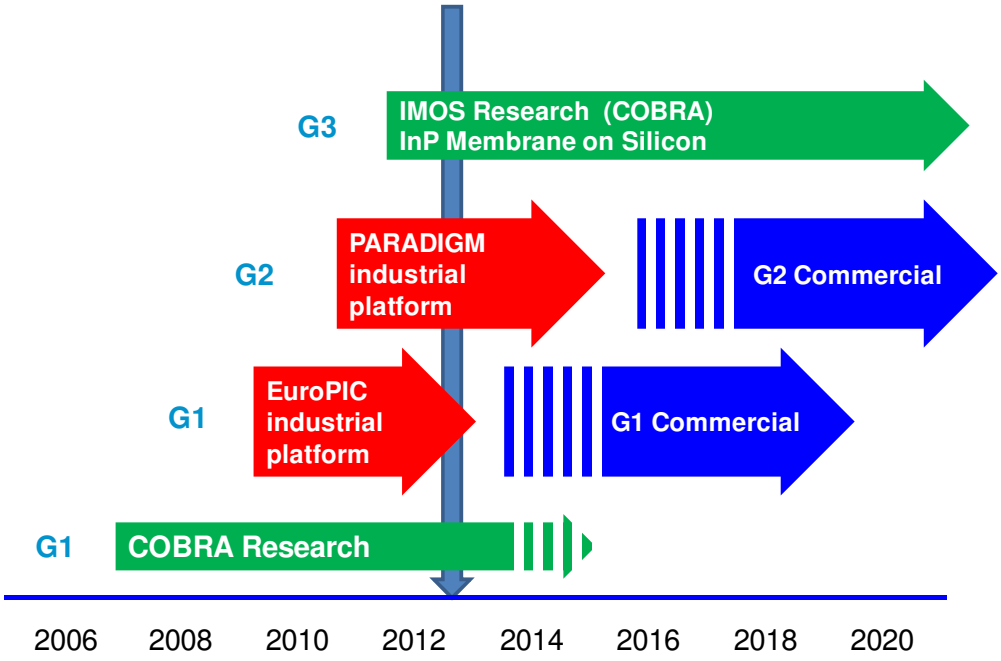


Figure 15 Roadmap for foundry commercialisation

The roadmap foresees first exploitation of the generic fab commercially through 2014 – 2015; however, the JePPIX platform and the fabs are already in close discussion about quasi-commercial activity to further trial the EuroPIC platform in 2013.

Summary

The EuroPIC consortium has taken an important first step in setting up a generic technology platform for ASPICs in InP using all industrial/commercial elements. Many successful designs have already been realised by project partners and a few by external groups trialling the platform. We stand at the threshold of commercialisation for this important technology.

[5] The JePPIX Roadmap 2012 document can be downloaded from http://www.jeppix.eu/document_store/JePPIX_Roadmap_2012.pdf

The platform organisation JePPIX (The JePPIX co-ordinator is Luc Augustin, coordinator@jeppix.eu) continues to promote the platform activities in Europe, whilst the ICT PARADIGM project seeks to extend the capability of the platforms through new technology introduction such as extensions to a full transmit and receive, and to a 40G capability, also embracing a wider range of wavelength of operation.

4. Potential Impact of the EuroPIC Project

We are confident that EuroPIC has already made a significant impact in many different spheres.

- Academia through publications and invited talks
- SMEs, large companies and academia through the user group and newsletters
- Web presence (Websites of EuroPIC and JePPIX)
- Social networking presence (LinkedIn)
- Business potential through JePPIX and GPICsLab
- Personal contacts

This view of a rapidly increasing level of interest in the generic fab is supported both by developments in the PARADIGM project where a very recent call for new users has attracted in excess of forty design proposals, and in the number of invited presentations at international conferences.

Introduction

Photonic Integrated Circuits have shown an impressive increase in performance and complexity over the last two decades. But of the many components that have been investigated and reported by academic and industrial research labs very few have reached the commercial stage, so far. The main reason is that development of PICs is very expensive and large markets (typically well beyond 100.000 pieces) are required to pay back for the required investment. Such large markets can only be served by big companies, and even for them the commercial risks are high.

EuroPIC has aimed at investigation and experimental demonstration of a novel production paradigm that leads to a dramatic reduction of PIC R&D&M (Research&Development&Manufacturing) costs by more than an order of magnitude. The expected cost reduction is such that it will bring the application of PICs in a variety of advanced products within reach for many SMEs. By doing this it lays the foundation for a dramatic expansion of the application spectrum and the market volume of PICs and novel or improved products that are enabled by or gain a competitive advantage by applying PICs for low-cost integration of complex functionality.

The EuroPIC project has taken a first step towards unlocking the power of a small set of integration processes, with cost-effective horizontal foundry access facilitated by an advanced user design interface. This will provide Europe with a lead in photonic integration

and the basis for significant SME-led economic growth in a wide range of fields that are dependent upon photonic technology.

Cost-effective, automated and high-quality manufacturing.

The major cost factors contributing to the total costs of a PIC are the investment costs of the cleanroom, the development costs of the semiconductor-based integration process, the costs of qualification and testing, the cost of packaging.

A large fab, such as the one owned by one of the partners, requires an investment of around €500M for building the cleanroom and developing the processes. It could produce around 6,000 3" wafers a year at full capacity, ultimately leading to chip costs of the order of €3/mm^2. For most, if not all fabs the total capacity is only partially used because the volume of today's applications is not large enough for the installed capacity. A number of fabs have opened their cleanrooms for developing components for so-called fabless customers. In this way the costs of the fab and part of the process development can be shared by several customers. This production model is called the ***custom foundry model***, as opposed to the ***vertically integrated model*** where a foundry is exclusively used for products from the fab-owning company. Even if it can be based on available process know-how in the fab, investments in the order of €1M or more are needed to adapt the process for the new product to the customer requirements. In the custom foundry model, sales volumes exceeding 10,000 pieces are required, therefore, for bringing the chip costs below €100 /chip. In combination with the required investment of more than €1M and the risk on future returns, this makes PICs unattractive for SMEs.

In the ***generic foundry model***, which has been investigated and experimentally demonstrated in EuroPIC, not only the fab costs, but also the process development costs and the costs of qualification are shared by all customers, because a variety of ASPICs uses the same generic process. In this approach we are left with the costs of design and packaging. The costs of design will also be strongly reduced because in the applied methodology a variety of functions is synthesised from a small set of basic building blocks By properly characterising the performance of the basic building blocks, and implementing accurate models in a design tool, the designer can be relieved form a lot of work requiring detailed knowledge of the production process, and on the longer term single-cycle product design becomes feasible for a class of ASPICs that has been designed well within the design rules, just like in micro-electronics. And most of the laborious and expensive qualification procedure that is required to guarantee long term operation under harsh conditions is no longer necessary for each individual ASPIC, but can be restricted largely to the process itself and the basic building blocks. In this way the costs of design for ASPICs with moderate

complexity can be reduced below €100,000, which will bring ASPIC costs in the €100 range already for volumes of a few thousand components. This will allow optical systems which presently cost several thousand Euros or more to be replaced with much cheaper integrated solutions. Innovative companies will accordingly be able to develop products for a wide range of applications at much lower cost, thereby stimulating growth.

Addressing New Markets

Through its SME User Group, which continues to be expanded with an active dissemination policy, EuroPIC expects to be able to address a variety of markets in which the costs of PICs are presently prohibitive for broad application. For example, in the project ASPICs have been fabricated with application in:

Sensors Fibre-based sensors are a rapidly increasing market. In 2010 their volume exceeded $650M, and estimates suggest that this could reach $3.31 billion in 2017. They play a key role in reducing environmental hazards by monitoring the integrity of large constructions like bridges, dykes, roofs of large buildings, windmill propeller blades, large reservoirs for storage of oil or chemicals, offshore platforms etc.

A new analysis from Frost & Sullivan, "World Fiber Optic Sensors Markets," finds that the market earned revenues of $656.4 million in 2010 and estimates this to reach $3.31 billion in 2017. FO sensing also plays a critical role in other applications such as security, structural health monitoring, civil, industrial, energy, and defense.

In fibre-based sensors the readout unit usually contains InP-based sources, detectors and signal processing devices in expensive equipment, which often is far more expensive then the sensing fibre itself [6]. ASPICs may substantially reduce the costs of this equipment and therefore open new markets with a value well over €100M. *Two ASPICs have been designed by TU Eindhoven, and fabricated during the project; one at HHI, one at Oclaro. The first is a chip for measuring Brillouin scattering in a fibre attached to large engineering constructions for monitoring strain levels in the construction, the second a chip measuring the strain and temperature variations in fibre Bragg gratings.*

Interconnect With the increasing processor speeds the need for photonic interconnect in computer backplanes is rapidly increasing and not only the interconnection, but also the switching should be performed in the optical domain. Fast photonic switches for Terabit server backplanes, HPC and multi-core architecture connections constitute a huge potential market for PICs addressed by a EuroPIC switch ASPIC. The market size for server backplanes is estimated to be ~$150M in 2008 and predicted to be $800M by 2012. On board

[6] http://www.laserfocusworld.com/articles/2011/03/fiber-optic-sensors.html

interconnects are anticipated to have a $4Bn market by 2012. Large data centre operators such as Google have also embraced optics as a route to managing the enormous data flows (and associated power demands) of modern computing. *University of Cambridge has designs and tested a number of 4x4 port optical switch designs, built from semiconductor optical amplifier (SOA) based switching elements. This integrated switch is designed to operate as a transparent switch, being both lossless and transparent to the data-rate of the optical signals that it switches.*

Telecommunications So far, telecommunications has been the main driver for PIC-development. Fibre based networks of increasing speed have been required to carry internet services, with increasingly more sophisticated use of bandwidth. To support this growth in data rates PICs of ever increasing complexity are required. The access market is especially interesting for a foundry approach because of the large market volumes which could run to many millions of chips in Europe alone. *EuroPIC has addressed three ASPIC designs for access networks: one for application in a WDM Fibre-to-the-Home(FTTH) network, and two for Radio-over-Fibre (RoF) applications in wireless access. The WDM FTTH application addresses development of a chip that runs the communication with 20-40 subscribers in the Central Office. Further a fast tunable laser demonstrates the potential of the EuroPIC technology for demanding applications in the core or Metro network***.**

Medical applications and signal processing The wavelength window around 1.5µm, that can be addressed with InP-based ASPICs, is particularly relevant for diagnostic analysis of opaque tissue, because the penetration depths at these wavelengths are a factor of 3 higher than in the near IR window around 0.8µm, up to a few millimeters, due to lower scattering losses in the tissue. This is particularly relevant for analysis of suspect skin tissue or intra-arterial diagnostics, using techniques like Optical Coherence Tomography (OCT) or Raman Scatterometry. The market for OCT equipment presently exceeds €200M. The market for Raman scatterometry is a factor of ten smaller, but if it is possible to integrate the Raman sensor on an InP-chip at a cost of a few hundred €, it may be applied in a tool that will be in the diagnostic toolkit of a significant proportion of all doctors (more than a million for the EU alone). Another application is in non-linear microscopy where sub-picosecond pulses reveal properties of biological tissue that cannot be assessed in another way. Mode locked lasers are promising devices for producing the short pulses required for these applications, but they are also useful in high-speed data transmission and clock generation. *The University of Cambridge has demonstrated for the first time an integrated, high quality, variable repetition rate short pulse source (mode locked laser) for bio-photonic applications with 109MHz – 14GHz repetition rates using the Oclaro platform.*

These are just a few examples of the ~20 different ASPIC designs realised over the life of the project with a broad range of applications in mind. In addition to the existing consortium partners, EuroPIC has been careful to identify commercial exploitation routes for these developments and we are convinced that the ASPIC cost level targeted in EuroPIC will generate many more applications still. The market for ASPIC driven products could exceed the €1Bn level within a decade and EuroPIC has taken an important step to provide Europe with a lead in this development.

Matching global regulatory requirements

By simplifying products we eliminate many components that are conventionally needed, thereby reducing the use of materials and the corresponding environmental impact involved in their production. With regard to the semiconductor fabrication processes, by building all circuits on well proven, qualified processes we eliminate many yield hazards, thus maximizing the number of chips that can be made per process run and again reducing materials use.

Transfer from research to industrial environment.

EuroPIC is a unique example for effective transfer of an approach that has been developed in a research environment (the ePIXnet network of excellence) to an industrial environment, by a consortium with a strong team of leading research and manufacturing partners. The roadmapping activity of EuroPIC and JePPIX will greatly enhance the effectiveness of transferring research results into industrial applications, by providing a clear picture to research partners where the technology development is expected to go.

Europe: world market leader.

The economics of PIC production has been under intense pressure since the growth and collapse of the telecommunications 'bubble' in 2001, leading to radical restructuring and consolidation of the photonics industry. New business models continue to be explored. At one extreme, systems companies such as Infinera have adopted a value chain based on intensive vertical integration, with their chips being the enabler for specific systems solutions. At the other extreme, we see the emergence of huge chip manufacturing organizations in the Far East, notably in China, serving diverse fields including solid state

lighting and solar energy, as well as the kinds of photonic devices considered here. It will be very difficult for European and US companies to compete with such large fabs for manufacturing of simple commodity components. As is recognised by Horizon 20/20, it is mandatory for Europe to move to technologies that require a significantly higher level of knowledge. A generic integration technology is such a technology, where knowledge translates to a high added value for advanced products. In the USA the emergence of the OPSIS[7] organisation for Si Photonics is a significant development. Through EuroPIC Europe has retained its lead in InP based technology and Europe is excellent position to become a world market leader for design and manufacturing of ASPICs.

Additional Impacts

Moving from device R&D to circuit design and development

The creation of a generic technology base with a well defined user-interface will cause a shift from device-oriented R&D to circuit design and development. This will enable much more complex functionalities to be realised than is possible with today's device oriented approach. The impact of this development can hardly be over-estimated: it will open new fields of research on a much higher abstraction level than today's device engineering. In the long term, novel developments in the field of micro- and nano-lasers indicate that up to one million components per chip in digital applications may become feasible. This will enable applications that are far beyond our present imagination. The present project addresses a first crucial step in this direction.

Societal impact

Through a radical shift in thinking the achievements of the project stimulate high-technology, high-skill economic development across many sectors. In micro-electronics, which has adopted a foundry model, a lot of fabless IC companies have been very successful in Europe and high-value, high-skill jobs have been created. New applications, in health care, sensors, metrology and consumer devices, will themselves bring important social benefits. Many of the companies in these markets are SMEs and our project will stimulate the growth of this next generation of European industries maintaining high skill jobs for Europe, not only in the design and manufacturing of the photonic circuits themselves but particularly in the design and manufacturing of systems based upon them.

[7] http://opsisfoundry.org/

The market penetration of cost-effective ASPICs is expected to have an impact in many aspects of daily life. For example, in structural health monitoring with implications for safety and energy efficiency, in health, and in sensing, data transport and telecommunications where integrated solutions will be more energy efficient and can support more complex control systems such as in traffic flow.

European dimension

European regions that presently lack the relevant technological infrastructure, for example in the new member states, can gain access to the fabrication technology through the new EuroPIC business model which opens the way for them to take advantage of opportunities to develop and exploit advanced PICs. As part of the PARADIGM project a design hub centred on University of Warsaw has been created for precisely this purpose.

Countries such as France, Germany, The Netherlands, and the UK, have a strong history in photonics and semiconductor technology and in some partner countries such as the Netherlands, current funding policies at the national level have created a dynamic business community with many new high technology companies in this area.

Europe has shown that it can defend its markets well in high tech areas (see for example German strength in automotive engineering and in photonics) and we are confident that given suitable access to generic fab facilities, SMEs across Europe will take advance of the technology offered, keeping them competitive and indeed giving them a significant advantage on the world stage. So far Europe has the lead in this technology development and programmes such as EuroPIC help this to remain the case.

National and International Activities

The project is intimately connected with the existing JePPIX platform. JePPIX, which has recently been appointed a part time coordinator at TU Eindhoven, provides for university-based training in design techniques and coordination of relevant research, as well as outreach to a wider user community in both academic and commercial spheres. EuroPIC proposes the GPICsLAB[8] concept to enable interested groups, particularly SMEs with related technical goals, to collaborate on ASPIC development in the pre-competitive phases of development. JePPIX will work with EuroPIC partners to set this up in the coming months, focussing around the needs of companies working in the fibre-based sensor area.

[8] The GPICsLAB concept is elaborated much more fully in project deliverable D1.6. It provides a focus for SMEs to participate in and share the costs of a joint PIC development activity. It will provide a cost effective means for SMEs with common objectives, but little experience in photonic integration, to develop the skills of their employees and to accelerate the uptake of new technology. It is modelled on the successful DevLab concept (http://www.devlab.nl/)

Dissemination activities and exploitation of results

EuroPIC has been very active in its dissemination of the foundry concept. It is represented in a "Linked-in" discussion group set up through JePPIX, and at the industry level through EPIC involvement.

Publications at conferences and in scientific papers:

In addition to material published on its public website (http://europic.jeppix.eu , EuroPIC has

- In excess of 50 publications
- Increasing numbers (~15 in 2012 alone) of invited presentations on aspects of the generic fab show growing interest worldwide.

User based activities

- Three user group meetings have been held to date
- Six newsletters have been published
- JePPIX roadmap 2012 published.

Training

Course held in Eindhoven annually

- Broadly based, JePPIX-TU/e umbrella
- Two week introduction to photonic circuit technology, and chip design.
- Attracts ~20 attendees each year

Recognition of training needs alongside the developments in design environment and fab has been an important aspect of EuroPIC. Future training plans are continuing to mature alongside the PARADIGM project which features regular calls for applications groups external to the project to propose designs. Training courses have been continuously adapted to new platform requirements as they have developed. Many training sessions have been held by software partners on tools specific to EuroPIC, both to support existing consortium partners and other interested individuals, for example for training courses targeted at the EuroPIC Run 2 designers hosted by PhoeniX in July 2011 and the project has launched a new 'one week' focussed, circuit based, design course to support new designers on the platform as part of its the Training Expansion programme.

Design Manual

Controlled by NDA, the ***Design Manual*** is effectively a public document for those interested groups prepared to sign up. Setting up the means to distribute user level information such

Dissemination level		
PU	Public	**PU**

as the Design Manual, and information about the status of multi-project wafer runs has been an important aspect of the project.

PDAFlow API

The software, which is at the heart of the new design environment, will also be 'published' though public release via and independent foundation, or Stichting, in the Netherlands.

5. EuroPIC General facts and figures

Project Number: FP7 programme: EuroPIC CP-TP 228839-2 *European manufacturing platform for Photonic Integrated Circuits*

Project Start Date: 1st August 2009

Project Duration: 36 months

The public website address for the EuroPIC project is http://europic.jeppix.eu

Partners in the EuroPIC consortium are:

Technical University of Eindhoven (Co-ordinator)
Willow Photonics Ltd, UK
Oclaro Technology, plc., UK
PhoeniX Software, Netherlands
CIP Technologies, UK
BB Photonics, Netherlands
Alcatel-Thales III-V Lab, France
Genexis, Netherlands,
Photon Design Ltd, UK
Filarete, Italy
University of Cambridge, UK
FiberSensing, Portugal
Baas B.V., Netherlands
Fraunhofer Institute for Telecommunications,Heinrich Hertz Institute, Germany
VanderHoekPhotonics, Netherlands
EPIC, France

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European manufacturing platform for Photonic Integrated Circuits

SEVENTH FRAMEWORK PROGRAMME

Dissemination level		
PU	Public	**PU**

6. JePPIX General facts and figures

Joint European Platform for InP-based Photonic Integrated Components and Circuits

JePPIX (http://jeppix.eu) is a platform for **low-cost development** of Application Specific Photonic Integrated Circuits (ASPICs) in Indium Phosphide. JePPIX aims at a **generic integration technology** in which a wide variety of ASPICs can be designed and fabricated using a **standardized process**, similar to 'fabless' ASIC design and manufacturing in microelectronics.

Its **Mission is to develop the technological infrastructure for InP-based foundry operation** (standardised foundry processes, design kits, component libraries, generic packaging, generic testing)

The platform is working with key companies in the field of Photonic Integration, which are cooperating in projects like EuroPIC (EU-NMP), PARADIGM (EU-ICT) and MEMPHIS (NL) to establish the feasibility of this new design and manufacturing methodology using **full-scale industrial processes**. It seeks to develop design toolkits for rapid prototyping and to stimulate the expansion of commercial activity.

JePPIX activities so far include:

- offering small-scale access to a university process for fabrication of PICs (supported by COBRA-TU/e), for research purposes,
- organisation of a successful symposium Third European Platform Integration Forum (EPIF2011); 21st June, (Eindhoven, Netherlands) to inform potential industrial users about the possibilities of Photonic Integration, which was attended by more than one hundred participants,
- setting up of a User Group consisting of companies and institutes that are interested in application of PICs in their products or systems. This group already counts more than 100 members and is rapidly expanding.
- organisation of an annual 2-week training course in PIC design and integration technology. This course has run each year since 2006 with an average attendance of ~20 scientists.
- providing design support for users that design PICs in the COBRA foundry runs.

JePPIX already provides a brokering service on a small scale, facilitating access for potential users to the COBRA fab and organizing training activities and support.

Partners: Europe's leading

- Chip manufacturers & packaging (Oclaro, FhG-HHI, CIP)
- Photonic CAD companies (Phoenix Software, Photon Design, Filarete)
- Equipment Manufacturers (ASML, Aixtron, Oxford Plasma Tech)
- Research Labs (III-V Lab, COBRA, Cambridge, Politecnico di Milano)
- Coordinator: COBRA

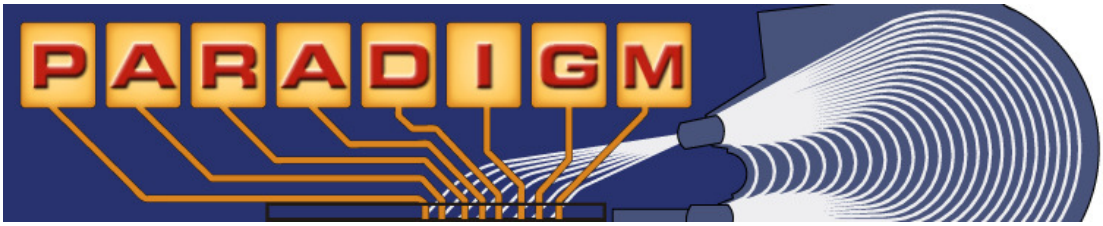
Related Projects:

EU: EuroPIC & PARADIGM

Netherlands: MEMPHIS, IOP Photonic Devices, STW GTIP

The JePPIX coordinator, based at the TU Eindhoven, is Luc Augustin. coordinator@jeppix.eu

7. PARADIGM General facts and figures



Project Number: FP7 programme: ICT 257210 PARADIGM *Photonic Advanced Research And Development for Integrated Generic Manufacturing*

Project Start Date: 1st October 2010

Project Duration: 48 months

PARADIGM is an integrating technology project and primarily concerned with foundry platform process development based on technologically advanced InP platforms. It focusses on advanced platforms for 40GHz transmit and receive functions and extended wavelengths of operation. Packaging is essential to complement the generic PIC technology and PARADIGM is investigating suitable 'generic' designs of photonic package capable of dealing with large numbers of dc and rf + optical I/O. Through calls organised by the consortium PARADIGM has formed a group of applications providers (the Applications Group). PARADIGM will work closely with its Application Group to trial real examples of applications specific PICs on its platforms.

Partners in the EuroPIC consortium are:

Technical University of Eindhoven (Co-ordinator)
Willow Photonics Ltd, UK
Oclaro Technology, plc., UK
PhoeniX Software, Netherlands
CIP Technologies, UK
Bright Photonics, Netherlands
Alcatel-Thales III-V Lab, France
Photon Design Ltd, UK
Filarete, Italy
University of Cambridge, UK
Fraunhofer HHI, Germany
Fraunhofer IZM, Germany
Linkra srl (Compel) Italy
Gooch and Housego (UK)
Politecnico di Milano (Italy)
Chalmers University (Sweden)
University of Warsaw (Poland)

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or go to the project website http://paradigm.jeppix/eu .

Dissemination level		
PU	Public	**PU**