PROJECT FINAL REPORT

Grant Agreement number: **242 521**

COMETS

COnverters broadband low power high perforMancE for Telecommunications in Space

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1 Final publishable summary report

1.1 Executive summary

For the satellite digital communication systems designed in a tough competitive context, the European Space Industry (with the end users represented within the project by EASDS Astrium Stevenage (UK) and Thales Alenia Space Toulouse (FR) requires advanced components in terms of performance, flexibility and power consumption. Indeed, future telecommunications payloads will contain digital processors to make best use of scarce spectrum and to offer best operational flexibility to operators and end-customers.
This puts ever more drastic requirements for Data Converters and in particular onto Analogue to Digital Converters (ADC).
As they are strategic components for satellite communications, the COMETS project research effort on European sourced radiation hardened ADC's is mandatory:

1. to respond to the demand for such high conversion capacity, currently not available on the market and
2. to ensure long-term European independence.

Starting from system level requirements is fundamental to develop the right ADC expected by the industry and to open wide market perspectives to it.

The project "phase1" lead to the 10bit 1.5GSps rad-hardened and low power ADC (ref EV10AS180AGS), to serve mid-term critical needs of the Space Industry. The ESCC evaluation according to ESCC226900 performed by e2v and the CNES has demonstrated the suitability of EV10AS180A for operation in space environment.

As longer term needs see increasing performances, a 12 bit ADC beyond State-of-the-Art is then focused in the frame of the "phase2" taking advantage of the advanced technology developed by Infineon (B7HF200) and modelling effort on bipolar transistor. This lead to the development of the 12b ADC (e2v P/N EV12AS200AGS). Characterization results exhibits above state of the art performances for high input frequency (>1GHz) at high sampling rate (1.5Gsps)

The total project duration was 41 months.

Specifications derived from advanced system level needs, proven design and radiation hardening expertise, high performance technology and related device modelling have been major assets for the COMETS project and formed the panel of factors that have contributed to the success in the project realizations.

These two ADC are key components for the European space industry to keep control on the design and production chain of the ADC's for Space telecommunications. This ensures the Europe's supplying independence for those strategic components.

1.2 Summary description of project context and objectives

For the satellite digital communication systems designed in a tough competitive context, the European Space Industry requires European sourced advanced components in terms of performance, flexibility and power consumption. Indeed, an increasing proportion of future telecommunications

payloads will contain digital processors to make best use of scarce spectrum and to offer best operational flexibility to operators and end-customers. This puts ever more demanding requirements for Data Converters and in particular onto Analogue to Digital Converters (ADC).
As they are strategic components for satellite communications, research on European sourced radiation hardened ADC's is mandatory 1) to respond to the demand for such high conversion capacity, and 2) to ensure long-term European independence.

The COMETS Programme aims at bringing to the Space Industry the European sourced advanced Analogue to Digital Converter.
The goal is to make available an ADC offering outstanding resolution, dynamic performance at low power consumption and radiation hardening to enhance satellite uplink and down link pay-load implementation, in terms of channel count and response to the rapid increase in bandwidth demands.

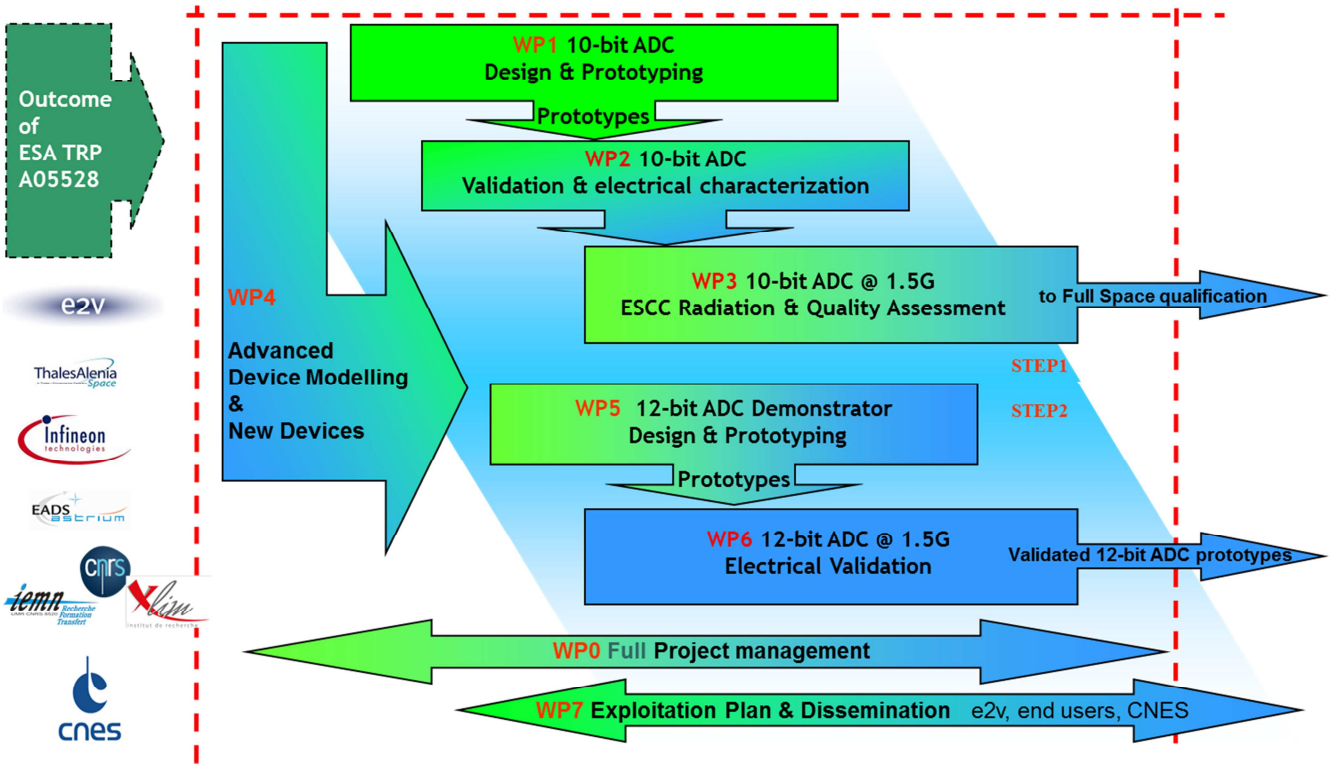
The consortium's efforts were driven by e2v (France), a company which offers to the market the fastest ADC's in the world. Consequently, e2v were the designer of the ADCs. Specifications were agreed with key end-users, both main players in the European Space industry (Thalès Alenia Space France & EADS Astrium UK).
The design of ADC's have benefited from the most advanced SiGe process from Infineon (Germany). Infineon contributed to the COMETS project not only by providing the advanced fabrication technology but also by bringing their skills in RF modelling and process reliability. As modelling of transistors and lines is a key for such beyond state-of-the-art designs, the CNRS cooperated with Infineon and e2v to optimize the simulation of critical elements. CNES ("Centre National d'Etudes Spatiales") gave their expertise related to space grade and radiation hardened electronic component development, resulting from its historical involvement and support to the space segment of the telecommunication market.

The project was phased in two steps in order to minimize the project risks and to provide tangible results already at end of the first one.

The first step "STEP1" focused on an innovative low power fast ADC with DMUX designed on the existing B7HF200 Infineon technology; this "STEP1" leads to the 10-bit 1.5 GSps rad-hardened ADC updating the level of 'State of Art' data converters, to serve the short term critical needs of the Space industry. The evaluation of the devices in performance, reliability and irradiation based on ESCC standard concludes the STEP1.

As medium and long-term needs by the European space industry demand ever-increasing performances, COMETS Project proposed a high dynamic range 12-bit resolution ADC with DMUX with a clock rate of 1.5 GSps. These performances have been the focus of the "STEP2" taking advantage of "STEP1" results, the world-class expertise of the COMETS consortium including the advanced silicon technology developed by Infineon.
The total project duration was 41 months (only 5 months beyond the 36 months original duration).

The project was then shared in seven work packages as described in the work diagram below.



So WP1 corresponded to the design phase by e2v of the 10b ADC. This phase has benefited of outcome of the 1st development supported by ESA.
WP2 focused on the validation and characterization phase by e2v and end-users of the 10b ADC. This WP was led by the Thales Alenia Space.
In the WP3 (lead by the CNES), the 10b ADC was evaluated in term of, reliability, irradiation assessment and screening based on the ESCC2269000 (European Space Components Coordination standard). This concluded the step1.

The second step focused on medium to long term needs to propose a 12b resolution ADC with an unprecedented clock rate of 1.5Gsps taking advantages of Step 1 results as well the modeling and technology improvement outcome of WP4 (lead by Infineon). WP5 was the design development phase. This step 2 will has been concluded with the validation and characterization of the 12b ADC by e2v, TAS and EADS ASTRIUM in the WP6. To note 12b ADC ESCC evaluation and space qualification are not part of the project scope.

<u>Step 1 Main outcome</u>: 10b ADC1.5Gsps
The 10b ADC is based on design on B7HF200 (SiGe) technology from Infineon that is a full vertical isolated bipolar transistor and offer low power together with high speed operation and inherently radiation robustness so suit for space application. This ADC is single core architecture (not interleaved) that does not need calibration over frequency region and/ or temperature range operation.
This architecture ensures with very low latency with 4 clock cycles pipe line delay that is quite safe in regards to radiation issue (SEU SEE) that could appears.
The 10B ADC features 8.5 ENOB (Effective Number Of Bit) together with 60dB of SFDR(Spurious Free Dynamic Range) at 1.5Gsps in L band and Fin equal to 1800Mhz and a Noise Power Ratio (NPR) of 43 dB with 500Mhz pattern. (Ultra wide band pattern) enabling direct undersampling

ultrawide band pattern in the L band region simplify and improve performance of the receiver system by removing down conversion stages, saving system global power consumption.
Hence it offers more flexible operation together with system cost reduction.
Full scale input voltage span 0.5Vpp in one hundred ohm (input power of -5dBm) is very convenient to ends users to drive the ADC especially at high frequency.
The total power consumption including a DMUX1:4 LVDS compatible logic is 1.9 watt maximum.
Temperature range for Tcase = -55degC up to Tjunction = 125degC.
The package is in ceramic and hermetic dedicated to space application. This package is custom has been designed in order to optimize high frequency operation.

A full evaluation according the ESCC226900 standard (in the frame of the WP3) is performed to proof the suitability of operation of the ADC10b 1.5Gsps in a space environment.

10bit ADC has been included on the ESA European Preference Part List.

Step 2 Main outcomes: 12b ADC1.5Gsps
Making a 12 bits ADC is not as simple as just adding 2 additional bits of the existing 10 bits ADC
On the performances it means improving the SNR performance and SFDR by at least 6 dB and one more bit of ENOB in same operating condition (1.5G L band) with a the lowest possible power trade off.
To minimize the risk, the same proven base line (fully differential) used for the 10b ADC has been used; The scale input voltage span is still 0.5Vpp in one hundred ohm (input power of -5dBm) despite it is even harder to achieve on a 12bits but (still relaxing constraint at system level) in Lband. One of the key points is also the power consumption and so defines the trade-off between speed and power.
ENOB is better than 9dB. This is compliant to final simulation and last agreed specifications but lower than the initial target.

This architecture offers the main advantage to not need calibration over frequency region and/ or temperature range operation. To be noted that is is a key advantage with regards to US competition.

Making this gap has been achievable thanks additional modelling notably of the vertical isolated PNP transistor and complement of modelling on the non-linear zone of the NPN transistor to help designers to optimize the design and of course design improvement.

This low power, high performance rad-hardened 12-bit 1.5GSps ADC & DMUX should provide the following benefits to the European space community:

- Allow to remove stages of RF down-conversion thanks to the wide analogue input bandwidth resulting in significant cost, mass and power savings.
- Provide customers with as yet unattainable dynamic range and NPR (Noise Power Ratio) performance for competitive next generation broadband applications.
- Open new opportunities in existing markets such as cellular communications, broadband multimedia.
- Decrease the number of conversion chains and associated costs (both fixed and operating costs) by the capability to process 500 MHz bandwidths of data.
- Allow to revise and optimize the frequency plan thanks to the flexibility of a fully digital payload.
- Ensure future-proof compatibility in digital output interconnectivity as digital processing component speeds and capacities for space applications advance in the future.

- Be ITAR free

1.3 S&T results / foregrounds

1.3.1 WP1: ADC 10-bit / 1.5 Gsps Design

This work-package consists of the design and manufacturing of the 10b 1.5Gsps ADC.

Task 1.1: Specification
The table below summarizes the target specification

Table 1. 10-bit 1.5 GSps ADC Target Specifications

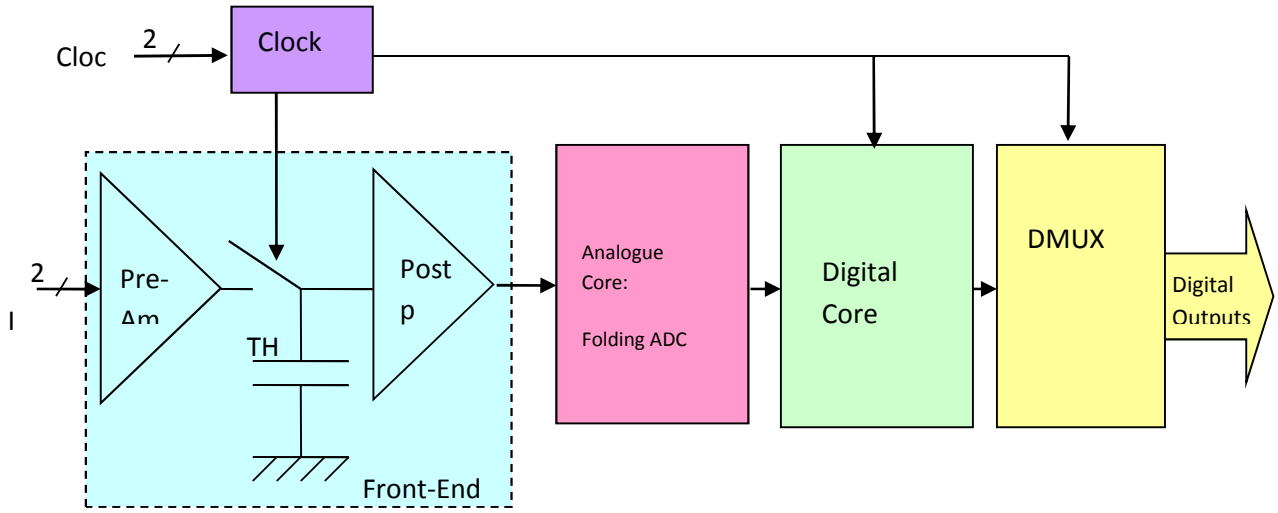
Parameter	Typical value [original requirement]	Comments	Final Specification	Unit
Fsampling	1.5	Maximum sampling clock frequency	1.5	GSps
Fin	1.8	Effective analogue bandwidth (-3dB)	1.8	GHz
Ain	1	Differential analogue input	0.5Vpp	Vpp diff
Vcc	5 / 3.3	Analogue and Digital supply	5/3.3/2.5	V
P	1360	Total power dissipation with DMUX 1:2	1700	mW
ENOB	8.5	Fc = 1.5 GHz, Fin = 750MHz, -12 dBFS	8.5	Bit FS
SFDR	62	Fc = 1.5 GHz, Fin = 750MHz, -12 dBFS	62	dBFS
THD	60	Fc = 1.5 GHz, Fin = 750MHz, -12 dBFS	60	dBFS
SNR	55	Fc = 1.5 GHz, Fin = 750MHz, -12 dBFS	55	dBFS
NPR	45	Notch centered on 50 MHz and 350 MHz, notch width 500 KHz on 20 MHz-700 MHz band, at Fc = 1.5 GHz at optimum loading factor of -13.1 dBFS	44	dB
jitter	200	ADC internal clock jitter noise at Fc = 1.5 GHz	200	fs rms
Radiation ionizing total dose	>100		110Krad(Si)	Krad (Si)
Latch up free (SEL)	>80		>80	MeV-cm²/mg
SEE	1E-03 to 1E-02	Geosynchronous orbit	1E-03 to 1E-02	SEU/device.day
SEFI (Single event Functional Interrupt)	>100 years	Recoverable with Reset	>100 years	MTBF

Permanent conversion errors	>100 years	Recoverable with Reset	>100 years	MTBF
Multi conversion errors	>1 year	Self-recovering	>1 year	MTBF
Single conversion errors	>1 day	Self-recovering	>1 day	MTBF
Operating Temperature Range	-55°C<T_C T_J <125°C	For functionality	-55°C<T_C T_J <125°C	°C
Operating Temperature Range	-20°C<T_C T_J <125°C	For performance	-20°C<T_C T_J <110°C	°C
Life Time	>20		20 years	Years

<u>Task1.2 & task 1.3: Design of the ADC</u>

The architecture of the ADC is briefly described in the figure below.

figure 1. High frequency ADC simplified architecture



Legend:
Pre-Amp = Pre-amplifier
Post-Amp = Post-amplifier
T/H = Track and hold

<u>There are five main blocks</u>:

A) Front-End Track and Hold

The goal of this cell is to make a high frequency analogue sampling.
This block gives limitation in noise or SNR coming from thermal noise (KT/C noise) of components and jitter noise coming from clocks. It gives also the limitations in spurious dynamic range against clock (internal settling time limitations versus clock frequency) and analogue frequency. In addition, the pre-amplifier is crucial because it needs to present constant impedance at the input of the ADC so that external filtering at the input of the ADC is made possible.
This block in combination with high frequency package modelling gives the -3dB full power bandwidth. This block is the most critical one because large switching current that are created internally, could lead to ringing effects limiting the dynamic performances.

B) Analogue core: folding and interpolation architecture.

Thanks to folding with interpolation technique, the size of such core is drastically reduced compared to standard flash ADC. The core is based mainly on three cascade folding amplifier creating each what is called coarse bit 2 bit so a total of 6 bit are easily created. The missing 4 bits are generated at the final folding stage.
This resulting architecture features a very good optimization of analogue input capacitance as seen by the output Track/hold which allows a good capability to drive the load at such high clock frequency. For instance in our case instead of the 1023 input comparators needed in the standard flash ADC only 25 comparators were used. The most important stage is the first folder which is correlated to the targeted INL (or Static THD). Integrated Non Linearity is given by the mismatching of NPN (and in second order of magnitude the load resistance) of the input comparator in correlation with the internal analogue full range of the analogue core. The better the matching coefficient of the process is, the lower has to be the size of input capacitance and power dissipation of the first input comparator.
Another issue for the analogue core is the settling time limitation against clock frequency.
Due to the track and hold architecture, the available analogue data is stable during half a period clock. The analogue core (and first latch of the digital part) has to be settled during this half clock period.

C) Input Clock Buffer:

This cell is important because it has great impact on the internal clock jitter of the ADC and also is used for the optimisation of different timing inside the ADC.
The ADC jitter noise comes from the equivalent input voltage source (we neglect the input current as low output impedance is considered) dividing by the input slew rate at clock transition.

To lower the jitter the number of cell should be limited (min 2 to 3) and the swing internally increased. Using a process with low parasitical base resistance and high fT helps to decrease the loss in jitter. The impact of jitter at high frequency could limit the effective number of achievable bit.

D) Digital Part

In terms of criticity, this part is mainly concerned with the BER (Bit Error Rate) and clock speed limitation coming from instance from error in digital decoding.
The BER is mainly coming by the bandwidth limitations of the first array of latches directly loaded on the last analogue part.
To overcome this limitation extra row of pipelined Master slave latch have been added to reduce despite the drawback is an extra power dissipation. Thanks the large peak fT of the process, the extra power dissipation is however limited with an acceptable BER.

This phase has benefited of outcome of the 1st development in partnership with ESA TRP contract in collaboration with the same partners as CNES, Thalès Alenia Space and EADS ASTRIUM with a first silicon results that have proven the architecture choice with the B7HF200 technology.
However, few optimisations remained necessary to improve the robustness of the design for the space operation. Robustness improvement and performances optimisations is however not a straightforward tasks.

The main optimisations were to improve

- Performances versus temperature versus power supplies
  - High temperature Performances rolloff (SNR,THD,SFDR) above Tj > 90degC
  - Performances roll off versus VCCA3 (SNR,THD,SFDR)
  - INL figures that limits the SFDR.

- Timing
  - Notch in frequencies between 800MSPS and 1200MSPS in demux 1:2 and demux 1:4
  - Maximum sampling frequency in demux 1:1 too low

- Functionalities
  - Out of range coding (under flow over flow)
  - Dynamic Built In Test pattern in demux 1:1 (datas twice slower).
- Others
  - ESD (750V) on Clock input Buffer

Task 1.4 Chip manufacturing

The chip is manufactured with B7HF200 silicon technology licensed by Infineon (part of the consortium) in Germany.

This technology features above 200 GHz (peak fT) Heterojunction bipolar Transistor in SiGeC (SiGe + Carbon). Those transistors are 100 % vertical isolated NPN Transistors that ensure natively a good protection to radiation effects

figure 2. Cross section of the Heterojunction bipolar Transistor in SiGeC .

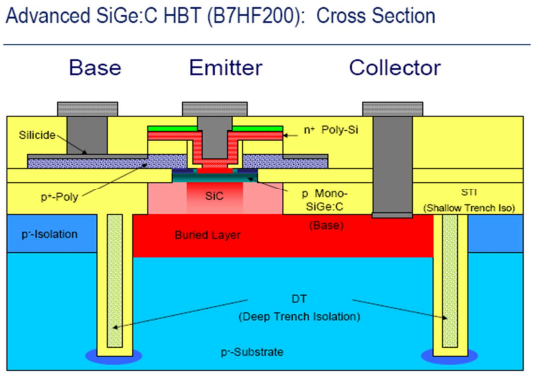
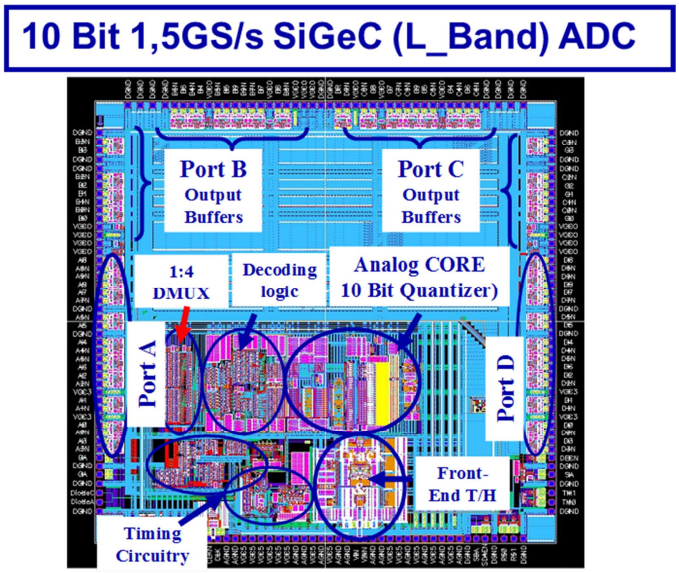


figure 3. Top layout of the 10b ADC



Task 1.6 : Assembly of the 10-bit ADC

The chip is assembled in a customized 255 pin ceramic and hermetic package with solder column interposer. The assembly is performed by e2v.

figure 4. Pictures of the 10b ADC assembled in the ceramic package

See WP3 for more details on the assembly process.

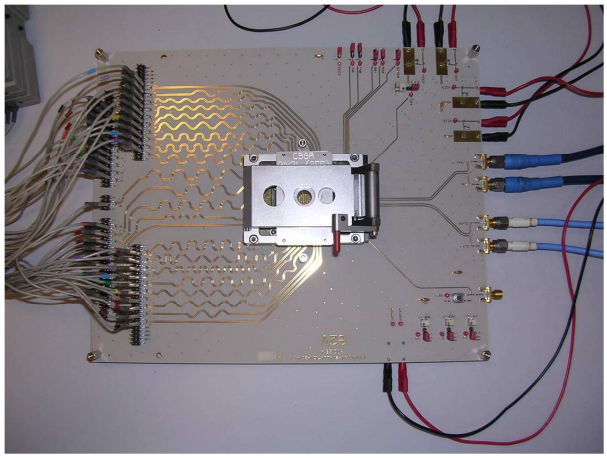
1.3.2 WP2: ADC 10-bit / 1.5 Gsps Characterisation

Objectives:

- Electrical Validation & characterisation of the 10b ADC
- Evaluation of the 10b ADC by the End-users

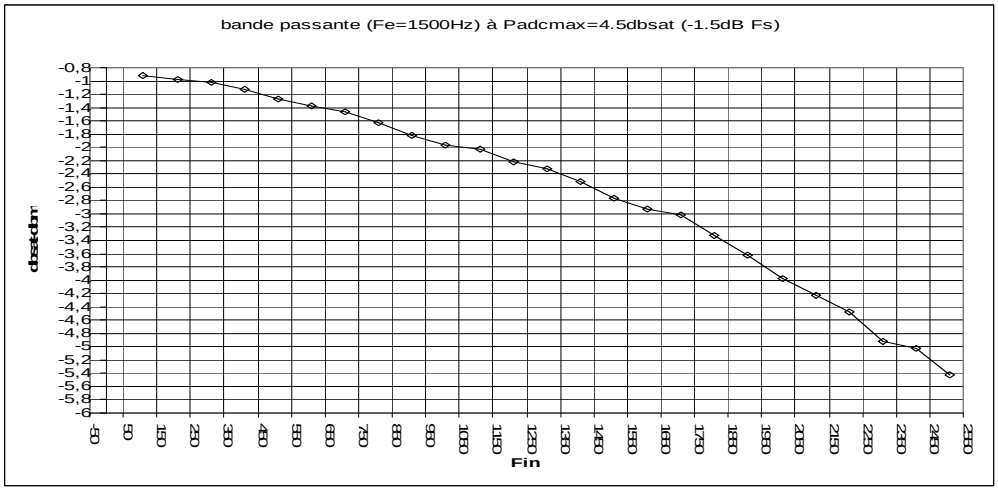
10b ADC (EV10AS180AGS) have been characterized by e2v, TAS and EADS ASTRIUM on evaluation board are summarized in the graphs below on the evaluation board and according the strategy defined in the task2.1

figure 5. Picture of the evaluation board with the dedicated socket.



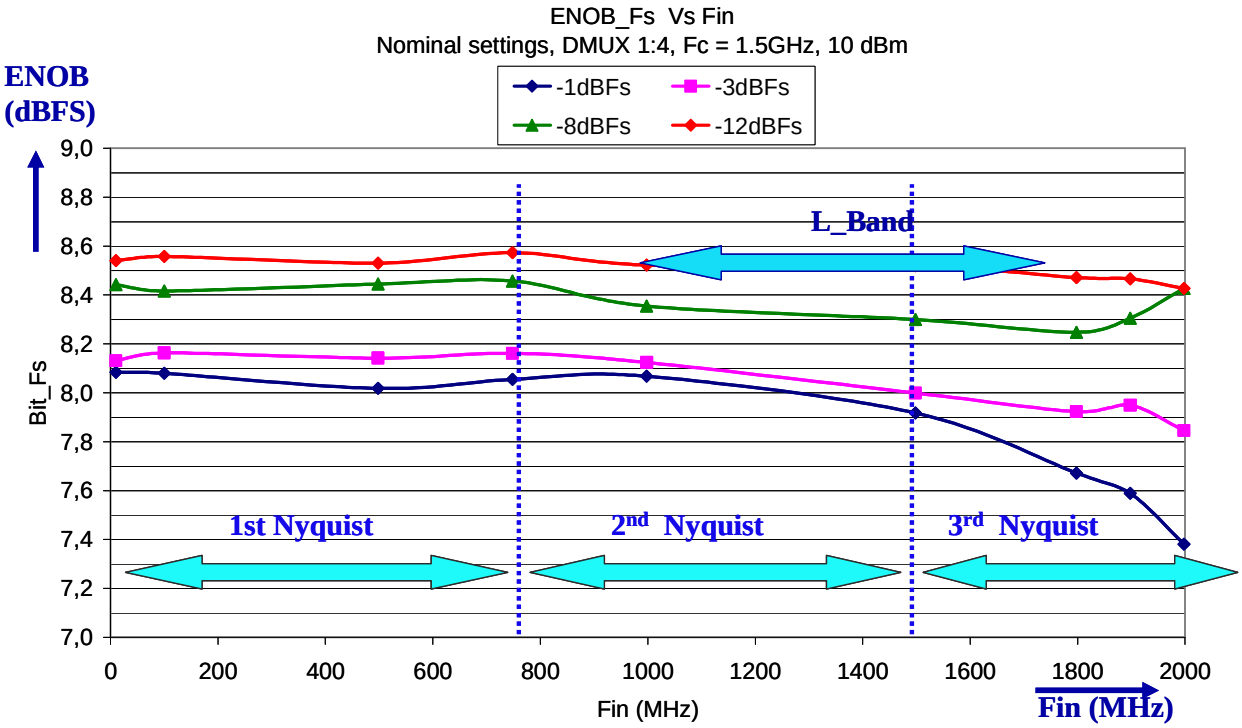
Main results of the characterization performed by by e2v, TAS and EADS ASTRIUM on evaluation board are summarized in the graph below.

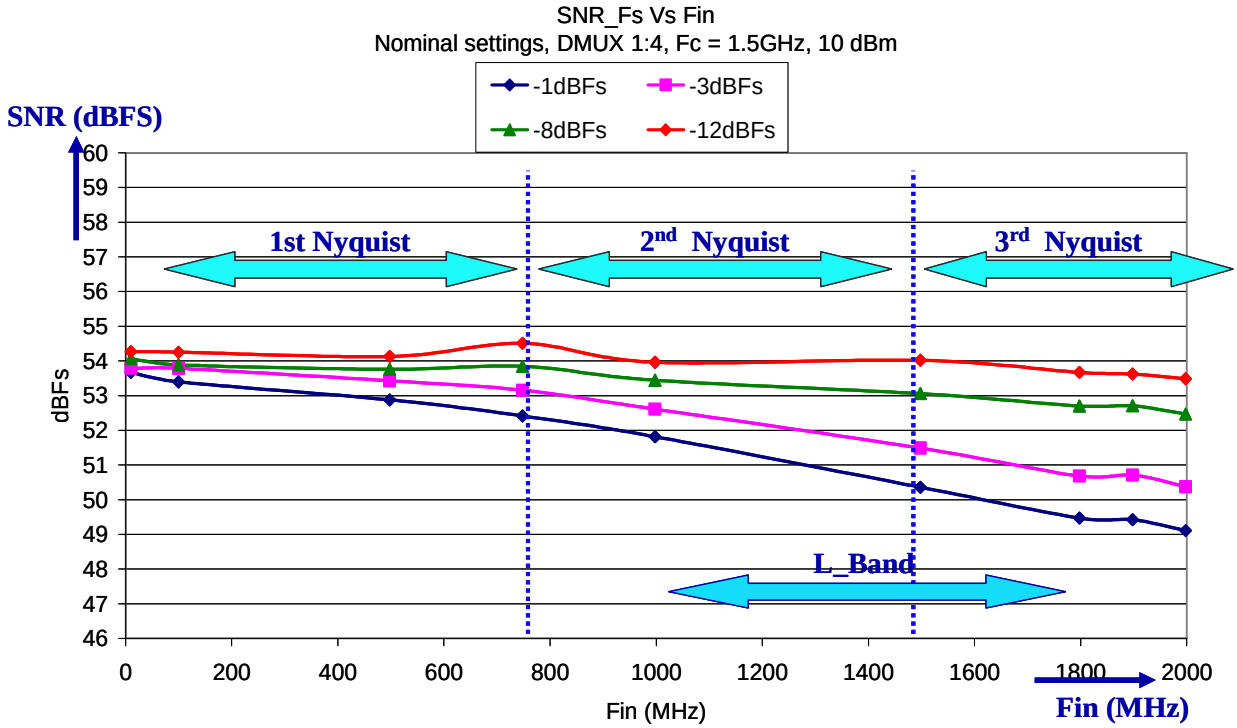
figure 6. Input bandwidth @Fs=1.5GSps

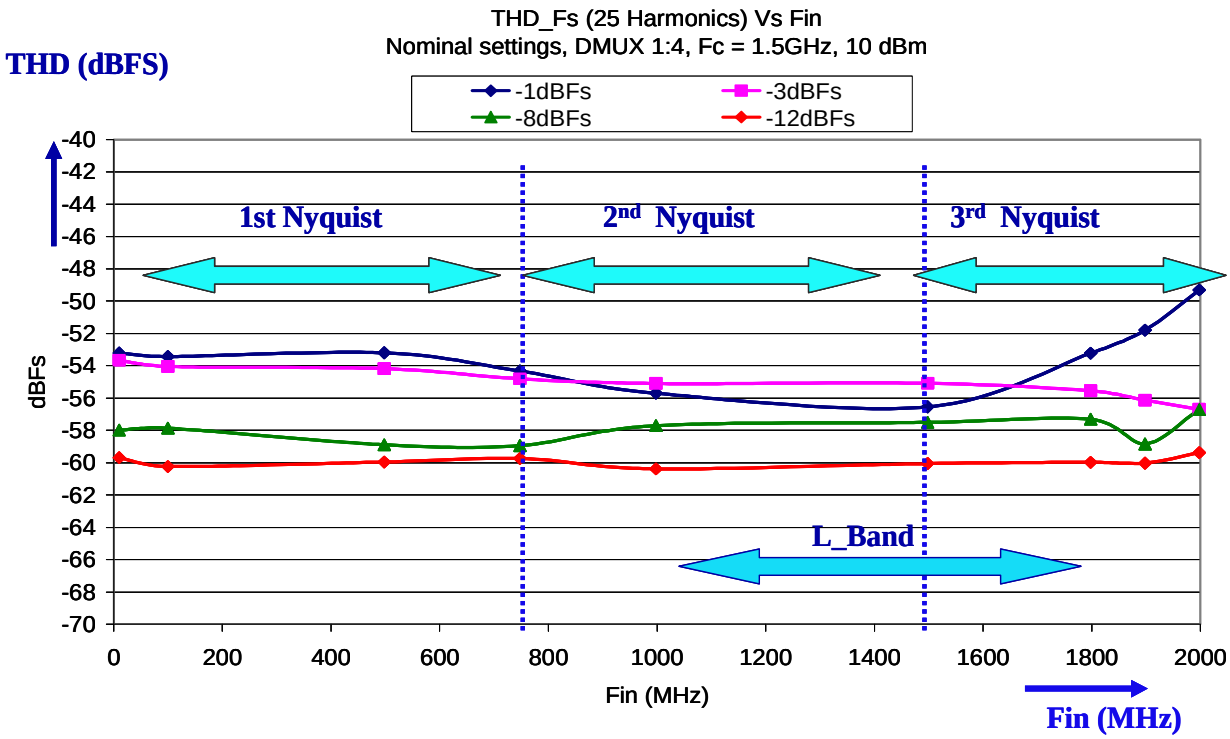


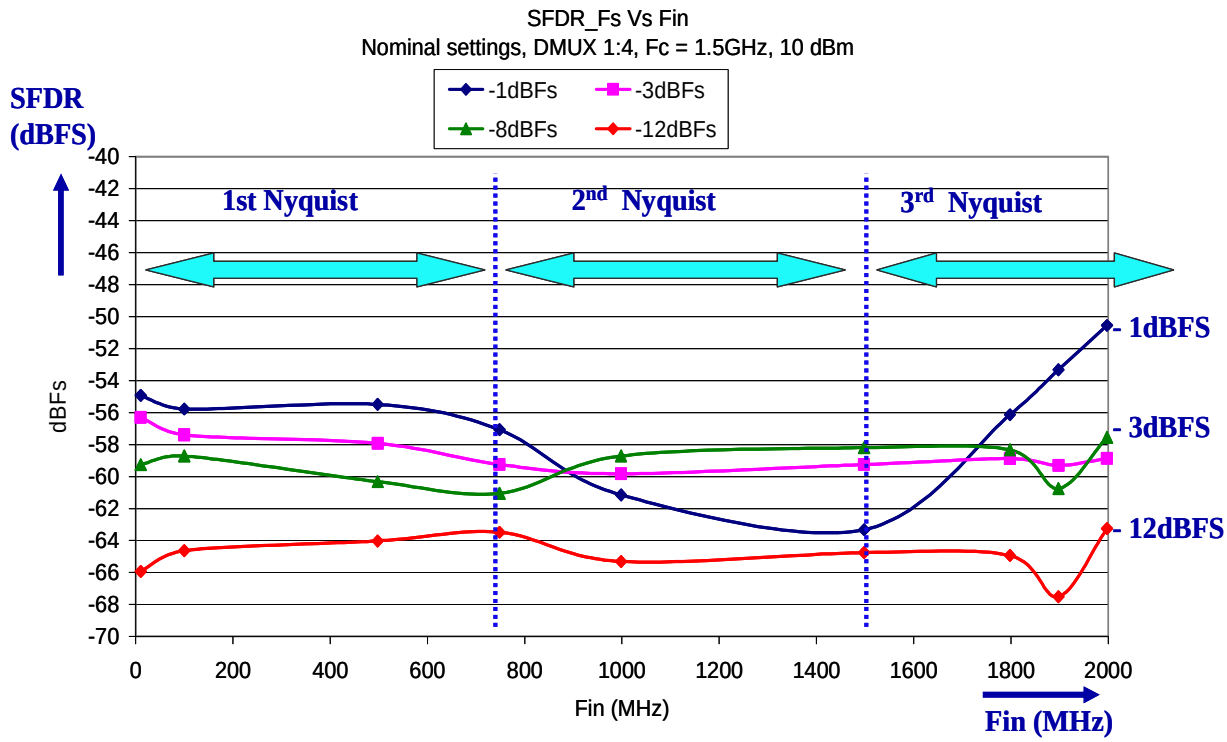
The global attenuation from 10MHz up to 2.5GHz, is 5dB with a slope of around 0.2dB/100MHz

figure 7. singles tone FFT Computation versus Fin @ 1.5GSps



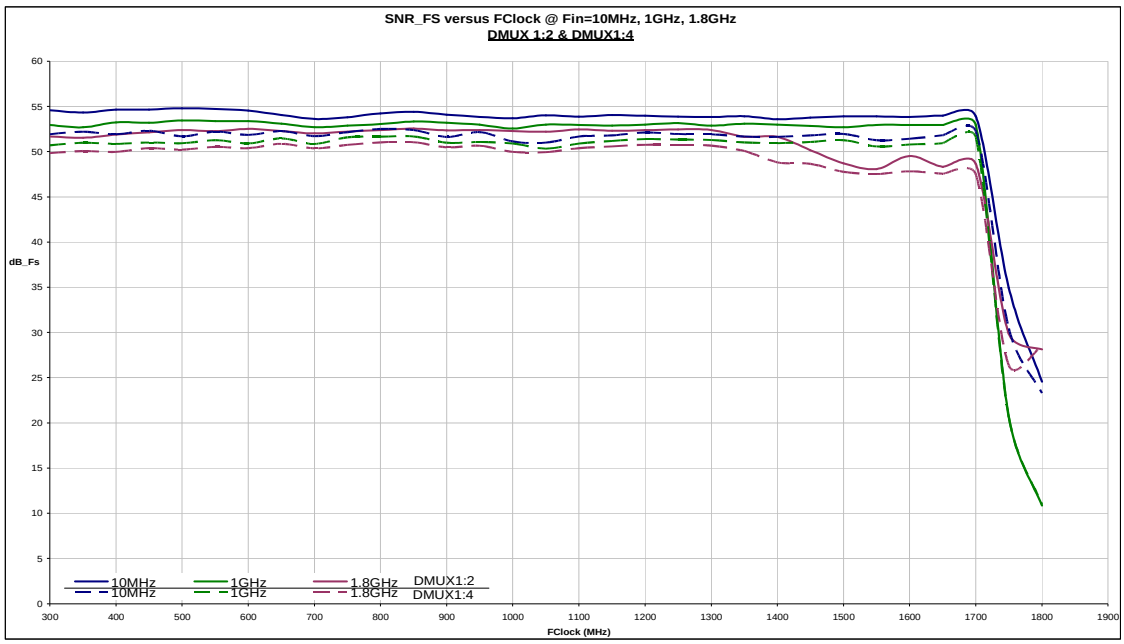


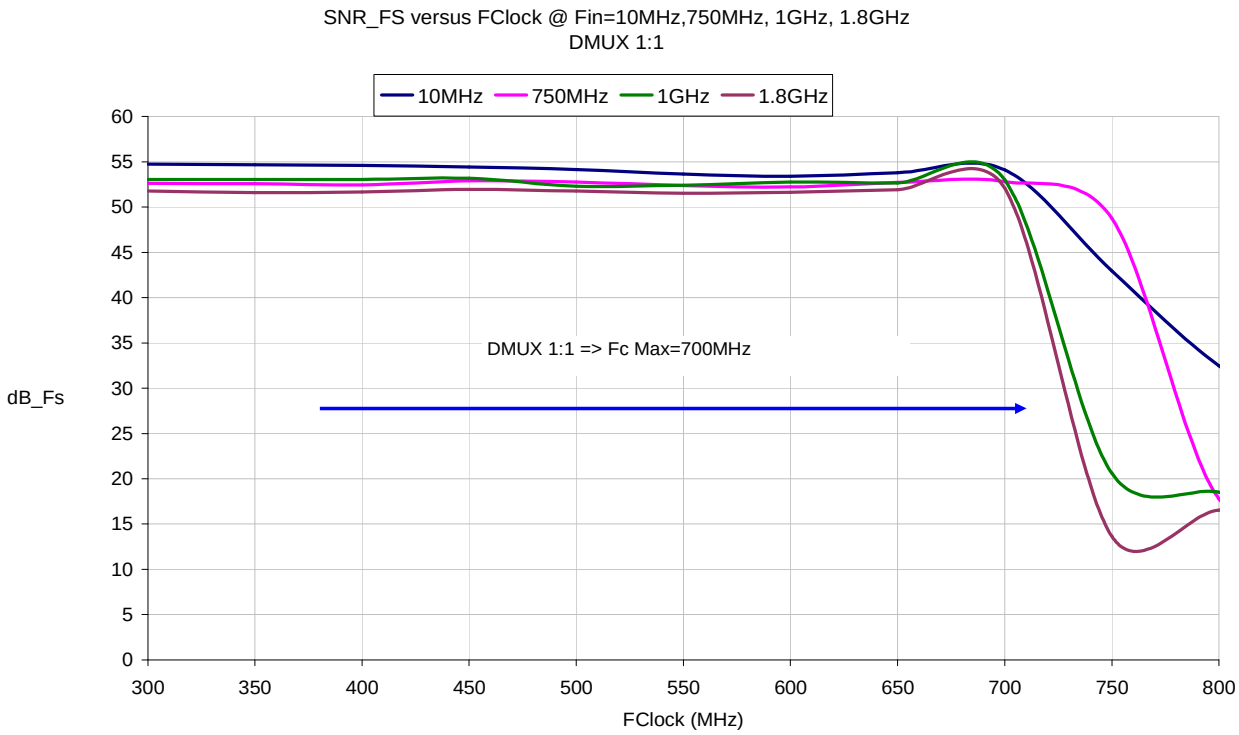

THD_Fs (25 Harmonics) Vs Fin
Nominal settings, DMUX 1:4, Fc = 1.5GHz, 10 dBm
THD (dBFS)
-1dBFs
-3dBFs
-8dBFs
-12dBFs
1st Nyquist
2nd Nyquist
3rd Nyquist
L_Band
dBFs
Fin (MHz)
Fin (MHz)


SFDR_Fs Vs Fin
Nominal settings, DMUX 1:4, Fc = 1.5GHz, 10 dBm
SFDR (dBFS)
-1dBFs
-3dBFs
-8dBFs
-12dBFs
1st Nyquist
2nd Nyquist
3rd Nyquist
- 1dBFS
- 3dBFS
- 12dBFS
dBFs
Fin (MHz)
Fin (MHz)

The single tone performances are almost independent of the input frequency - Fin (around 8.6 bits for -12dbFs).
The spurious and harmonics are not very sensitive to input frequency (SFDR around 65 dBFs)
Performances (Signal to Noise ratio) are stable versus sampling frequency

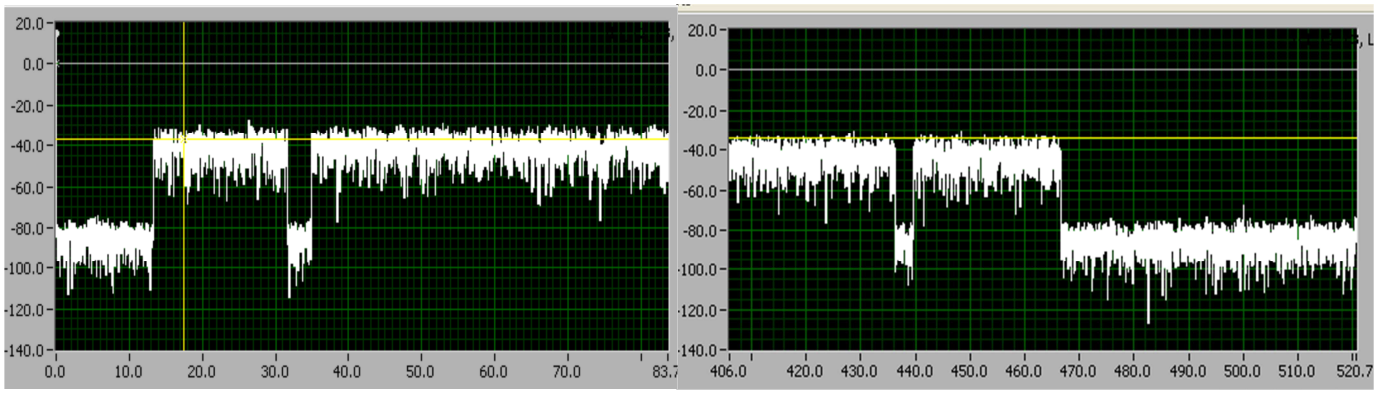
figure 8. single tone FFT Computation versus Fs





Broadband performances,

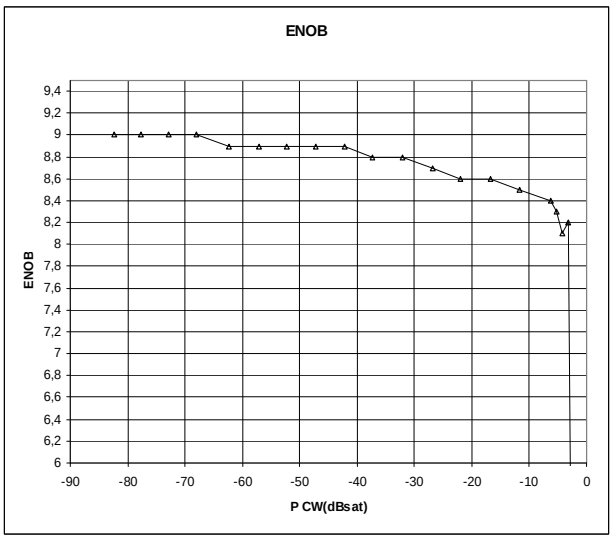
figure 9. 1,5GSps 1st Nyquist NPR(Noise Power Ratio) at Optimum loading factor -13 dBFS (450 MHz Pattern, 5MHz Notch around 33MHz & 438MHz : NPR = 44 dB)

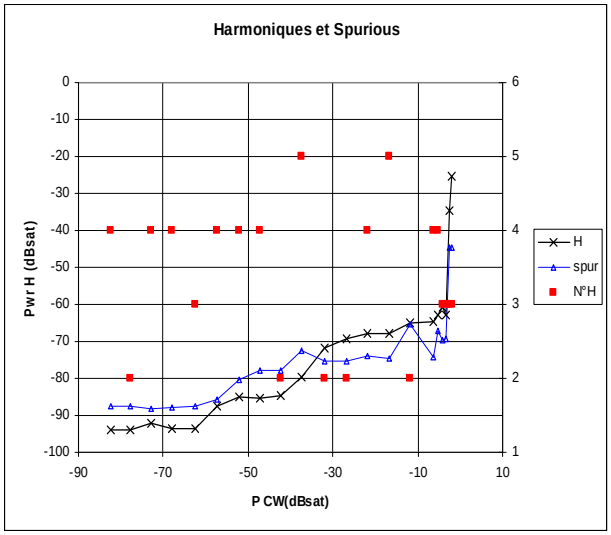


Evaluation 10 bits ADC through dedicated board by TAS

The dedicated bread board representative of final application has been developed in order to check that it has no impact on the performance.

figure 10. FFT performances dedicated board by TAS





In a more representative context, the performances remain the same and the EV10AS180A is very easy to use.

Conclusions

Performances are compliant with the specifications.

1.3.3 WP3: ADC 10-bit / 1.5 Gsps ESCC Evaluation

Objective

- ESCC evaluation of the 10b/1.5 GSps ADC Designed in STEP1 according to ESCC2269000
- To introduce ADC in EPPL and use it in space programs

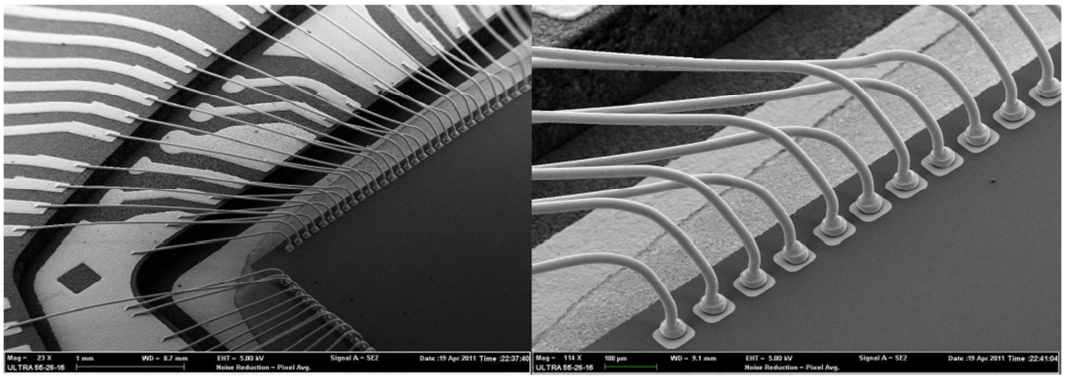
Task 3.0: Industrial means & Device qualification by e2v

This task consists to develop and validate the industrialization means:

- Automatic testing on Teradyne ATE
- Material for Burn-in & qualification - ATE dedicated test interface
- Probe card for wafer testing
- Package test board
- Writing, debug & validation of test programs (Wafer & package)
- Correlation with characterization data
- Burn-in Boards

In parallel the ball gold bonding process on gold pad from B7HF200 technology with ceramic BGA package (picture below) have been qualified by e2v.

figure 11. Picture of the ball bonding to the die



Task 3.1 : Evaluation test plan (construction analysis, screening, life test…)

The evaluation test plan (ref. NE 31S 207330revA) has been elaborated by CNES and e2v according the ESCC226900 specification.(EVALUATION TEST PROGRAMME FOR MONOLITHIC INTEGRATED CIRCUITS ESCC Basic Specification No. 2269000 of Oct 2002.

It includes all tests which results are summarized in the next paragraph.

Task 3.2 : Evaluation test (construction analysis, screening, life test…)

Below the main step of manufacturing flow of the device (based on the ESCC9000 Chart F3 screening)

Main steps description:

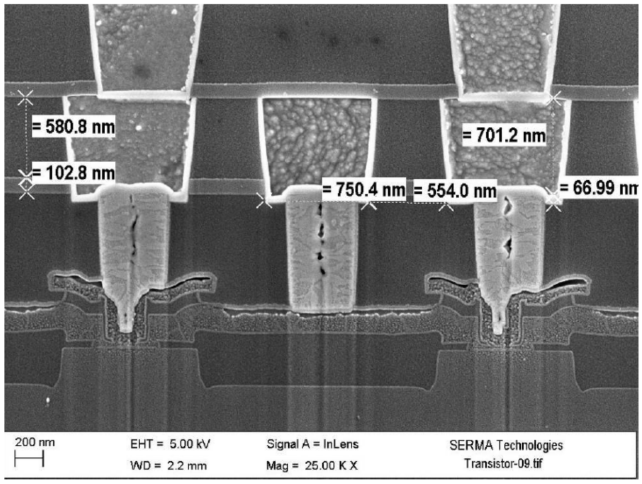
Die attach
Wires bonding
e2v Internal inspection
Customer internal source inspection → Delegated to e2v quality inspector
Sealing
Marking + Serial
Pind-test
Pre-ambient temperature measurements
Pre-High & Low temp measurement
Deduction for test gold samples
Burn-in
Post-ambient temperature measurements
Drift calculation
High & Low temp measurements
PDA calculation
SCI attach
Xray control
Fine & Gross link
Final ambient electrical measurements
Dimensional measurements
Mass measurement
External visual inspection
Customer final source inspection

(The final source inspection has been performed in collaboration with CNES)

1. Construction analysis (ESCC2269000- Subgroup 2C) :
   a. SEM analysis

The SEM analysis concludes that EV10AS180AGS product mask VN41A is compliant with Infineon B7HF200 specification

figure 12. PSEM cross section of the die



b. Internal vapor contents

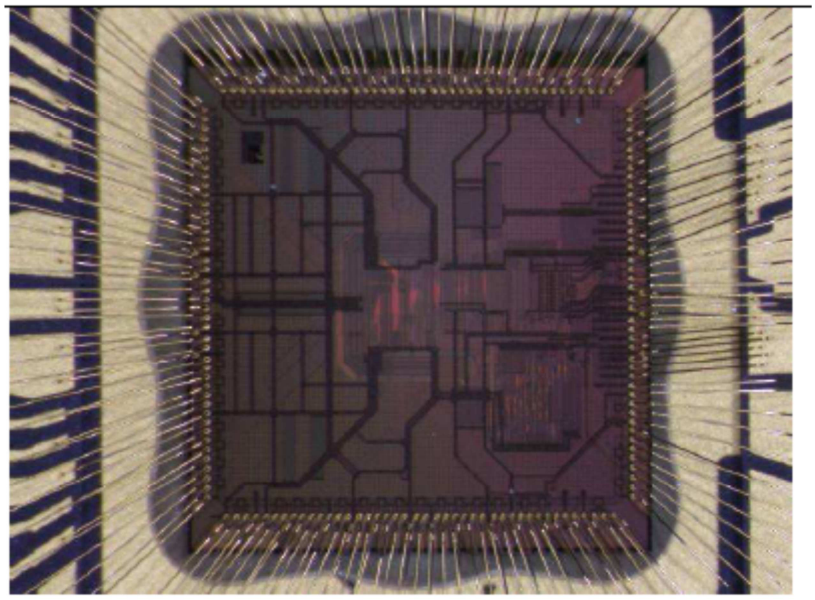
Internal water vapor content on 3 devices issued from assembly lot ID: 9971861 / DC: 1130 / Product: EV10AS180AMGS9NB1

TEST Acceptable criteria	METHOD Condition	Sample	Humidity Result	Status
Internal water vapour content < 5000 ppm	MIL-STD-883 TM1018 Procedure 1	3	346 ppm 279 ppm 325 ppm	Pass

c. Backend construction analysis performed by CNES

The construction analysis have been performed by the CNES on the EV12DS130AGS device which is 100% similar (in term of manufacturing) with the EV10AS180AGS (10b ADC) as the devices share the same package, same technology.

figure 13. Picture of chip in its package with wire bonding



Conclusion of the destructive physical analysis did not show abnormalities in the device.

2. <u>Package Evaluation (ESCC2269000- Subgroup 2D) :</u>

The package evaluation have been performed on the EV12DS130AGS by similarity

Done by similarity with: 12bit 3Gsps Muxdac → Same Package / same assembly process see report *NE 31S 207330*				
TEST Acceptable criteria	METHOD Condition	Sample	Fail	Status
Environmental tests Temperature cycling Fines et grosses leaks Thermal shock Fines et grosses leaks Temperature cycling Fines et grosses leaks External Visual Inspection Electrical test	 MIL-STD-883 TM 1010 cond C **100cy** +150°C/-65°C MIL-STD-883 TM1014 cond A & C MIL-STD-883 TM 1011 cond C **100cy** +150°C/-65°C MIL-STD-883 TM1014 cond A & C MIL-STD-883 TM 1010 cond C **400cy** +150°C/-65°C MIL-STD-883 TM1014 cond A & C ESA SCC 20500 ATE program	6	0	Pass
Mechanical tests Mechanical shock Fines & grosses leaks Vibration Fines & grosses leaks Mechanical shock Fines & grosses leaks Vibration Fines et grosses leaks External Visual Inspection Electrical test	 MIL-STD-883 TM 2002 cond B. **5**x(6 axis : pulse duration 0.5 ms/1500 g) MIL-STD-883 TM1014 cond A & C MIL-STD-883 TM 2007 cond A **12**x(3 axis: 20 to 2000 Htz/20 G/4 min mini) MIL-STD-883 TM1014 cond A & C MIL-STD-883 TM 2002 cond B. **45**x(6 axis : pulse duration 0.5 ms/1500 g) MIL-STD-883 TM1014 cond A & C MIL-STD-883 TM 2007 cond A **108**x(3 axis:20 to 2000 Htz/20 G/4 min mini) MIL-STD-883 TM1014 cond A & C ESA SCC 20500 ATE program	6	0	Pass
Reflow simulation Reflow simulation Fines et grosses leaks Reflow simulation Fines et grosses leaks External Visual Inspection Electrical test	 J-STD-020D **3** x SnPb Eutetic profil peak > 220°C MIL-STD-883 TM1014 cond A & C J-STD-020D **2** x SnPb Eutetic profil peak > 220°C MIL-STD-883 TM1014 cond A & C ESA SCC 20500 ATE program	6	0	Pass
Internal water vapor contents	MIL-STD-883 TM 1018 Humidity < 5000ppm	3	0	Pass
Solderability test (wetability) External Visual Inspection	 RD21S205279 e2v internal procedure / ESA SCC 20500	3	0	Pass

Conclusions:
EV10AS180AMGS9NB1 product has passed with success subgroup 2D - Mechanical tests -by similarity with EV12DS130AMGS9NB1 product.

3. Endurance test (ESCC2269000- Subgroup 3B et 3C) :

High Temperature Operating Life					
Step	Test	Method	Condition	CA / CR	Fail / Ok
1	Electrical test	Prog: EV10AS180A	Ambient, Low and High temperatures	45 / 0	Pass
2	Ext.Visual insp.	ESCC 20500	-	45 / 0	Pass
3	Burn-In	MIL-STD-883 TM1005	Screening Burn-In (done 460 Hrs) Tj = 165°C / SP.31S.203844	45 / 0	-
4	Electrical test	Prog: EV10AS180A	Ambient, Low and High temperatures	45 / 0	Pass
5	Ext.Visual insp.	ESCC 20500	-	45 / 0	Pass
6	HTOL	MIL-STD-883 TM1005	0H to 500H Tj = 165°C / SP.31S.203844	15 / 0	-
7	Electrical test	Prog: EV10AS180A	Ambient, Low and High temperatures	15 / 0	Pass
8	Ext.Visual insp.	ESCC 20500	-	15 / 0	Pass
9	HTOL	MIL-STD-883 TM1005	500Hrs to 1000H Tj = 165°C / SP.31S.203844	15* / -	-
10	Electrical test	Prog: EV10AS180A	Ambient, Low and High temperatures	15 / -	Pass
11	Ext.Visual insp.	ESCC 20500	-	15 / -	Pass
12	HTOL	MIL-STD-883 TM1005	1000Hrs to 1500H Tj = 165°C / SP.31S.203844	15 / -	-
13	Electrical test	Prog: EV10AS180A	Ambient, Low and High temperatures	15 / -	Pass
14	Ext.Visual insp.	ESCC 20500	-	15 / -	Pass
15	HTOL	MIL-STD-883 TM1005	1500Hrs to 2000H Tj = 165°C / SP.31S.203844	15 / -	-
16	Electrical test	Prog: EV10AS180A	Ambient, Low and High temperatures	15 / -	Pass
17	Ext.Visual insp.	ESCC 20500	-	15 / -	Pass

Conclusions:
EV10AS180AMGS9NB1 product has passed with success 2000Hrs life test (Tj 165°C)
Using accumulation component hours of all life test done on B7HF200 technology, we obtain 140 FIT at operating Tj = 110°C

Task 3.3 Radiation assessment

- Heavy ions tests completed, Report TRAD/TI/EV10A/XXX2/E2V/ELG/1106 rev.2 :
  - No SEL at 125degC up to a LET of 80 MeV-cm²/mg (with a tilt) and up to 67.7 MeV-cm²/mg (without tilt)
  - No SEFI. No permanent error .
  - Low SEE LET threshold of 0.7 to 1.6 MeV.cm²/mg
  - SEE saturated cross-section in the range of 3.8E-5 to 2.1 E-04 cm²
  - Worst case long SEU/SET duration is 48 consecutive corrupted data

→ For a geostationary satellite:

- SEE rate of 2.48E-04 to 8.24E-02/device.day
- Worst case Multiconversion errors is 1.27E-02/device/day (MTBF > 78 days)
- Worst case Single conversion errors 8.24E-02/device.day (MTBF > 12 days)

- Protons tests completed. Report TRAD_TP_EV10A_XXX1_E2V_ELG_1111_Rev1:
  - No SEL up to 184MeV
  - No SEFI . No permanent error.
  - Very few SEE were detected with proton tests even if the device appears to be sensitive down to the 20MeV Energy. Saturated cross-section in the range of 1E-10 to 1.3E-09 cm²
  - Worst case long SEU/SET duration is 5 consecutive corrupted data

→ For a geostationary satellite:

- SEE of 4.47E-05 to 7.83E-03/device.day
- Worst case Multiconversion errors is 1.16E-03/device/day (MTBF> 862 days)
- Worst case Single conversion errors of 7.83E-03/device.day (MTBF>127 days)

- Total Ionizing Dose tests completed, Report NE 31S 207917 rev.B
  - The EV10AS180A ADC was tested up to 110 krads(Si) with a very low dose rate of 36 rad (Si)/h. It was concluded that the EV10AS180A ADC had neither functional failure nor parameter drift up to 110 Krad (Si). Static and Dynamic results were satisfactory for all parameters.

- Analysis of the data collected during irradiation experiments completed, report ref. NE 31S 208018 issue A "EV10AS180A : 10-bit 1.5 Gsps ADC Radiation test report Infineon B7HF200 E2V"

Results from TID test, Heavy ions test and Protons test demonstrate the suitability for operating EV10AS180A ADC in space environment. All the results were synthesized in table below:

Parameter	Symbol	Results	Unit	Comments
Radiation total dose	TID	110	Krad	No issue
Latch up free	SEL	> 80	MeV-cm²/mg	No SEL at 184MeV with protons
SEFI (Single event Functional Interrupt) - Recoverable with Reset	SEFI	NO SEFI		
Permanent conversion errors - Recoverable with Reset		No permanent error		
HEAVY IONS				
LET threshold	LETth	0.7 to 1.6	MeV	Depending on the pattern

Parameter	Symbol	Results	Unit	Comments
Saturated cross-section	Xsat	3.8E-05 to 2.1E-04	Cm²	Depending on the pattern
Long SEU/SET duration	Long SEU	< 48	consecutive corrupted data	48 consecutive data for dynamic tests 44 consecutive data for static tests
SEE performance for a geostationary satellite				
SEE performance	SEE	2.48E-04 to 8.24E-02	SEU/device.day	Depending on the pattern
Multi conversion errors (self recovering)		1.27E-02 / Device.day (>78 days)	MTBF	Worst case obtained for static tests $01F at 600Msps Better results with dynamic tests at 600Msps: 1.82 E-02 (55 days)
Single conversion errors (self recovering)		8.24E-02 (12 days)	MTBF	Worst case obtained for static tests $20F at 00Msps Better results with dynamic tests at 600Msps: 1.82 E-02 (5 days)
PROTONS				
Energy threshold	Eth	< 20	MeV	
Saturated cross-section	Xsat	1E-10 to 1.3E-09	Cm²	Depending on the pattern
Long SEU/SET duration	Long SEU	< 5	consecutive corrupted data	
SEE performance for a geostationary satellite				
SEE performance	SEE	4.47E-05 to 7.83E-03	SEU/device.day	Depending on the pattern
Multi conversion errors (self recovering)		1.16E-03 / Device.day (>862 days)	MTBF	
Single conversion errors (self recovering)		7.83E-03 (127 days)	MTBF	

Task 3.4 Results synthesis and introduction in EPPL

- Redaction of the PID is completed (reference NE31S209406)
- Redaction of the detail specification completed (reference NE31S209260)
- Redaction of the synthesis report completed=> (reference NE31S209206)

CONCLUSIONS:

The product has passed with success all tests as defined in test plan ref: NE 31S 207330 and evaluation test programme for monolithic Integrated circuits ref: ESCC N°2269000.
Results from this evaluation demonstrate the suitability of EV10AS180A ADC product for operation in space environment.

1.3.4 WP4: Advanced device modelling and New Devices

Work package 4 has been dedicated to advanced modelling and characterization efforts to support the realization of the challenging circuit applications of this project. This included exhaustive noise characterizations at low and high frequencies, intensive thermal characterization, and investigations/modelling of the transistors beyond the limits of their typical operating range, e.g. near breakdown voltages. Furthermore several additional device options have been investigated to improve the usage of the high-speed bipolar process for the targeted high-end applications.

Three of the COMETs partners have been involved in this work package: CNRS with its advanced characterization laboratories IEMN and XLIM; Infineon as the supplier of the semiconductor technology; and e2v as the designer of the high-performance ADCs.

To meet the objectives of work package 4 the work was split into three tasks: Task 4.1, advanced device modelling, task 4.2, advanced device characterization, and task 4.3, new devices. In this section an overview of the main results is given.

As a base for characterization and modelling samples of a large variety of the high-speed npn SiGe heterojunction bipolar transistors and of the vertical pnp bipolar transistors have been prepared by Infineon and have been delivered to the CNRS laboratories IEMN and XLIM. DC and high frequency S parameter measurements in extended operating regimes (including saturation and high current regimes) have been carried out on these samples.

Extensive speed and especially high-frequency noise characteristics of the npn transistors have been measured by IEMN. The very comprehensive characterization over a large frequency and bias range allowed the extraction of iso-curves for transit frequency fT, maximum oscillation frequency fmax, and minimum noise figure NFmin. This enables the circuit designer to select optimized bias points for low noise, low power, or high gain operation. This extensive characterization work has been described in detail in appendix A2.1 of deliverable report D4.2 by IEMN.

A sophisticated thermal measurement setup has been used to achieve microscopic thermal measurements of npn transistors under realistic bias conditions and to validate electrical measurements of the thermal resistance.

The characterization of the pnp transistors at XLIM led to the extraction of new models, extending the possible usage of the pnps to their speed limit.

In the second half of the project XLIM used comprehensive characterization of the npn transistors to extract advanced models for these devices, including previously not covered effects like current gain decrease at high collector currents, accurate cut-off frequency modelling at saturation, breakdown behaviour and self-heating effects. These models were provided to Infineon and e2v in Verilog format. This work is described in great detail in appendix A2.2 of deliverable report D4.5.

Regarding new devices a resistive device has been introduced into the production process and has been included in the process design kit as an additional wiring option and to provide a “damping resistor” to reduce the risk of instability and ringing problems. Furthermore devices for integrated injection logic have been realized as an attractive option for saving area and lowering power consumption. First circuits have been fabricated to prove functionality of the new devices on circuit level.
Extensive low-frequency noise characterization of the npn and pnp transistors, and of the polysilicon resistors has been done. This led to improved low-frequency noise models of the npn transistors and

of the resistors, and to the first low-frequency noise models of the B7HF200 pnp transistors. The progress achieved by these new noise models is demonstrated by the application example of an operational amplifier. Especially the new noise models for the pnp transistors have been important, because these devices are now more and more used in various key building blocks, and have been also evaluated for the ADCs. For the same reason additionally Monte-Carlo parameters for the pnp transistors have been determined.

Moreover e2v designers have found that increasing the voltage swing for the 12 bit ADC design, as it would be beneficial for increasing resolution, has a negative impact on ADC characteristics ("curve bends" in the INL characteristics). It was suspected that operation of the high speed npn transistors close to avalanche breakdown was the cause of this issue. Therefore the carrier multiplication factor due to the avalanche effect was characterized and included in the models of the high speed transistors. This was very beneficial to investigate and verify by e2v the experimentally found circuit characteristics.
The above mentioned limitation of the usable voltage swing triggered first investigations towards a new npn type. B7HF200 offers a high speed npn with a thin epitaxial collector layer and a specific selectively implanted collector (SIC) providing a BVCE0 of 1.7 V and an fT of 170 GHz, and a high voltage npn with a thick epitaxial collector layer and a lower doped SIC providing a BVCE0 of 4 V and an fT of 35 GHz. In some stages of the ADC the low breakdown voltage of the high speed npn is a limitation, but the high voltage npn cannot be used due to the low fT. Therefore a device was fabricated based on the high speed npn transistor, but without the SIC. It was expected that such a device can offer a very interesting compromise between BVCE0 and fT. The experimental results proved this expectation: The high speed npn without SIC provided a BVCE0 of 2.4 V and a transit frequency fT around 100 GHZ. The characteristics of this new npn type have been provided to e2v for evaluation.

A further input from the ADC designers was that a fast pnp transistor would provide interesting options for ADC design. Therefore first experiments were carried out for improving pnp speed, at least for the next process generation. It was shown that a doubling of the buried layer doping still could decrease the buried layer sheet resistance by nearly a factor of two, and that the increase of the collector doping of the pnp by a factor of 2 to increase the intrinsic speed still results in sufficient breakdown voltage BVCE0 of around 9V.

Conclusions

The new developed models notably have permitted to understand and then solve the "S curve bends" in the INL characteristics that limited the performances in the first 12b ADC testchip.

A part of the work of WP4 has been presented at international conferences or in international journals:

[1] N. Waldhoff, F. Danneville, N. Rolland, P.-A. Rolland, K. Aufinger, Bias Point Optimization for Low Power / Low Noise Applications of Advanced SiGe HBT, Proc. of European Microw. Integr. Circ. Conf., EuMIC 2011, pp. 386-389.
[2] K. Aufinger, H. Knapp, S. Boguth, O. Gerasika, R. Lachner, Integrated Injection Logic in a High-Speed SiGe Bipolar Technology, Proc. of IEEE Bipolar/BiCMOS Circ. and Techn. Meeting, BCTM 2011, pp. 86-89.
[3] A. El Rafei, A. Saleh, R. Sommet, J. M. Nébus, and R. Quéré, Experimental Characterization and Modeling of the Thermal Behaviour of SiGe HBTs, IEEE Trans. Electron Devices, vol. 59, no.7, pp. 1921- 1927, July 2012.

[4] A. Saleh, A. El Rafei, T. Reveyrand, R. Sommet, J.M. Nébus, R Quéré, Compact RF non-linear electro thermal model of SiGe HBT for the design of broadband ADCs, International Journal of Microwave and Wireless Technologies, Vol. 4, Issue 06, pp. 569-578, December 2012.

1.3.5 WP5: ADC 12-bit design & prototyping

The specification for the 12b ADC has been summarized in the table below.

Parameter	Target values	Unit	Comments	Final specification
Resolution	12	bits		12b
Fsampling	1.5	Gsps	Maximum sampling clock frequency	1.5
Fin	1.5	GhZ	Effective analog bandwidth	1.8
Ain	1..2	Vpp diff	Differential analogue input	0.5
Fcut	4	GHz	-3db analogue cut off frequency	2.3
Vcc	5/3.3	V	Analogue and digital supply	5/3.3
Power	<1.9	W	Total power dissipation with DmuW1:2	3.2W
ENOB	10.5	Bits FS	Fc =1.5GHz, Fin = 750MHz, -12dBFS	9.3
SFDR	76	dBFS	Fc =1.5GHz, Fin = 750MHz, -12dBFS	69
THD	72	dBFS	Fc =1.5GHz, Fin = 750MHz, -12dBFS	64
SNR	65	dBFS	Fc =1.5GHz, Fin = 750MHz, -12dBFS	58.5
NPR	55	dB	Notch centred on 50MHz & 350MHz, notch width 500kHz on 20MHz-700MHz band at Fc = 1.5GHz at optimum loading factor	48
Jitter	50	Fs rms	ADC internal clock jitter nise at Fc =1.5GHz	50
Digital outputs	LVDS / DMUX1:2			LVDS/ DMUX1:2

e2v has developed a first test chip to better assess the reachable performances taking account the technology, architecture performances versus the risks.

This first testchip 12b ADC has been designed based on the silicon proven architecture used for the 10b ADC during the phase 1 of the project.

Silicon performances exhibited by the testchip are very encouraging while below end users expectations. Various improvements have been considered and debated with the partners. Finally e2v concludes that the reached performances on the testchip are much closed to the optimum taking account architecture, available technology and architecture.

Finally it has been decided that the way forward is the design of a stabilized 12b version based on architecture / process (B7HF200) of the 12b ADC testchip that propose a revision below initial target specification but lowering risk.

Despite the revised specification, end users (TAS and ASTRIUM) have confirmed their support within COMETS FP7

The new design also took advantage from the latest devices modelling from Infineon (WP4) to correct notably non linearity issue that was the main limiting factors.
PNP transistors have also been used in dynamic way for the first time.

Specifications are being finalized and consigned in the document SO13S208576-A (deliverable D5.5 & D5.4).

Task 5.2 Design of the 12b ADC

In order to improve the performances as well the robustness of the design , e2v designers focused .

- INL improvement at high input level using notably the new transistors models delivered by the WP4.
- Stabilization of the performance at 1.5GSps by optimizing the track and hold stage
- Introduce 2 power supplies compatibility to better fit with end users requirements: Introduction of the LVDS buffer compatible to 3.3V and 2.5V as required by ends users to limit the number of power supply to embed on application board. So that the LVDS output buffers.
- Implementation of a triple majority voting architecture in the timer cells to improve the robustness to radiation upset.
- Few modifications of the 3SWI functionalities for performances optimization. (Application adjustments)
- Performances improvements for the large input scales (ie obtain the same level of performances obtained after LUT correction).

So the first main challenge and difficulties encountered for this run were:

- Root cause understanding of INL issues of the testchip and implementation of the correction.
- Others bugs/limitations have been detected on the testchip thanks to an extended characterization.
- Thermal aspects carefully taken into account to fulfil reliability specification.
- Keeping the same power budget:
- performances improvement for large input scale
- Implementation of TMV,
- Only 2 power supplies for the same performances level.

Simulation results are then very closed from the specification.
Simulation results have been presented to partners during the CDR on the October 2nd, 2012. (Deliverables 5.3 & 5.4)

Main simulation results are summarized in the table below :

		testchip	Spec	12b ADC	
Vin	Vin	0.5	0.5	**0.5**	Vpp
Integral Non Linearity (for information only)	INL-	+/-12	+/-5	**+/-5**	LSB
Nb of ps		5/3.3/2.5	5/3.3	**5/3.3**	
Power	P_D	3.22	~3.3 (+80mW)	**~3.2 (+15mW with 2Supplies)**	W
FS = 1.5Gsps Fin = 750 MHz @-1dBFS	SFDR / (cor LUT)	54/63	65	**65**	dBFS
	SNR	57	57	**57**	
	THD	53/58	62	**62**	
	ENOB	8.3/8.9	9.0	**9.0**	
FS = 1.5Gsps Fin = 1500MHz @-1dBFS	SFDR	55/66	65	**65**	dBFS
	SNR	56	56	**56**	
	THD	54/60	62	**62**	
	ENOB	8.3/8.8	8.9	**8.9**	
FS = 1.5Gsps Fin = 750 MHz @-12dBFS	SFDR	69	69	**69**	dBFS
	SNR	58.5	58.5	**58.5**	
	THD	65	65	**64**	
	ENOB	9.3	9.3	**9.3**	
FS = 1500Gsps Fin = 1500MHz @-12dBFS	SFDR	66	66	**69**	dBFS
	SNR	58.5	58.5	**58.5**	
	THD	65	65	**64.5**	
	ENOB	9.2	9.2	**9.2**	
Functionality /features		SA, SDA, …	TMV, CA, no SA, No HSR	**TMV, CA, no SA, No HSR, ..**	

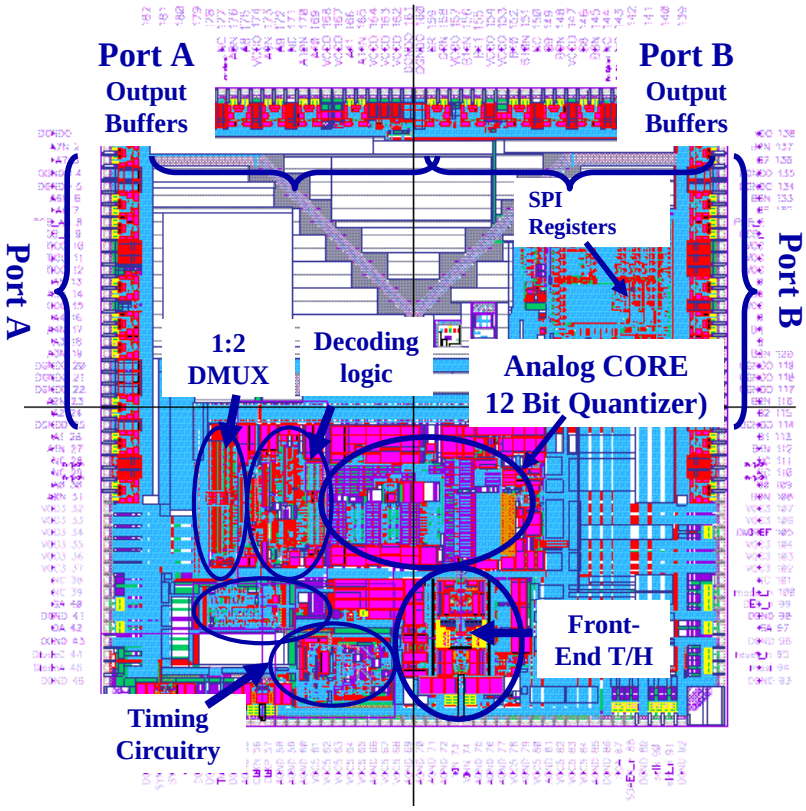
In conclusion this new revision offers

- stabilized performances @1.5Gsps with ENOB>9 @-1dBFS
- TMV on the clock paths
- implements news features to ease the application
- 2 power supplies compatibility instead of 3 for only +15mW increase.
- Clock adjust features to fine tune the performances
- Sampling delay adjust functionality improvement
- Output eye diagram improvement

Task 5.4 Manufacturing of the 12b ADC

Infineon has been in charge to manufacture the wafers that were finally delivered in April 2013. (Deliverable D5.5) in B7HF200.

figure 14. Layout of the 12b ADC



Task 5.6 Assembly of 12b ADC samples

Chips have been assembled in the CI CGA package 255 with Solder Column Interposer. (same package as the 10b ADC). Below a picture of the EV12AS200AGS device.

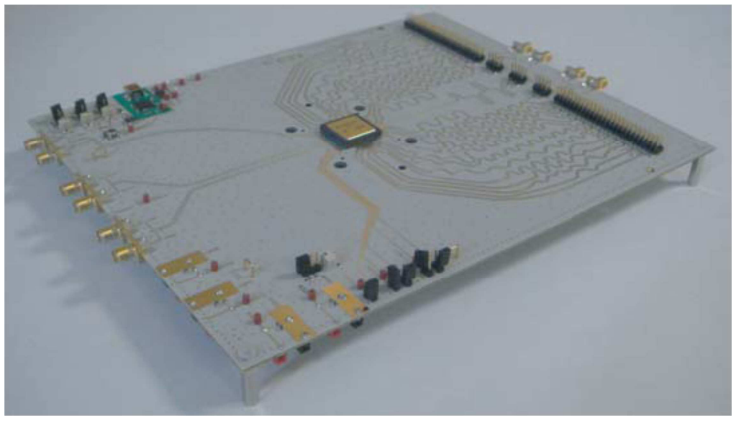
figure 15. Picture of the 12b ADC samples in CI CGA package

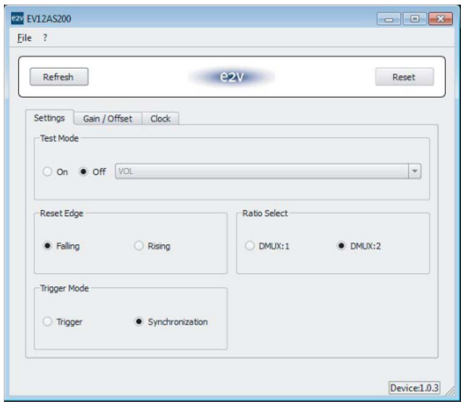
1.3.6 WP6: ADC 12-bit Validation & assessment

Task 6.1: Definition of validation strategy & means

A specific evaluation boards and user interface software have been developed.
Evaluation board are designed in order to be compatible with most of measurements equipment.

figure 16. Picture of the 12b ADC evaluation board and GUI software



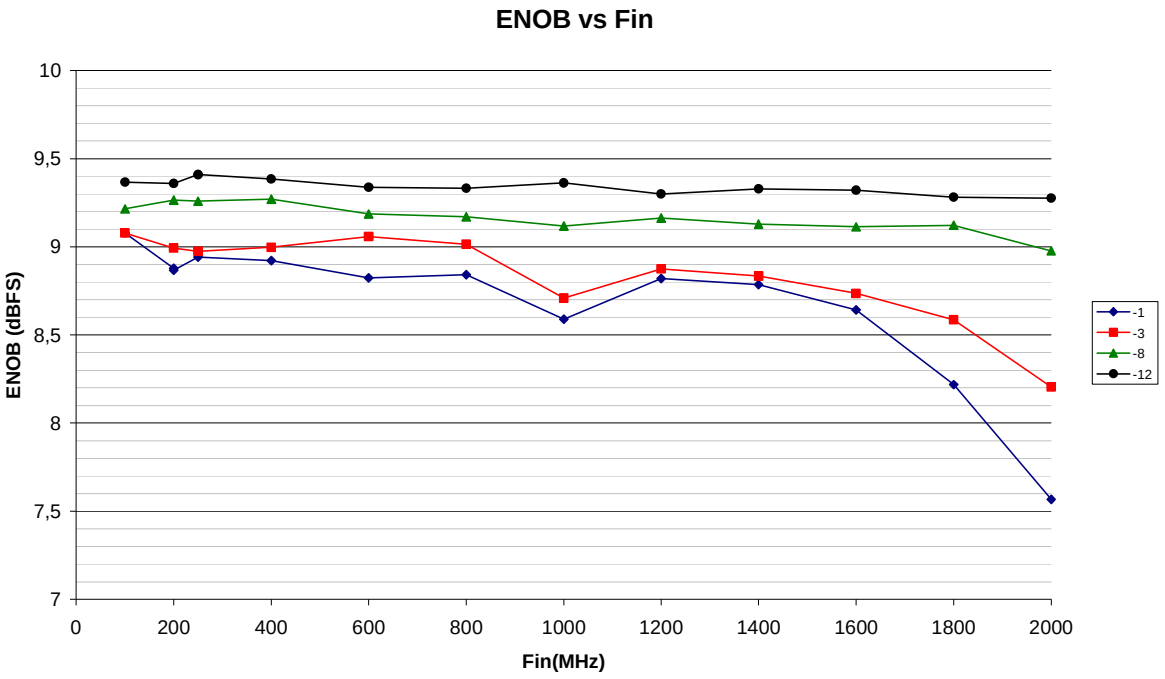


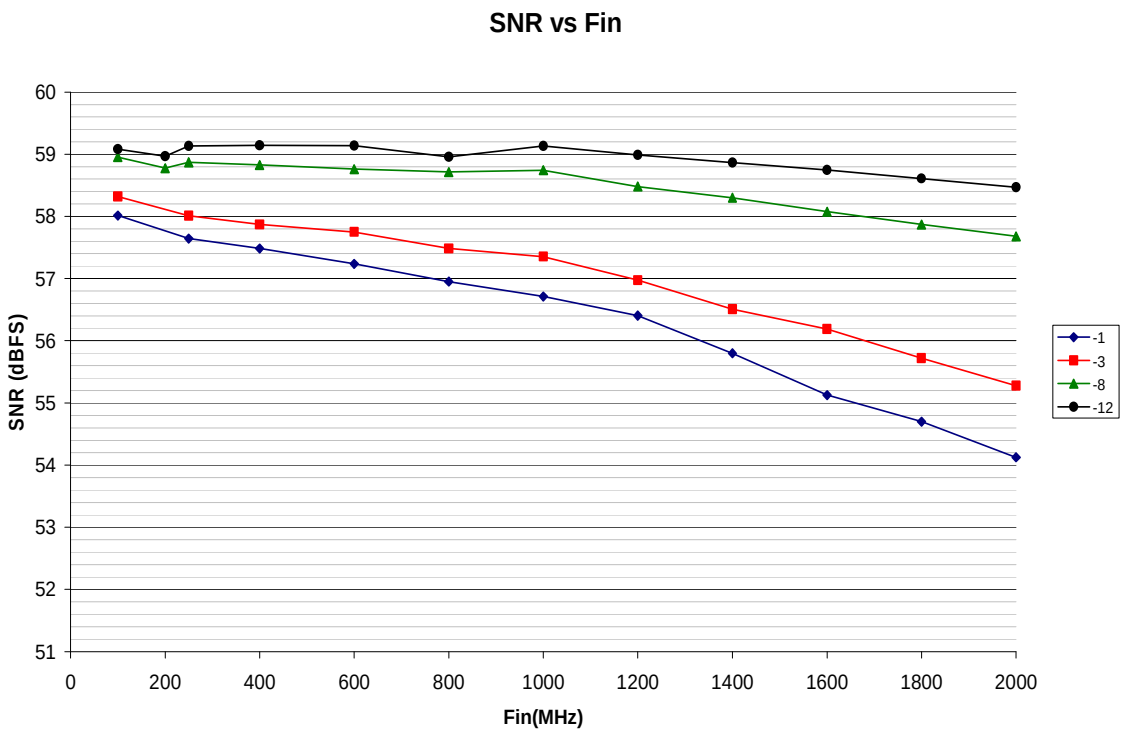
The software allows via a graphical user interface to set the different modes of the 12b ADC as de the DMUX mode, or other setting as the picture below.

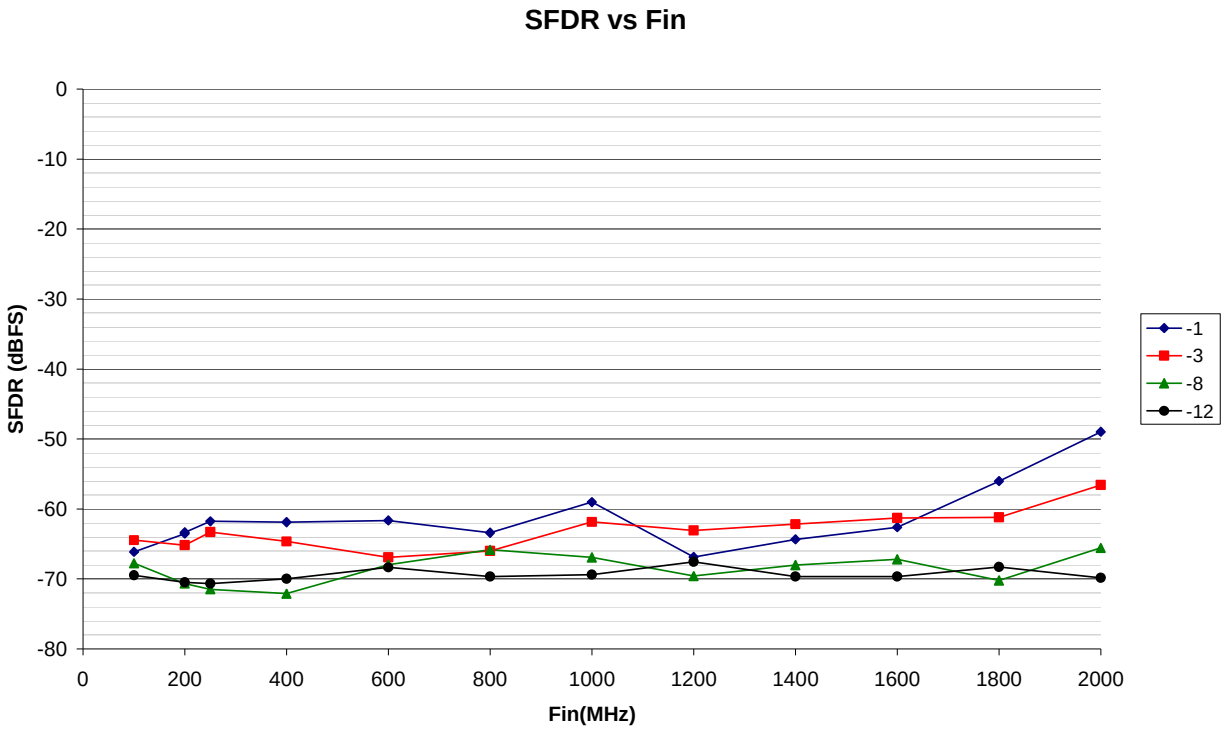
Task 6.2: Electrical validation

Measurements are compliant with the specifications.
The following figures show AC performances according to analogue input frequency at Fclock=1.5Gsps.

figure 17. Picture of the 12b ADC single tone performances versus input frequency at different input levels (-1, -3, -8, -12dBFS) Fs = 1.5GSps DMUX 1:2






SFDR vs Fin
SFDR (dBFS)
0
-10
-20
-30
-40
-50
-60
-70
-80
0
200
400
600
800
1000
1200
1400
1600
1800
2000
Fin(MHz)
-1
-3
-8
-12

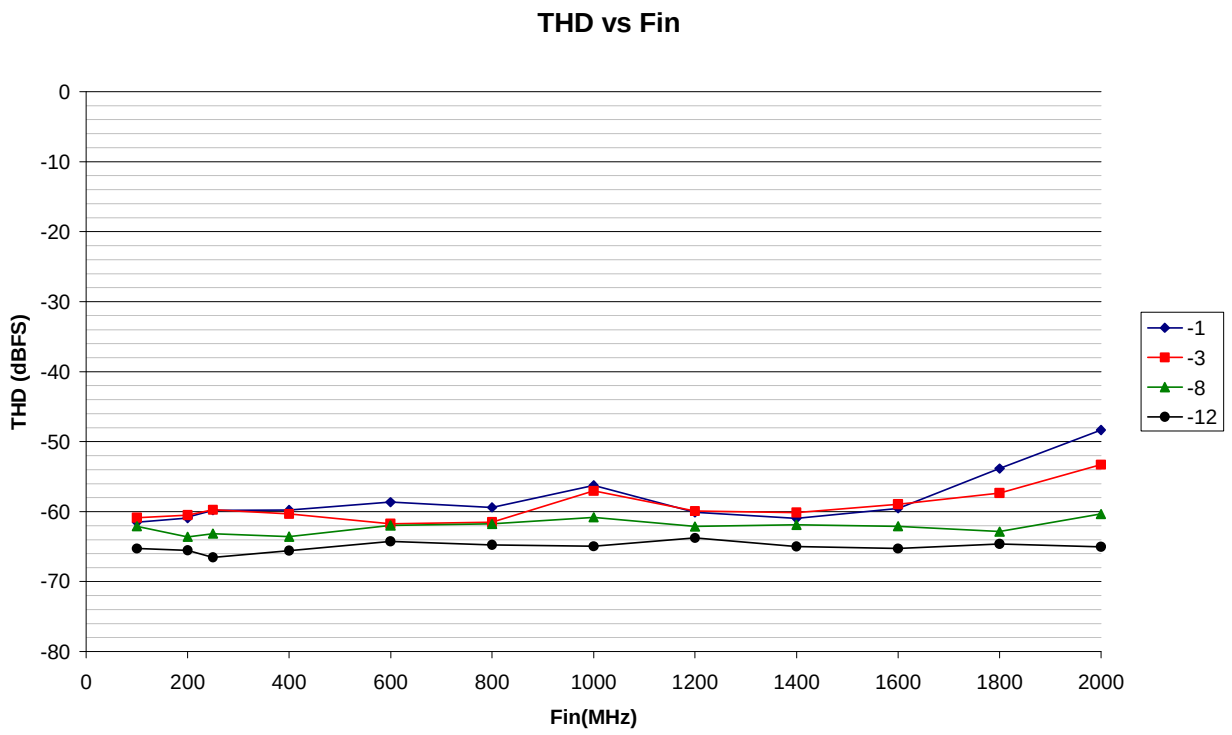
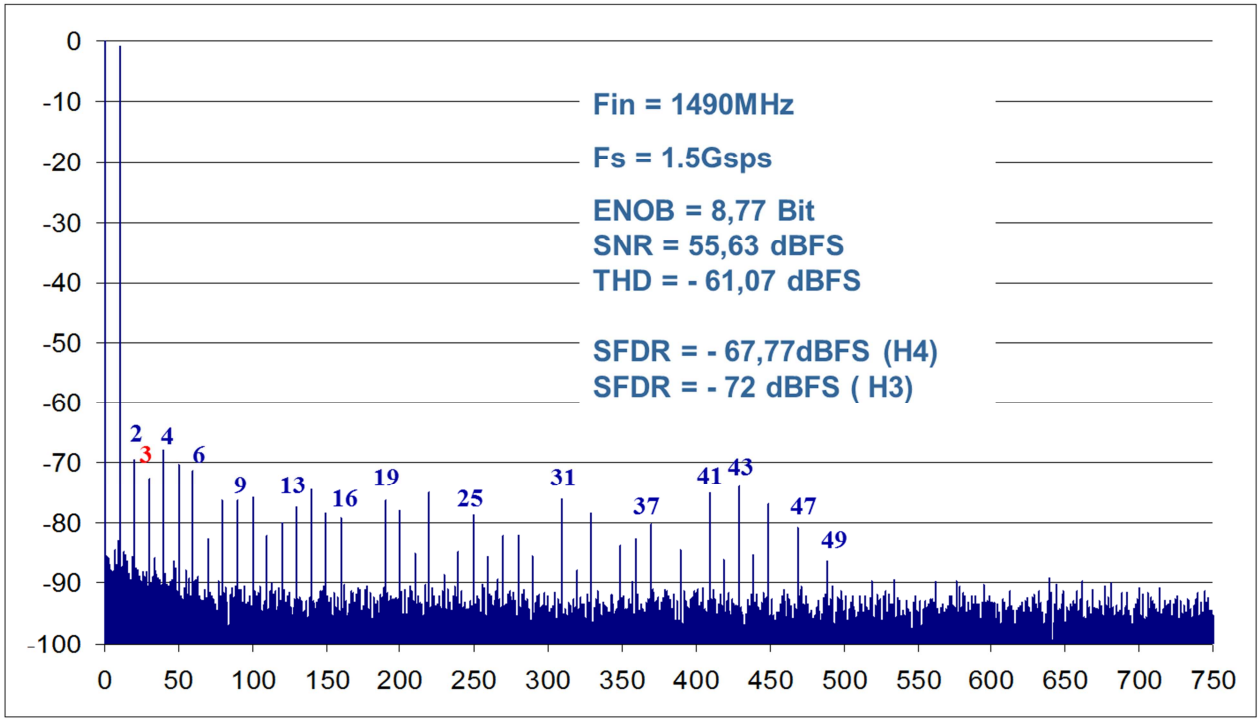
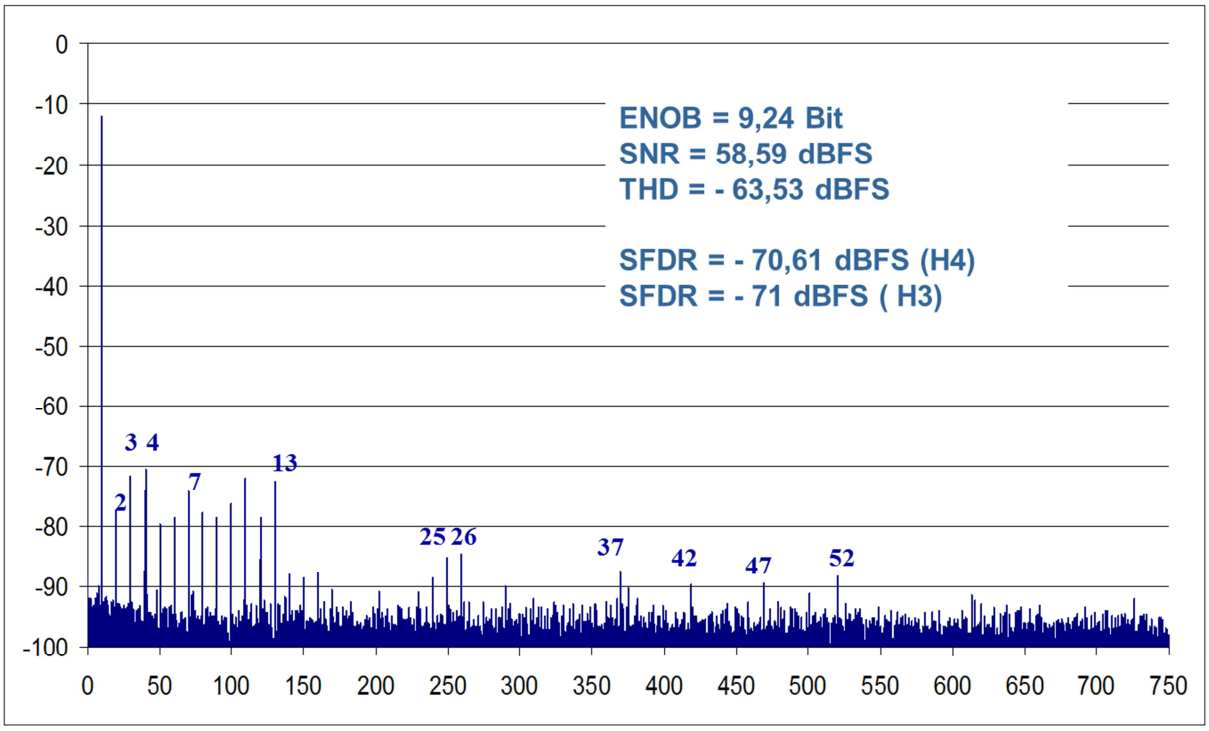

THD vs Fin
THD (dBFS)
0
-10
-20
-30
-40
-50
-60
-70
-80
0
200
400
600
800
1000
1200
1400
1600
1800
2000
Fin(MHz)
-1
-3
-8
-12

figure 18. Spectral purity of the 12b ADC respectively for -1 dBFS and -12dBFS



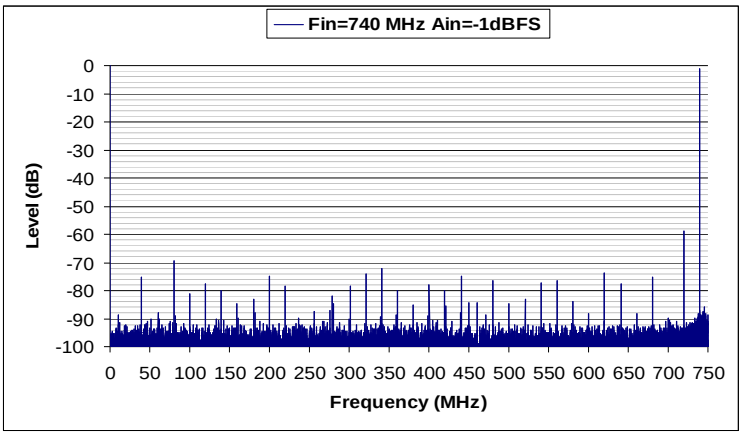


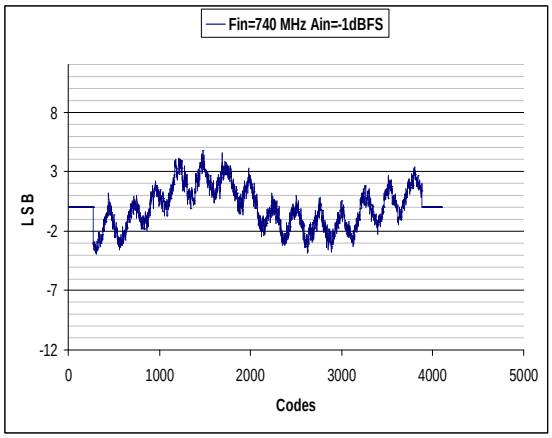
Conclusions

The main improvement of this revision has been successfully validated.

- Correction of INL shape:

”S” curve bend on the INL characteristics (seen on the firt testchip) has been corrected thanks to accurate modelling of NPN transistor (avalanche effect).

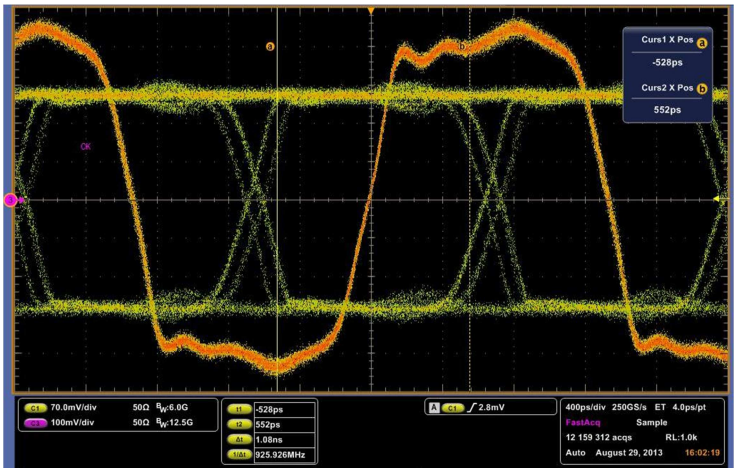




- Eye diagram:

Eye opening is significantly improved in DMUX1:1 and DMUX2:1 and is not impacted by temperature.

figure 19. Eye DMUX2:1 at Fc = 1.5Ghz



- Dual power supplies:

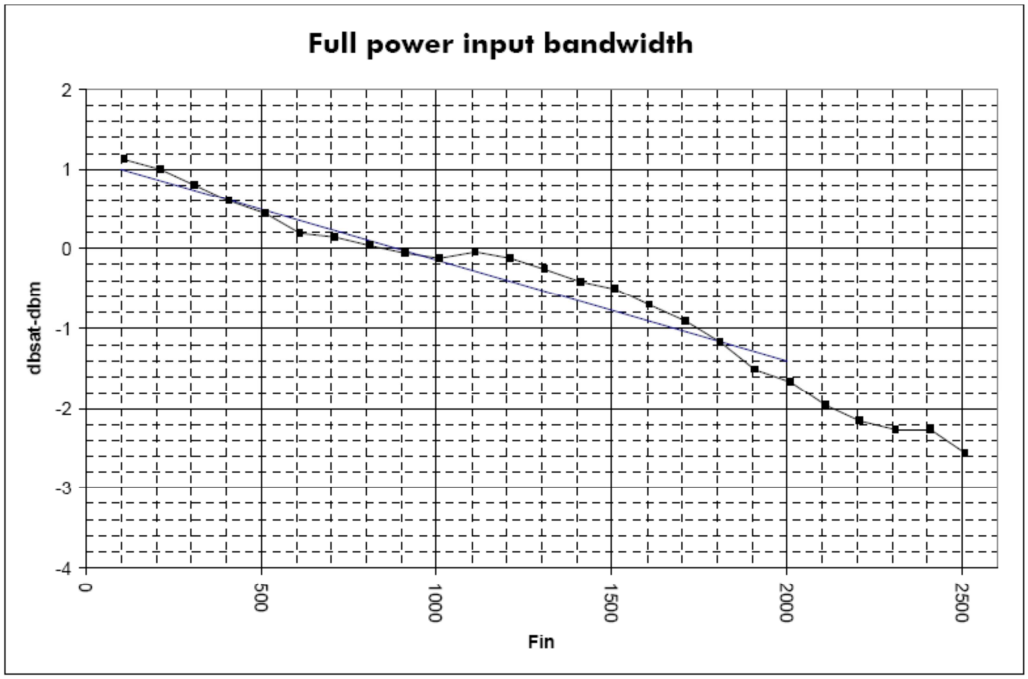
It is now possible to use VccO at 3.3V. Therefore only two different power rails can be used.
TMV architecture implemented in order to improve the radiation robustness (SEE single even effect issue) does not affect clock max =1.7GHz

<u>Task 6.4: Electrical Validation by end users TAS and ASTRIUM</u>

For TAS (reference report : 100615958U)
In all the different tested configurations (Fin <2.5GHz and Fsamp <1.7GHz) :

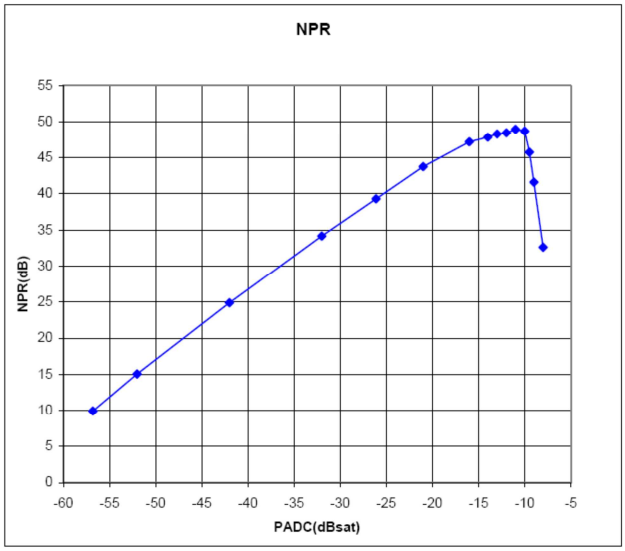
- The gain slope is around 0.15dB/100MHz

figure 20. 12b ADC input bandwidth



- ENOB is better than 9 bit for Pin up to –2dBFs, and it is better than 9.3dB for power level up to –12 dBFs.
- Worst spurious (or harmonic) are lower than 66dB under full scale CW
- NPR is better than 45dB at optimum, with a full band signal

figure 21. NPR results



As a conclusion, the results of the tests run by TAS are very similar to figures given by E2V. It can also be noted that the EV12AS200 ADC offers a significant increase of performance compared to 10 bit EV10AS180 ADC, especially in term of NPR (around 3 dB), ENOB (around 0.6 bit) in particular, and SFDR (roughly 2 to 5dB),

1.4 Potential impact

1.4.1 For e2v

The project started in 2010 and one of the achievements is the successful design of the 10b ADC @ 1.5Gsps an d 12b ADC @1.5GSps ADC's (Analog to Digital Converter) featuring state of the art performances especially at very high input frequency.
Those ADC have been successfully developed by e2v in partnership with Astrium and Thalès Alenia Space (TAS).

Considering its unmatched performances, these ADC also gave rise to interest over the whole industry worldwide in the space market but also adjacent industrial market.

All figures show that the ADC's developed in FP7 COMETS project is a great technical achievement for Europe, as its direct competitors are in the US. More over, the European space industry keeps control on the design and yet to come, production chain for such high-level devices which ensure the supplying independence of Europe

The main advantages brought by the broadband L Band, 12b 1.5GSpsADC to the Satellite market for the digital payload are:

- Allow for optimizing use of scarce spectrum
- Bring flexibility to operators (re-configurability)
- System simplification (possibility to remove down conversion thanks to L Band)
- European sourcing (No ITAR procurement issues) (design / wafer manufacturing / assembly / test)

The mains space applications are:

- Digital payload in Telecom satellite
- SAR radar (e.g. Earth observation)
- Positioning

Other applications in adjacent markets are

- Acquisition board COTS
- Defense applications

<u>Space Market</u>
Thanks to new satellites and replacement orders, satellite manufacturers are creating a balance between available capacity and new demand. This is expected to provide a sustainable market for satellite manufacturers, and subsequently to Space level component manufacturers such as e2v.
The satellite manufacturing market is dominated by six major manufacturers Thales Alenia Space (TAS) and Astrium in Europe, Boeing, Lockheed Martin, Orbital Sciences, and Space Systems/Loral in the United States. These manufacturers serve #35 different satellite services operators within a cyclical market.
Intelsat, SES Global and Eutelsat represent a very significant part of the satellite operators and as such their impact on the market is very important.
Evaluation of Space market for the 12b ADC developed in COMETS

<u>Competition</u>
Regarding Fast Broadband ADC's e2v is facing key players all located in the US. Main competitor is TI (US).

E2v as such is the only ADC vendor in Europe to be able to produce ADC (and DACs) with high-end performance beyond competition, especially at very high input frequency, allowing significant system simplification.

Product durability

For over 25 years e2v Grenoble has been providing high performance products to the Space market worldwide. e2v's broad capabilities in terms of hermetic packaging and test are unique in Europe. This capacity is supported by a reliable product obsolescence mitigation strategy dedicated to long term support of customers' needs.

The duration of availability of the 10b & 12b/1.5GSps ADC's and developed in the frame of the COMETS project, is beyond 5 years after the device is placed on EPPL.

CONCLUSIONS

E2v foresees a low volume but very high added value market in Space activity which fully the justifies the development of the 12b ADC which has taken place in COMETS FP7 project.

This will have to be followed by the Space qualification and ESCC evaluation of the 12b ADC in the frame of the ITT ESA funding.

1.4.2 For ASTRIUM

Digital payload processing capability is a key technological enabler for operators of telecommunication satellites. The ability to digitally route traffic, dynamically adjust power and coverage in response to changing link budgets is a key requirement actively sought by commercial operators of telecommunication satellites.

ADC convertor technology is the essential front-end of all digital payload processors. The new 10 and 12-bit ADCs from e2v provide Astrium with options when selecting mixed-signal convertors for future digital payload processors.

The e2v ADCs have been architected to allow direct digitization of L-band carriers making future DSPs lighter, smaller, less power consuming and lower cost. Astrium Ltd. evaluated the 10 and 12-bit ADCs developed by the COMETS project.

For the 10-bit part, Astrium measured a full-scale, baseband, single-tone performance between 8 and 8.2 bits when sampling at 1 GSPS.

The baseband NPR measured from the 10-bit ADC ranged from 39.5 to 42.5 dB when sampling at 1 GSPS. This is equivalent to a dynamic broadband performance between 8 and 8.5 bits. The L-band NPR measured from the 10-bit ADC ranged from 26 to 40 dB as a function of sampling frequency.

For the 12-bit ADC, Astrium measured a full-scale, baseband, single-tone performance around 9 bits when sampling at 1 GSPS. The UHF and L-band NPR measured from the 12-bit ADC was 48 dB when sampling at 1 GSPS. This is equivalent to a dynamic broadband performance of 9.3 bits.

A number of key observations were made during the development of the 10 and 12-bit ADCs regarding specification, performance, packaging, using the evaluation hardware and Simulation support. All of these suggestions have been shared constructively with e2v to ensure their ADCs are fit-for-purpose, benefit the space industry, as well as delivering added value to our customers.

Astrium Ltd. is working with its customers to identify missions that can baseline the new e2v range of space-grade mixed-signal convertors. We are now seeing success for a number of different applications including telecommunications, navigation and Earth observation.

1.4.3 For Infineon,

The first obvious impact is creating additional market opportunities for its leading-edge SiGe high speed technologies. Such technologies allow the design of very competitive high performance RF applications. On the other hand typical volumes for such applications are rather low. Additional opportunities, like the telecommunication applications in space investigated in this project help to broaden the application, which is key for assuring the availability of such high-speed semiconductor technologies at reasonable fabrication costs in Europe. This also helps to safeguard the related direct and indirect employment.

But the impact of the COMETS project goes far beyond this. It provided an ideal environment for bringing together not only semiconductor technology provider and application designer at a very early stage of product development, but especially also enabled a close cooperation with academia, in this case with the very advanced CNES characterization and modeling laboratories. By demonstrating the advanced capabilities of these research institutions on the specific COMETS example this establishes contacts and networks that extend the impact beyond the COMETS project itself for future research and development projects.

A part of the gained knowledge on new devices and advanced characterization was also published in peer reviewed international journals and conferences, contributing to advancing the scientific state-of-the-art, see the list in section 2. As a further effect the close cooperation between industry and academia also ensured that graduate students in their PhD research work gained experience with real life examples from modern technologies and applications, in this case especially with an advanced European SiGe HBT technology. This is a clear impact on Europe's graduate education, beneficial for both, industry and the academic institutions.

1.4.4 For TAS

TAS customers demand is moving to more and more capacity but with reduced power and mass impact.

For TAS, COMETS project represents a wide step in the way to be able to respond to such an ambitious demand. In fact it has played to major roles.

The first one is of course that it has given access of a very wide band A to D converter for space application. Indeed, with the complete evaluation for space environment of the EV10AS180 ADC, a very wide band quite low power component is available for short term demands, and the EV12AS200 lets have access to even significantly higher performance, with similar technology, thus space compatible.

But, furthermore than that, its activity during the project has allowed TAS to be able to manage such sharp and sensitive components in term of implementation and solution of electrical issues for space applications, which is mandatory to be able to achieve the customers expected performance.

1.4.5 CNES

In the frame of COMETS project, the ESCC evaluation of 10bits EV10AS180 ADC was performed and all results were satisfactory. With this high quality level reached, E2V 10bits ADC can be used in space equipments. The development of 12bits EV12AS200 ADC was achieved in frame of COMETS. Here the results are lower because this product will be not offered by E2V for space applications

1.4.6 CNRS

The benefit of IEMN from its participation is mainly in increase in academic knowledge. This project gave us the opportunity to:

- further improve our S parameter measurement and noise Figure extraction methodology on new bipolar transistors.
- better understand the physical key parameters required to realize high frequency, high resolution ADC
- Finalize the development thermal test bench base on the IR-camera
- publish a paper at Proceedings of 6th European Microwave Integrated Circuits Conference, EuMIC 2011, Manchester, UK, october 10-11, 2011, 386-389, ISBN 978-1-61284-236-3

The benefit for XLIM is in improvement of technical skills concerning

- Electro thermal modelling of SiGe transistors based on low frequency S parameter measurements
- Narrow pulsed I/V (50 ns) characterisation knowledge for ultra fast semiconductor devices.
- Non linear model in both SDD format and Verilog format for implementation in ADS Agilent and Cadence CAD tools

Two papers have been published

- Compact RF Non linear electro thermal model of SiGe HBT for the design of broadband ADCs:
  A Saleh,A EL Rafei, T Reveyrand ,R Sommet, JM Nebus, R Quéré
  International Journal of microwave and wireless technologies, Vol 4, issue 06, pp. 569-578. , December 2012
- Experimental characterization and modelling of the thermal behavior of SiGe HBTs
  A El Rafei, A Saleh, R Sommet , JM Nebus , R Quéré
  IEEE Transactions on electron devices vol 59 ,N° 7 ,pp 1921-1927 , July 2012

1.5 Project public website

www.comets-fp7.eu

2 Use and dissemination of foreground

Section A (public)

This section includes two templates

- Template A1: List of all scientific (peer reviewed) publications relating to the foreground of the project.
- Template A2: List of all dissemination activities (publications, conferences, workshops, web sites/applications, press releases, flyers, articles published in the popular press, videos, media briefings, presentations, exhibitions, thesis, interviews, films, TV clips, posters).

These tables are cumulative, which means that they should always show all publications and activities from the beginning until after the end of the project. Updates are possible at any time.

TEMPLATE A1: LIST OF SCIENTIFIC (PEER REVIEWED) PUBLICATIONS, STARTING WITH THE MOST IMPORTANT ONES										
NO.	Title	Main author	Title of the periodical or the series	Number, date or frequency	Publisher	Place of publication	Year of publication	Relevant pages	Permanent identifiers[2] (if available)	Is/Will open access[3] provided to this publication?
1	*Bias Point Optimization for Low Power / Low Noise Applications of Advanced SiGe HBT*	N.Waldhoff	Proc. of EuMIC		EuMA (European Microwave Association)		October 2011	pp. 386-389		No
2	*Integrated Injection Logic in a High-Speed SiGe Bipolar Technology*	K. Aufinger	Proc. of BCTM		IEEE		October 2011	pp. 87-90		No
3	Experimental Characterization and Modeling of the Thermal Behaviour of SiGe HBTs	A. El Rafei	Trans. Electron Devices	vol. 59, no.7	IEEE		July 2012	pp. 1921- 1927		No
4	Compact RF non-linear electro thermal model of SiGe HBT for the design of broadband ADCs	A. Saleh	Int. J. of Microwave and Wireless Tech.	Vol. 4 is. 6	Cambridge Univ. Press		December 2012	pp. 569-578		No

[2] A permanent identifier should be a persistent link to the published version full text if open access or abstract if article is pay per view) or to the final manuscript accepted for publication (link to article in repository).
[3] Open Access is defined as free of charge access for anyone via Internet. Please answer "yes" if the open access to the publication is already established and also if the embargo period for open access is not yet over but you intend to establish open access afterwards.

TEMPLATE A2: LIST OF DISSEMINATION ACTIVITIES								
NO.	Type of activities[4]	Main leader	Title	Date/Period	Place	Type of audience[5]	Size of audience	Countries addressed
1	conference	E2v	Let 's embrace Space	12-13 May 2011	Budapest (Hungary)	Space community		Europe
2	conference	E2v/CNES	RADECS2012	Sept 2012	Biarritz (FR)	Space community		

[4] A drop down list allows choosing the dissemination activity: publications, conferences, workshops, web, press releases, flyers, articles published in the popular press, videos, media briefings, presentations, exhibitions, thesis, interviews, films, TV clips, posters, Other.

[5] A drop down list allows choosing the type of public: Scientific Community (higher education, Research), Industry, Civil Society, Policy makers, Medias, Other ('multiple choices' is possible).

Section B (Confidential[6] or public: confidential information to be marked clearly)
Part B1

The applications for patents, trademarks, registered designs, etc. shall be listed according to the template B1 provided hereafter.

The list should, specify at least one unique identifier e.g. European Patent application reference. For patent applications, only if applicable, contributions to standards should be specified. This table is cumulative, which means that it should always show all applications from the beginning until after the end of the project.

TEMPLATE B1: LIST OF APPLICATIONS FOR PATENTS, TRADEMARKS, REGISTERED DESIGNS, ETC.					
Type of IP Rights[7]:	Confidential Click on YES/NO	Foreseen embargo date dd/mm/yyyy	Application reference(s) (e.g. EP123456)	Subject or title of application	Applicant (s) (as on the application)

[6] Note to be confused with the "EU CONFIDENTIAL" classification for some security research projects.

[7] A drop down list allows choosing the type of IP rights: Patents, Trademarks, Registered designs, Utility models, Others.

Part B2

Type of Exploitable Foreground[8]	Description of exploitable foreground	Confidential Click on YES/NO	Foreseen embargo date dd/mm/yyyy	Exploitable product(s) or measure(s)	Sector(s) of application[9]	Timetable, commercial or any other use	Patents or other IPR exploitation (licences)	Owner & Other Beneficiary(s) involved
	Ex: New supercond uctive Nb-Ti alloy			*MRI equipment*	*1. Medical* *2. Industrial inspection*	*2008* *2010*	*A materials patent is planned for 2006*	*Beneficiary X (owner) Beneficiary Y, Beneficiary Z, Poss. licensing to equipment manuf. ABC*

In addition to the table, please provide a text to explain the exploitable foreground, in particular:

- *Its purpose*
- *How the foreground might be exploited, when and by whom*
- *IPR exploitable measures taken or intended*
- *Further research necessary, if any*
- *Potential/expected impact (quantify where possible)*

[19] A drop down list allows choosing the type of foreground: General advancement of knowledge, Commercial exploitation of R&D results, Exploitation of R&D results via standards, exploitation of results through EU policies, exploitation of results through (social) innovation.

[9] A drop down list allows choosing the type sector (NACE nomenclature) : http://ec.europa.eu/competition/mergers/cases/index/nace_all.html

3 Report on societal implications

Replies to the following questions will assist the Commission to obtain statistics and indicators on societal and socio-economic issues addressed by projects. The questions are arranged in a number of key themes. As well as producing certain statistics, the replies will also help identify those projects that have shown a real engagement with wider societal issues, and thereby identify interesting approaches to these issues and best practices. The replies for individual projects will not be made public.

A General Information *(completed automatically when **Grant Agreement number** is entered.*

Grant Agreement Number:	242 521
Title of Project:	COMETS
Name and Title of Coordinator:	Jean-luc Diverchy - R&D Program Manager

B Ethics

1. Did your project undergo an Ethics Review (and/or Screening)? • If Yes: have you described the progress of compliance with the relevant Ethics Review/Screening Requirements in the frame of the periodic/final project reports? Special Reminder: the progress of compliance with the Ethics Review/Screening Requirements should be described in the Period/Final Project Reports under the Section 3.2.2 *'Work Progress and Achievements'*	***0Yes XNo***
2. Please indicate whether your project involved any of the following issues (tick box) :	***YES***
RESEARCH ON HUMANS	
• Did the project involve children?	*No*
• Did the project involve patients?	*No*
• Did the project involve persons not able to give consent?	*No*
• Did the project involve adult healthy volunteers?	*No*
• Did the project involve Human genetic material?	*No*
• Did the project involve Human biological samples?	*No*
• Did the project involve Human data collection?	*No*
RESEARCH ON HUMAN EMBRYO/FOETUS	
• Did the project involve Human Embryos?	*No*
• Did the project involve Human Foetal Tissue / Cells?	*No*
• Did the project involve Human Embryonic Stem Cells (hESCs)?	*No*
• Did the project on human Embryonic Stem Cells involve cells in culture?	*No*
• Did the project on human Embryonic Stem Cells involve the derivation of cells from Embryos?	*No*
PRIVACY	
• Did the project involve processing of genetic information or personal data (eg. health, sexual lifestyle, ethnicity, political opinion, religious or philosophical conviction)?	*No*
• Did the project involve tracking the location or observation of people?	*No*
RESEARCH ON ANIMALS	
• Did the project involve research on animals?	*No*
• Were those animals transgenic small laboratory animals?	*No*

• Were those animals transgenic farm animals?	*No*
• Were those animals cloned farm animals?	*No*
• Were those animals non-human primates?	*No*
RESEARCH INVOLVING DEVELOPING COUNTRIES	
• Did the project involve the use of local resources (genetic, animal, plant etc)?	*No*
• Was the project of benefit to local community (capacity building, access to healthcare, education etc)?	*No*
DUAL USE	
• Research having direct military use	0 Yes X No
• Research having the potential for terrorist abuse	*No*

C Workforce Statistics

3. Workforce statistics for the project: Please indicate in the table below the number of people who worked on the project (on a headcount basis).

Type of Position	Number of Women	Number of Men
Scientific Coordinator		2
Work package leaders	2	5
Experienced researchers (i.e. PhD holders)	1	3
PhD Students		3
Other	3	18

4. How many additional researchers (in companies and universities) were recruited specifically for this project?	**0**
Of which, indicate the number of men:	

D Gender Aspects

5. Did you carry out specific Gender Equality Actions under the project?

○ Yes
✕ No

6. Which of the following actions did you carry out and how effective were they?

	Not at all effective				Very effective
❑ Design and implement an equal opportunity policy	○	○	○	○	○
❑ Set targets to achieve a gender balance in the workforce	○	○	○	○	○
❑ Organise conferences and workshops on gender	○	○	○	○	○
❑ Actions to improve work-life balance	○	○	○	○	○

○ Other:

7. Was there a gender dimension associated with the research content – i.e. wherever people were the focus of the research as, for example, consumers, users, patients or in trials, was the issue of gender considered and addressed?

○ Yes- please specify

✕ No

E Synergies with Science Education

8. Did your project involve working with students and/or school pupils (e.g. open days, participation in science festivals and events, prizes/competitions or joint projects)?

✕ Yes- please specify: PhD in WP4

○ No

9. Did the project generate any science education material (e.g. kits, websites, explanatory booklets, DVDs)?

○ Yes- please specify

✕ No

F Interdisciplinarity

10. Which disciplines (see list below) are involved in your project?

✕ Main discipline[10]: 2.2

○ Associated discipline[10]:

○ Associated discipline[10]: 2.3

G Engaging with Civil society and policy makers

11a Did your project engage with societal actors beyond the research community? *(if 'No', go to Question 14)*

○ Yes
✕ No

11b If yes, did you engage with citizens (citizens' panels / juries) or organised civil society (NGOs, patients' groups etc.)?

○ No

○ Yes- in determining what research should be performed

○ Yes - in implementing the research

○ Yes, in communicating /disseminating / using the results of the project

[10] Insert number from list below (Frascati Manual).

11c In doing so, did your project involve actors whose role is mainly to organise the dialogue with citizens and organised civil society (e.g. professional mediator; communication company, science museums)?	○ ✕	Yes No

12. Did you engage with government / public bodies or policy makers (including international organisations)

- ✕ No
- ○ Yes- in framing the research agenda
- ○ Yes - in implementing the research agenda
- ○ Yes, in communicating /disseminating / using the results of the project

13a Will the project generate outputs (expertise or scientific advice) which could be used by policy makers?

- ○ Yes – as a **primary** objective (please indicate areas below- multiple answers possible)
- ○ Yes – as a **secondary** objective (please indicate areas below - multiple answer possible)
- ✕ No

13b If Yes, in which fields?

Agriculture		Energy		Human rights	
Audiovisual and Media		Enlargement		Information Society	
Budget		Enterprise		Institutional affairs	
Competition		Environment		Internal Market	
Consumers		External Relations		Justice, freedom and security	
Culture		External Trade		Public Health	
Customs		Fisheries and Maritime Affairs		Regional Policy	
Development Economic and Monetary Affairs		Food Safety		Research and Innovation	
		Foreign and Security Policy		Space	
Education, Training, Youth		Fraud		Taxation	
Employment and Social Affairs		Humanitarian aid		Transport	

13c If Yes, at which level? ○ Local / regional levels ○ National level ○ European level ○ International level	

H Use and dissemination

14. How many Articles were published/accepted for publication in peer-reviewed journals?	**4**
To how many of these is open access[11] provided?	
How many of these are published in open access journals?	**0**
How many of these are published in open repositories?	
To how many of these is open access not provided?	**4**
Please check all applicable reasons for not providing open access:	
✕ publisher's licensing agreement would not permit publishing in a repository ❑ no suitable repository available ❑ no suitable open access journal available ❑ no funds available to publish in an open access journal ❑ lack of time and resources ❑ lack of information on open access ❑ other[12]: ……	

15. How many new patent applications ('priority filings') have been made? *("Technologically unique": multiple applications for the same invention in different jurisdictions should be counted as just one application of grant).*		**0**
16. Indicate how many of the following Intellectual Property Rights were applied for (give number in each box).	Trademark	**0**
	Registered design	**0**
	Other	**NA**
17. How many spin-off companies were created / are planned as a direct result of the project?		**0**
Indicate the approximate number of additional jobs in these companies:		

18. Please indicate whether your project has a potential impact on employment, in comparison with the situation before your project:			
✕	Increase in employment, or	❑	In small & medium-sized enterprises
❑	Safeguard employment, or	✕	In large companies
❑	Decrease in employment,	❑	None of the above / not relevant to the project
❑	Difficult to estimate / not possible to quantify		

19. For your project partnership please estimate the employment effect resulting directly from your participation in Full Time Equivalent (*FTE = one person working fulltime for a year*) jobs:	*Indicate figure:*

[11] Open Access is defined as free of charge access for anyone via Internet.
[12] For instance: classification for security project.

Difficult to estimate / not possible to quantify	✕

I Media and Communication to the general public

20. As part of the project, were any of the beneficiaries professionals in communication or media relations?

✕ Yes ○ No

21. As part of the project, have any beneficiaries received professional media / communication training / advice to improve communication with the general public?

○ Yes ✕ No

22 Which of the following have been used to communicate information about your project to the general public, or have resulted from your project?

❑	Press Release	✕	Coverage in specialist press
❑	Media briefing	❑	Coverage in general (non-specialist) press
❑	TV coverage / report	❑	Coverage in national press
❑	Radio coverage / report	❑	Coverage in international press
❑	Brochures /posters / flyers	✕	Website for the general public / internet
❑	DVD /Film /Multimedia	❑	Event targeting general public (festival, conference, exhibition, science café)

23 In which languages are the information products for the general public produced?

❑	Language of the coordinator	✕	English
❑	Other language(s)		

***Question F-10*:** Classification of Scientific Disciplines according to the Frascati Manual 2002 (Proposed Standard Practice for Surveys on Research and Experimental Development, OECD 2002):

FIELDS OF SCIENCE AND TECHNOLOGY

1. NATURAL SCIENCES

1.1 Mathematics and computer sciences [mathematics and other allied fields: computer sciences and other allied subjects (software development only; hardware development should be classified in the engineering fields)]

1.2 Physical sciences (astronomy and space sciences, physics and other allied subjects)

1.3 Chemical sciences (chemistry, other allied subjects)

1.4 Earth and related environmental sciences (geology, geophysics, mineralogy, physical geography and other geosciences, meteorology and other atmospheric sciences including climatic research, oceanography, vulcanology, palaeoecology, other allied sciences)

1.5 Biological sciences (biology, botany, bacteriology, microbiology, zoology, entomology, genetics, biochemistry, biophysics, other allied sciences, excluding clinical and veterinary sciences)

2 ENGINEERING AND TECHNOLOGY

2.1 Civil engineering (architecture engineering, building science and engineering, construction engineering, municipal and structural engineering and other allied subjects)

2.2 Electrical engineering, electronics [electrical engineering, electronics, communication engineering and systems, computer engineering (hardware only) and other allied subjects]

2.3. Other engineering sciences (such as chemical, aeronautical and space, mechanical, metallurgical and materials engineering, and their specialised subdivisions; forest products; applied sciences such as geodesy, industrial chemistry, etc.; the science and technology of food production; specialised technologies of

interdisciplinary fields, e.g. systems analysis, metallurgy, mining, textile technology and other applied subjects)

3. MEDICAL SCIENCES

3.1 Basic medicine (anatomy, cytology, physiology, genetics, pharmacy, pharmacology, toxicology, immunology and immunohaematology, clinical chemistry, clinical microbiology, pathology)

3.2 Clinical medicine (anaesthesiology, paediatrics, obstetrics and gynaecology, internal medicine, surgery, dentistry, neurology, psychiatry, radiology, therapeutics, otorhinolaryngology, ophthalmology)

3.3 Health sciences (public health services, social medicine, hygiene, nursing, epidemiology)

4. AGRICULTURAL SCIENCES

4.1 Agriculture, forestry, fisheries and allied sciences (agronomy, animal husbandry, fisheries, forestry, horticulture, other allied subjects)

4.2 Veterinary medicine

5. SOCIAL SCIENCES

5.1 Psychology

5.2 Economics

5.3 Educational sciences (education and training and other allied subjects)

5.4 Other social sciences [anthropology (social and cultural) and ethnology, demography, geography (human, economic and social), town and country planning, management, law, linguistics, political sciences, sociology, organisation and methods, miscellaneous social sciences and interdisciplinary , methodological and historical S1T activities relating to subjects in this group. Physical anthropology, physical geography and psychophysiology should normally be classified with the natural sciences].

6. HUMANITIES

6.1 History (history, prehistory and history, together with auxiliary historical disciplines such as archaeology, numismatics, palaeography, genealogy, etc.)

6.2 Languages and literature (ancient and modern)

6.3 Other humanities [philosophy (including the history of science and technology) arts, history of art, art criticism, painting, sculpture, musicology, dramatic art excluding artistic "research" of any kind, religion, theology, other fields and subjects pertaining to the humanities, methodological, historical and other S1T activities relating to the subjects in this group]