Contents

4.1 Final publishable summary report

4.1.1 Executive summary

The objectives of the project "Hybrid organic/inorganic memory elements for integration of electronic and photonic circuitry" (HYMEC) were to resolve fundamental issues of materials science and to realize new hybrid inorganic/organic devices with functionality far beyond current state-of-the-art. This is of direct relevance to the objectives of the FP7-NMP Work Programme, as it calls for "design novel knowledge-based smart materials with tailored properties, releasing their potential for enhanced and innovative applications".
We performed coordinated research towards understanding and controlling all relevant properties of systems comprising inorganic metal nanoparticles (NPs) embedded in matrices of conjugated organic materials (organic semiconductors), and we demonstrated the function of such material hybrids in non-volatile memory elements (NV-MEs) that can be addressed electrically and optically, which thus represent potential interconnects of future hybrid electronic and photonic circuitry. Electronic, optical, dielectric, structural, and morphological properties of our systems were determined using state-of-the-art experimental techniques and theoretical modelling to establish a reliable and specific knowledge base, which we exploited for device fabrication and integration. During the first project stage, we identified that resistance switching is such devices is based on filament formation, rather than charge storage on the metal NP (as assumed so far in literature). With a properly adjusted work program, involving a new device layout, we have established reliable design rules for such devices in technologically relevant applications.
Moreover, we succeeded in implementing cost-efficient production routes, such as printing, as well as exploring the ultimate miniaturization of such memory elements by novel sublimation- and imprinting-based nanostructuring processes.
Through our cooperative efforts, we made use of the new knowledge for the realization of reliable non-volatile memory elements employing resistance switching, with a substantial extension of existing NV-ME functionality, i.e., optical addressing of devices in addition to purely electric addressing. This function was

integrated with further optical elements and multi-bit storage capability. This paves the way for large-area and low-cost advanced sensors for a multitude of stimuli (light, X-rays, mechanical stress, and chemicals).

4.1.2 4.1.2 Summary description of project context and objectives

The objectives of the project "Hybrid organic/inorganic memory elements for integration of electronic and photonic circuitry" (HYMEC) were to resolve fundamental issues of materials science and to realize new hybrid inorganic/organic devices with functionality far beyond current state-of-the-art. This was in response to the objectives of the FP7-NMP Work Programme that called for "design novel knowledge-based smart materials with tailored properties, releasing their potential for enhanced and innovative applications". Specifically, we performed research towards understanding and controlling all relevant properties of systems comprising inorganic metal nanoparticles (NPs) embedded in matrices of conjugated organic materials (organic semiconductors), with the aim to demonstrate the function of such material hybrids as non-volatile memory elements that can be addressed electrically and optically, which thus should represent potential interconnects of future hybrid electronic and photonic circuitry. Moreover, we targeted implementing cost-efficient production routes, such as printing, as well as exploring the ultimate miniaturization of such memory elements by novel sublimation- and imprinting-based nanostructuring processes.
Electronic, optical, dielectric, structural, and morphological properties of these systems were to be determined using state-of-the-art experimental techniques and modelling to establish a reliable specific knowledge base, which we can exploit for device fabrication and integration. Through our cooperative efforts, we should arrive at new knowledge for the realization of reliable non-volatile memory elements (NV-ME) employing resistance switching, with a substantial extension of existing NV-ME functionality, i.e., optical addressing (at least in one direction) of devices in addition to purely electric addressing.
This required attending to the following key issues that should enable achieving this objective:

A. Reveal the fundamental mechanisms for information storage and addressing in non-volatile memory elements based on metal NPs in conjugated organic matrices.
We set out to establish all physical prerequisites for charge storage in metal NPs embedded in organic semiconductor matrices. The mechanisms of charge storage and charge release, which are determined by the interface energy levels between the two dissimilar materials, by uni- and ambipolar currents through two-terminal devices should be identified, which was achieved. These results led to the conclusion that optical switching of charge storage on NPs is possible as proposed, but that such devices cannot be used for NV-MEs. We therefore devised an alternative device layout that allowed achieving NV-MEs with optical addressability (see below).

B. Expand the functionality of hybrid memory elements by including optical addressing.
The feasibility of optical addressing of NV-MEs should be established, by taking into account the actual switching mechanism. The original (patented beforehand by part of the consortium) idea of charge stored on metal NPs in organic matrices to be removed by optical excitation of the surrounding organic semiconductor material and subsequent charge transfer, which would be the optical equivalent to an otherwise electrical "erase" cycle, turned out to be non-functional in devices. Instead, we devised a new method to achieve optical switching by combining filamental-based switching devices with a photodiode. This enabled the realization of fully (in both directions) switchable NV-MEs, with functionality beyond that envisioned in the original proposal.

C. Develop cost-efficient fabrication routes of hybrid memory elements ranging from micro- to nanoscales.
Two major routes towards achieving cost-efficient fabrication were pursued, one of which targeted the ultimate cost-factor (printing and direct integration), while the other was driven by exploring the ultimate miniaturization and storage density limit of memory elements (nanostructure formation by glancing-angle deposition of organic materials and imprinting techniques for crossbar architectures).

D. Demonstrate fully functional electrically and optically addressable hybrid memory element arrays, including integration with other functions.
Through items A.-C. above, we derived models to correlate hybrid material properties and NV-ME function. These models had predictive character, and could thus be used to optimize memory elements with high quality specifications. Multi-bit crossbar memory were realized on two scales - low density storage capacity realized by printed device architectures, and high density storage architectures realized by imprinting methods. The memory elements were also integrated into electrical circuitry with response to external stimuli, light-emitting and (mechanical) sensor devices. Achieving these objectives represents significant advancements in fundamental material science, and through added value functionality of our devices, new technological applications were disclosed. The results of HYMEC strengthen European research and industry, including SMEs (e.g., the partner TOY of this project), sustainably.

4.1.3 Description of the main S&T results/foregrounds

HYMEC succeeded in realizing all targeted hybrid metal nanoparticle (NP) / organic matrix structures with highest reliability, as evidenced through comprehensive multi-technique analyses. The electrical characteristics of NV-MEs, in conjunction with our defined structures and theoretical modeling, allowed resolving all persisting open issues in literature regarding the resistive switching mechanisms in such devices:
(i) We revealed that charge storage on metal NPs in an organic matrix does occur, but the charging states of the NPs cannot be controlled electrically alone, so that devices are in essence always in the OFF-state without light stimulus.
(ii) When using our hybrid structures, controlled device conditioning leads to the formation of conductive filaments that can reversibly be formed and eliminated, so that full electrical writing/reading/erase cycles are possible in NV-MEs.
With the knowledge available from (i) and (ii), significant progress was enabled regarding extending the functionality of NV-MEs by including full optical addressing schemes:
(iii) Devices without filaments, i.e., where charges on metal NPs control the resistance state of the device, can be transiently switched to the ON-state during illumination with light that can be absorbed by the organic matrix, which subsequently neutralizes charges on the NPs by charge transfer. However, devices return to the OFF-state once illumination is turned off, so that fully functional NV-MEs cannot be achieved. Following these concepts, this knowledge sets an end to disputes in literature over switching in hybrid memory elements.
(iv) We devised a novel method to integrate full optical addressing schemes, including writing *and* erasing, in hybrid devices where electrical switching is based on filament formation. By adopting the device architecture with a photosensitive diode, full electrical and optical addressing of NV-MEs was demonstrated (example shown in Figure 1). This represents progress even beyond that originally anticipated in the project proposal and is presently subject of securing IP for HYMEC.

Based on existing state-of-the-art at project start we identified the main obstacles for the lack of understanding of the switching phenomena as a deficiency of well-controlled and comprehensive basic investigations of systems used for NV-ME fabrication. It was an essential objective of HYMEC to relief this deeply unsatisfactory situation. We now established clear-cut relationships between hybrid material properties and full device function, which was not available before. This was supported by multiscale modeling and simulation based on the developed models, which correlate circuital material aspects to the microscopic functionalities.

Besides generating considerable new knowledge on basic properties of NP/organic matrix systems, we exploited this to further improve NV-ME function, and to provide reliable guidelines for device architecture optimization and integration into memory arrays. Most notably, we implemented a novel strategy to expand the present functionality of NV-MEs: we combine electrical addressing of memory elements with optical means of stored information manipulation, providing access to numerous applications.

(v) We realized demonstrators of a unique light-addressable hybrid non-volatile memory array technology (see Figure 1). By vertically integrating an organic photodiode and a hybrid resistive switching element in one pixel, no additional building blocks such as transistors are needed for addressing the single nodes in an array. The 2-terminal wiring of two vertically stacked devices significantly reduces the footprint (F) of a single pixel down to the theoretical limit of $4F^2$, allowing integration with a high fill-factor. The presented features of simultaneous detection and storage of the photonic/image information directly in one pixel is closely related to the properties of inorganic CCD technology, but unlike CCD this technology does not show a destructive read-out and does not exhibit any signal-integrating behavior. With these essential features, the easy fabrication and simple wiring in combination with the advantages of organic electronics, the presented light-addressable array is a substantial step towards industry imposed specifications.

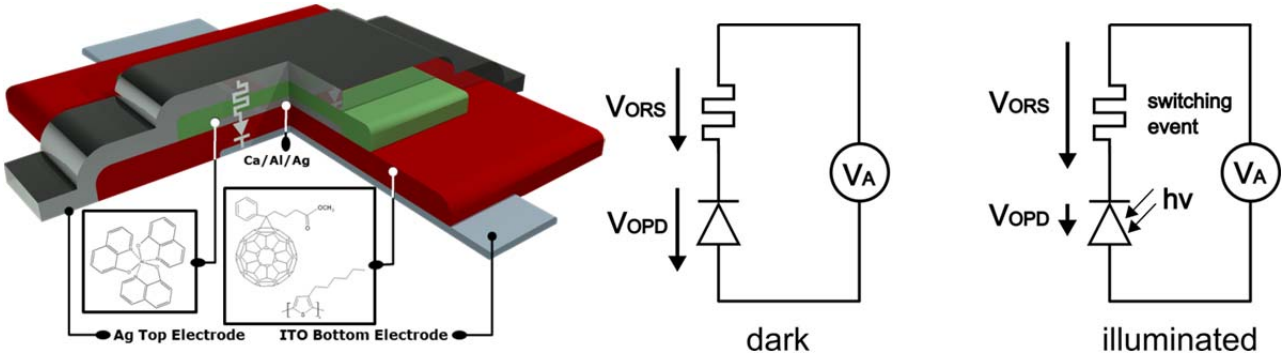


Figure 1. Schematic cross-section through a single pixel and the materials used and detection principle of a single pixel: illumination of the photodiode leads to a redistribution of the voltage drops across the two devices. This is used to trigger a threshold event which leads to a non-volatile resistance change in the resistive switching element.

4.1.3.1 Work Package 1: HYMEC Management (WP1)

The project management of HYMEC was carried out by Humboldt-Universität zu Berlin (UBER), with Norbert Koch as coordinator. He was assisted by a part-time scientific officer (Coordinator Assistant) working within the Coordinator Assistant Staff. The main tasks of the WP1 were to provide a regulated clear-cut structure for communication between HYMEC partners, the EC, and other entities. Efficient means for organizing meetings, decision-making, and overall project risk management.

During project lifetime WP1 implemented:

- Coordination between the EC and the project.
- Organized the biannual project meetings.
- Organized the midterm review meeting.
- Kept the consortium informed on the decisions taken by the different management bodies of the project.
- Created and maintained the project web page.
- Controlled the overall legal, contractual, financial, administrative and ethical management of the consortium.
- Generated cost statements and financial mediation between the EC and the partners.

The effectiveness of project management was critically important, particularly at ca. midterm of the project. At that point, it transpired that in contrast to expectations based on state-of-the-art knowledge, NV-MEs based on charge storage on metal NPs in organic matrices cannot be realized due to fundamental physics limits. The consortium developed a contingency plan in the month 15, which did not only cover the initial claims of our proposal, but even allowed to achieved more advanced functionality of devices. This revised work plan, with accordingly adjusted deliverables and milestones, was accepted by the project officer. Subsequently, no further problems were encountered and all deliverables and milestones achieved in due time.

WP1 List of deliverables and date of submission:

D1.1 Minutes of the Biannual Meetings of GB, TMC and IP Committee – (planned for **month 2**, delivered **every 6 month**)
D1.2 Annual HYMEC Meetings - (planned for every **12 months**, delivered **every 12 months**)
D1.3 Fully functional HYMEC-Webpage - (planned for **month 3**, delivered **month 3**)

4.1.3.2 Work Package 2: Single memory element fabrication and characterization (WP2)

The goal of WP2 was the fabrication, characterization, and optimization of precisely controlled single model memory elements with HYMEC hybrid systems.
The main objectives were:

- ✓ reliable fabrication protocols for active organic/inorganic hybrid layers in NV-MEs comprising controlled size and spatial distribution of metal NPs in organic matrices
- ✓ understanding of the conductance switching mechanisms of NV-MEs
- ✓ understanding of optical addressing mechanisms in NV-MEs
- ✓ knowledge-based guidelines for the optimization of NV-ME function parameters
- ✓ development of theoretical models and software to simulate NV-ME

The associated work was organized in four main tasks:

Task 2.1. Fabrication of defined model memory element structures
Task 2.2. Determination and optimization of conductance switching mechanisms
Task 2.3. Determination and optimization of optical addressing mechanisms

Task 2.4. Modelling, simulation, and verification of electrical device parameters and optical addressing

In the following, a description of the main results achieved in the individual tasks are given.

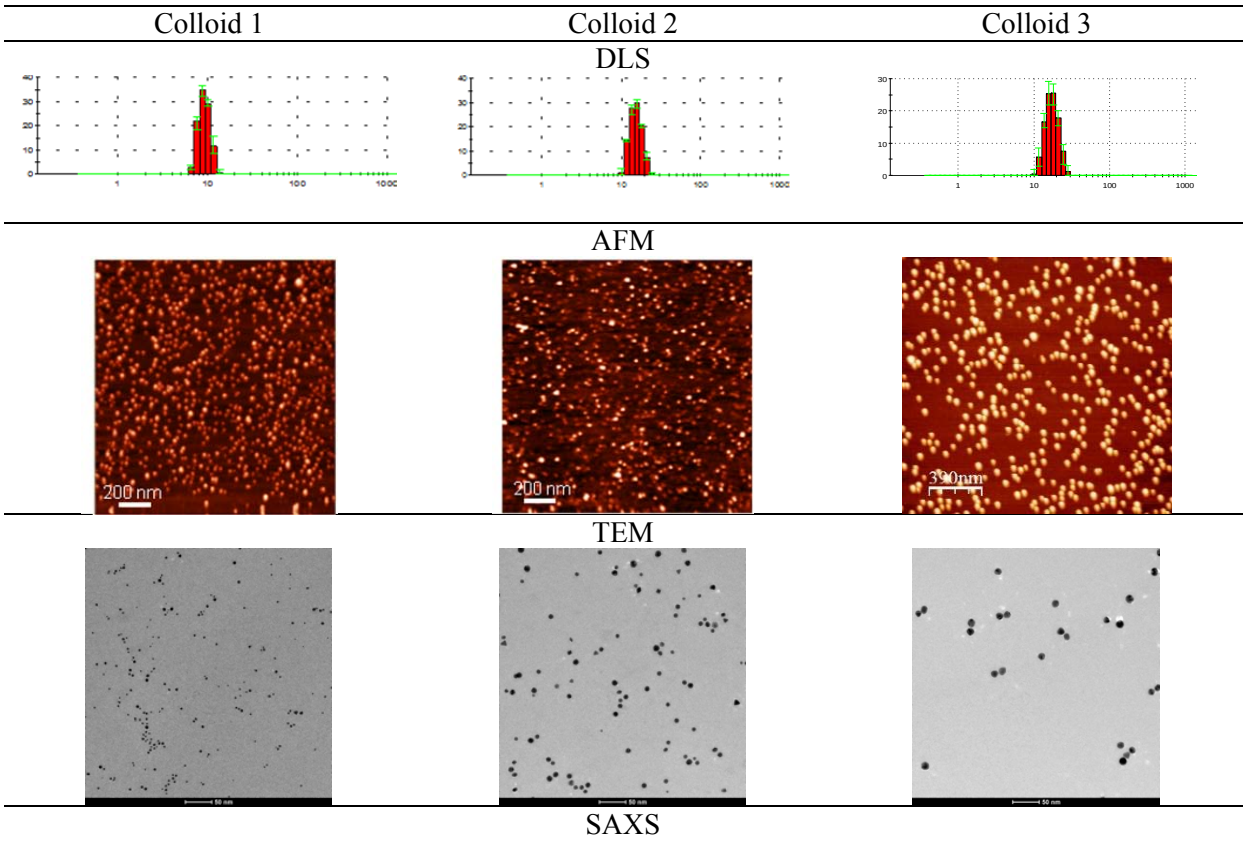
Task 2.1. Fabrication of defined model memory element structures

Synthesis of Au NP colloids

Three colloids were initially selected for solution-based approaches of the project. The monodisperse aqueous colloids of gold NPs (Au NPs) with spherical shape and the diameters: 5 nm (colloid 1), 9 nm (colloid 2) and 13 nm (colloid 3) were synthesized through a chemical reduction method.
The size and shape of aqueous colloids were investigated with Dynamic Light Scattering (DLS), Atomic Force Microscopy (AFM), Transmission Electron Microscopy (TEM), and Small Angle X-ray Scattering (SAXS). The overall characteristic of Au NPs are shown in Figure 2 and summarized in Table 1.

Table 1. The diameter of Au NPs in colloid 1, 2 and 3 obtained from DLS, AFM, TEM and SAXS, and the average value for each colloid.

Colloid no.	DLS [nm]	AFM [nm]	TEM [nm]	SAXS [nm]	Average value [nm]
1	9 ± 2	5,4 ± 1,0	5,1 ± 1,6	4,0 ± 1,0	**4,8 ± 0,7**
2	15 ± 3	9,5 ± 1,1	8,8 ± 1,7	8,0 ± 0,5	**8,8 ± 0,8**
3	18 ± 3	13,0 ± 0,8	14,0 ± 1,2	13,1 ± 0,1	**13,4 ± 0,6**



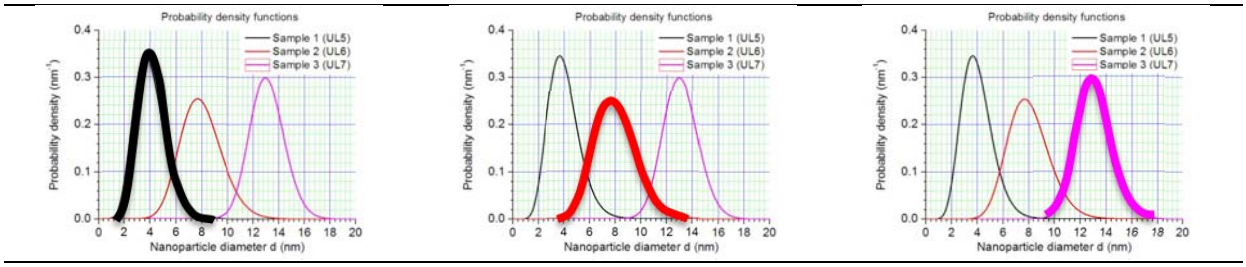


Figure 2. DLS, AFM, TEM and SAXS results of Au NPs characterization: colloid 1, 2 and 3.

In addition to the standard method for the device preparation, realized in controlled atmosphere in a glove box, an electrospray deposition method was developed.
The electrospray technique (see Figure 3) is a method for the deposition of NPs onto different substrates, i.e. device element, glass/ITO, Si/AlQ_3 or Si-wafer. The main feature of this technique is the possibility to cover the substrate with our well-characterized monodisperse NPs without a direct contact of solvent with the substrate's surface.

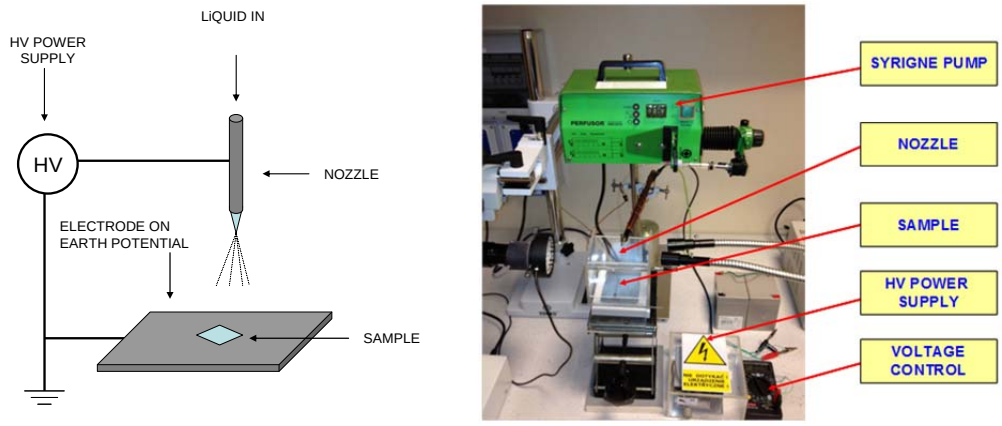
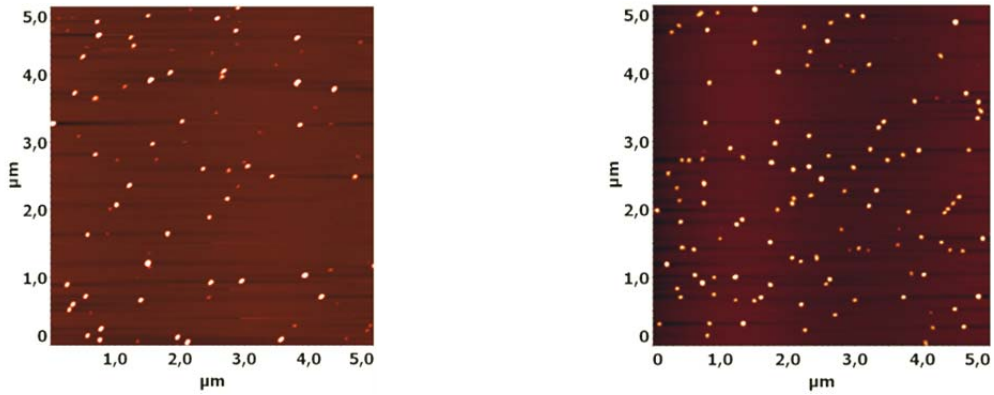
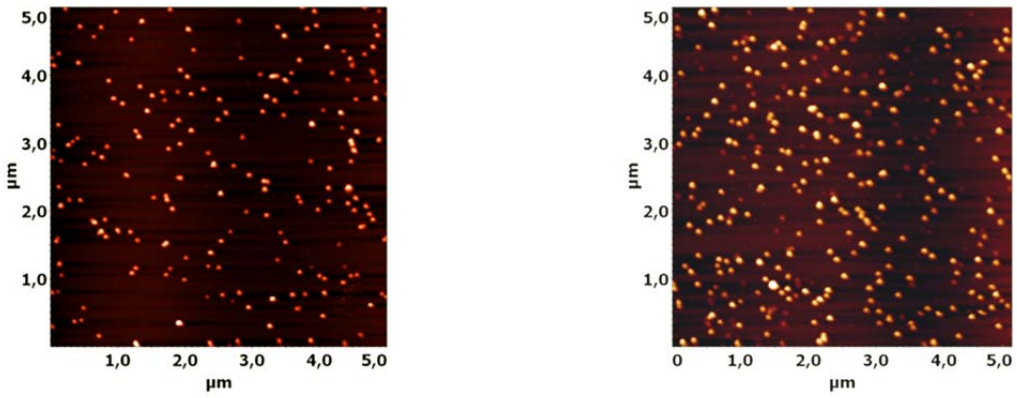


Figure 3. Scheme of the electrospray equipment for the deposition of NPs onto different substrates.

Using the electrospray technique it was possible to control the surface density of NPs on the sample by changing different electrospraying parameters. The influence of these parameters on the coverage of Au NPs on the sample was investigated (Figure 4). By increasing the deposition time, a controlled higher surface density of Au NPs is achieved.



(a) (b)



(c) (d)

Figure 4. AFM images of Si-wafers with Au NPs deposited via the electrospray technique with different surface coverage: 2% (a), 4 % (b), 7% (c), and 15% (d).

Different devices architectures realized in the project

According to the proposed research plan, six different device architectures were fabricated and characterized (see Figure 5):

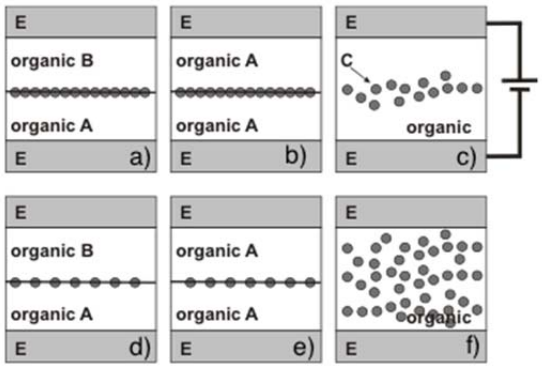


Figure 5. Schematic of the different architectures realized in the project.

The following key device parameters were used to evaluate the NV-ME functionality:

- ✓ ON/OFF ratio, i.e., the ratio between the current recorded at the same voltage in the ON (low resistance) state and in the OFF (high resistance) state;
- ✓ read/write time;
- ✓ retention time, i.e., the time during which the information (OFF or ON state of the device) is retained.

According to what was introduced in the proposal, each one of the previous device structures was fabricated, using different combinations of materials, and subsequently tested.

In WP2, the following combinations of materials were used:

#	**Structure A**
1	Al/PVK(toluene)/Al NPs/N1400/Al

#	**Structure B**
1	ITO/Alq3/Al NPs/Alq3/Ag
2	ITO/PVK/Al NPs/PVK/Ag

3	ITO/N1400/Al NPs/N1400/Au
4	Al/PVK (tetrahydrofuran)/Al NPs/ PVK (tetrahydrofuran)/Al
5	Al/PVK (toluene)/Al NPs/PVK (toluene)/Al

#	**Structure D**
1	ITO/PVK/Au NPs/PS/Ag

#	**Structure E**
1	ITO/N1400/Au NPs/N1400/Au
2	ITO/Alq_3/Au/Alq_3/Ag

#	**Structure F**
1	ITO/PS + Au NPs/Ag

These devices showed a switching behavior satisfactory for obtaining single memory elements, according to the objectives of the project.
In particular, two out of the six device architectures, namely architecture **F** (ITO/PS + AuNP/Ag) and architecture **B (**ITO/Alq3/Al/Alq3/Ag) showed the minimum targeted device performance with I_{ON}/I_{OFF} of ca. 10^5, retention times larger than 10^5 s (> 1 day), and read/write times faster than 100 µs. Thus, the milestone **M1 "Control over metal NP distribution in organic matrices"** was reached.

Task 2.2. Determination and optimization of conductance switching mechanisms

Based on the electrical as well as electro-optical characterization done at the partner NTCW, the following key features for memory devices based on ITO/Alq3/Au/Alq3/Ag was unraveled:

- ✓ The illumination of the memory device during operation or in short/open circuit conditions (over time) does not change the resistance state.
- ✓ However, for memory elements under illumination, it turns out that the open circuit voltage is significantly dependent on the resistance state, while the short circuit current is unaffected.
- ✓ In conjunction with impedance spectroscopy data, it was found that resistive switching in hybrid systems is mainly due to the formation of conductive filaments through the device. Charging / de-charging effects only play a minor role. A direct manipulation of the resistance state by light can thus not be achieved.

NV-MEs based on ITO/N1400/NP/N1400/Ag (where NPs may be of both Au and Al), showed a very reliable switching behavior and a surprising stability over time. All measurements were done in air, and after 16 months after fabrication the memory elements were working and still programmed in the on state (i.e., 16 months retention time). These devices were extensively characterized with several techniques. In particular, X-ray Photoemission spectroscopy (XPS) and Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) depth profiles (see Figure 6) were carried out on pristine and conditioned (written/erased/re-written for several times) NV-MEs to quantitatively and spatially characterize the possible metal penetration (filament formation) inside the organic layer.

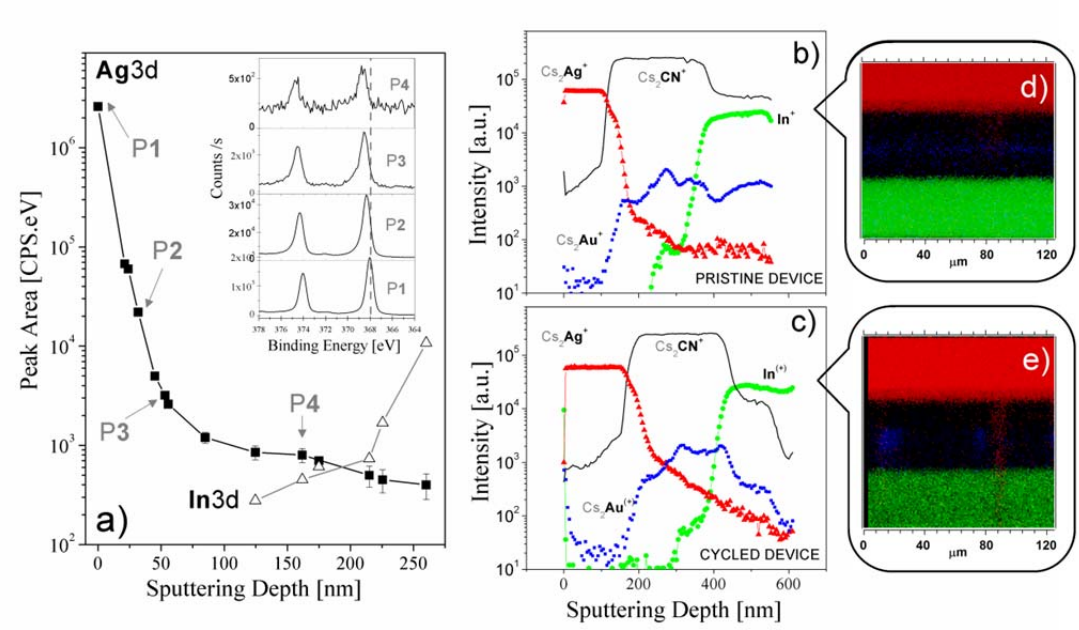


Figure 6. (a) XPS depth profile of a pristine Ag/(N1400+Au NPs)/ITO memory element showing the Ag_{3d} and In_{3d} peak area as a function of sputtering depth. The inset shows the vertically stacked HR Ag_{3d} spectra obtained at the corresponding points (depths) indicated in panel (a): the spectra are displayed with the appropriate y-scale to help the comparison. The dashed vertical line is to guide the visualization of the binding energy shifts. **(b)-(c)** ToF-SIMS depth profiles obtained on a pristine (b) and operated (c) device showing the intensity of the signal of silver ($C_{s2}Ag^+$, red triangles), indium (In^+, green dots), a N1400 fragment ($C_{s2}CN^+$, grey line) and gold ($C_{s2}Au^+$, blue dots) as a function of the sputtering depth. An enhanced Ag diffusion is evident in the operated device. **(d)-(e)** Two dimensional (XZ) cross sections extrapolated from the 3D ToF-SIMS images corresponding to (b) and (c) profiles (same color label) showing an Ag filament in the operated device.

The results clearly evidence the top electrode material diffusion inside the organic layer. Resistive switching mechanisms in devices thus must be interpreted in terms of formation and rupture of metallic filaments inside the organic layer, assisted in formation by the metal NPs. However, NV-MEs employing Au NPs are much more stable than those with Al NPs. This means that, to ensure the stability of the device, not only the organic semiconductor but also the other components must be stable. In particular, for Al NPs, it seems that the possible oxidation of the particles with time may dramatically affect the behavior of the whole structure.

Task 2.3. Determination and optimization of optical addressing mechanisms

Since within the first year of the project the investigations on single memory elements (MEs) revealed that the memory function of the majority of hybrid elements is based on filamentary nature, a direct manipulation of the resistance state by light cannot be achieved.
However, as foreseen in the project proposal the implementation of single memory elements into a device network requires an additional rectifying device in series with the memory (i.e., a diode). By shifting the optical functionality from the memory resistor to the diode, the whole proposed functionality could be achieved without limitations of the overall system performance (see WP5 below for full details).

Task 2.4. Modelling, simulation, and verification of electrical device parameters and optical addressing

The aim of this task was to develop a numerical theory tool to understand the physical mechanisms and to assist the development of memory devices. This objective required the understanding of electrical properties of organic materials and the development of proper models for the involved physical processes.

Two main mechanisms have been recognized for the resistive switching: (1) highly conductive and localized pathways (usually called filaments) can be formed inside the organic matrix through migration of metal atoms[2]; (2) NPs can act as charge trap sites (or induce trap states in the organic around them), and bistability is an effect of the trapped charge[3].
For the modelling of the charge transport in organic materials we use a semi-classical approach based on drift-diffusion equations coupled to the Poisson equation for the electrostatic potential; the model was developed within the TiberCAD simulation tool[4].

Resistance switching: space charge models

In Ref. 5 we studied three different charge trapping models of resistance switching in organic bistable devices with embedded NPs, and provided from literature several experimental evidences supporting each model.

1. *Space charge*. The formation of a space charge potential limits the transport of charge carrier of the same sign, thus reducing the current.
2. *Induced doping*. Trapped charges dope the organic, thus increasing the density of carrier of the opposite sign.
3. *Shockley-Read-Hall* (SRH) recombination. Trap states act as recombination centers. Once a fixed space charge is present around recombination centers, SRH recombination is suppressed, hence the current is raised.

Charges can be trapped and de-trapped controlling the applied voltage, thus switching the device and induce the bistability. We found that these effects are always concurrent, and the global effect is determined by the prevailing one.

Resistance switching: filament model

The filamentary mechanism is a very common process in resistance NV-MEs and it has been suggested to be the main switching mechanism in a large class of NV-MEs using both organic and inorganic semiconductors[6]. Filament forming is electrically driven: applying an external bias the internal electric field moves the ions growing the filament. The metallic phase of the filament is also less stable than a real metal. This means that the natural Joule dissipation of current converted into heat can provide enough energy to the ions in the filament to make them diffuse away and dissolve the filament (see Figure 7). This process starts beyond a temperature threshold. The "shrinking" of the filament diameter produces a reduction in the current carried by the filament with a consequent negative differential resistance (NDR). The higher the voltage the faster the dissolution. For a bias large enough the filament is eventually broken leading to an ON -> OFF transition. For an intermediate bias the filament is not completely, but only partially destroyed leading to an intermediate state.

The main achievements of our efforts were the following:
1. Development of an *organic model within drift-diffusion approximation* (tested with experimental measurements) for the entire device.
2. *Parameterization of organic materials* used in device fabrication (e.g., Alq3, α-NPD).
3. Development of two *charge mechanisms* to include the effect of charged NPs in order to simulate space charge limited current NV-MEs.
4. Investigation of switching mechanisms of experimental devices. Conclusion that the switching mechanism observed is mainly due to *filament formation* (thermochemical switching).
5. Implementation of a multiphysics model to describe *filament degradation* and negative differential resistance (NDR) in fabricated memory devices. The model has been compared to experimental measurements for the ON state and the ON -> OFF transition.

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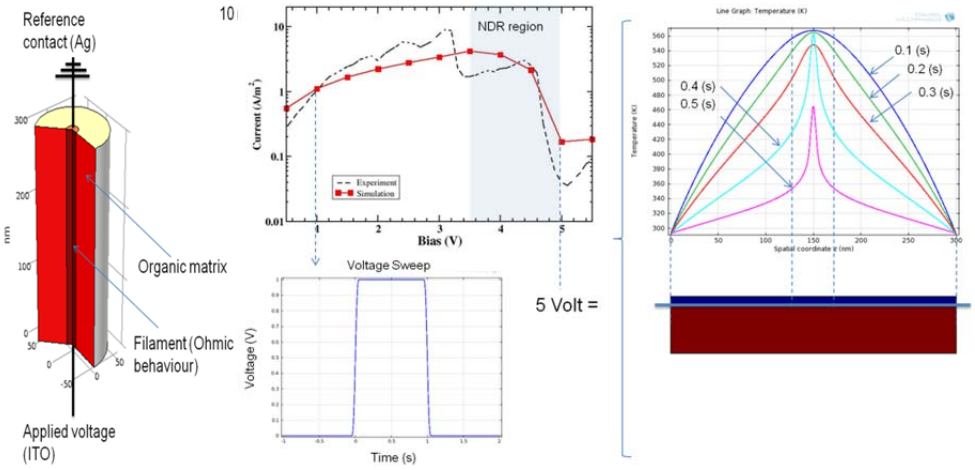


Figure 7. (left) Simulated device structure. (Top, center) comparison between experimental and simulated IV curves for the ON state of the memory device. (Bottom, left) voltage sweep applied at every voltage point. (top, right) temperature profile at different time steps (5 Volts) at the boundary between filament and organic semiconductor.

List of deliverables and date of submission:

D2.1 Characterization of single memory elements (planned for **month 12**, submitted in **month 12**)
D2.2 Fabrication guidelines for stable morphology and composition of single memory elements (planned for **month 12**, submitted in **month 12**)
D2.3 Optical manipulation of single memory element conductance/charge storage (planned for **month 18**, submitted in **month 18**)
D2.4 Model to simulate electrical characteristics of steady-state transport (planned for **month 18**, submitted in **month 18**)
D2.5 Optimization guidelines (planned for **month 24**, submitted in **month 24**)
D2.6 Inclusion of the effect of filament formation in the macroscopic device modelling tool (planned for **month 24**, submitted in **month 24**)

List of milestones and date achieved:

M1: Control over metal NP distribution in organic matrices (planned for **month 12**, achieved in **month 12**)
M2: Single memory element with specifications (planned for **month 15**, achieved in **month 15**)
M3: Identification of reliable conductance switching mechanisms (planned for **month 18**, achieved in **month 18**)
M4: Identification of reliable optical addressing mechanisms (planned for **month 18**, achieved in **month 18**)
M5: Decision if series-diode is needed (planned for **month 18**, achieved in **month 18**)

4.1.3.3 Work Package 3: Morphology, structural, electronic, and optical properties (WP3)

WP3's objective was to obtain a comprehensive knowledge of relevant morphological, structural, electronic, and optical properties of HYMEC non-volatile memory elements (NV-ME) by combining the use of state-of-the-art in-situ and ex-situ analysis techniques.

Key objectives of WP3 were to reveal:

- ✓ The size distribution and spatial distribution of metal NPs in organic matrices of model HYMEC systems, of NV-ME arrays, and of those integrated with other functions (from WP2, 4 and 5, respectively).
- ✓ The electronic structure and optical properties of the same model systems, arrays, and devices.
- ✓ The electronic structure of HYMEC systems at metal electrodes.
- ✓ The properties of idealized HYMEC systems sublimed in ultrahigh vacuum vs. fabricated in application relevant environments from solution.
- ✓ The influence of aging and operation under electrical stress on the stability of NV-MEs.

A large variety of structures and architectures were explored in the early stage of the project, starting from model hybrid layers, where metal NPs are deposited via different methods/conditions on organic thin layers, to fully operational NV-MEs, which were accurately electrically characterized. The materials selected and mainly studied in the second period of the project are based on:

- ✓ *Organic semiconductors*: Tris-(8-hydroxyquinoline)aluminum (Alq_3) and N-N-Di(naphthalene-1-yl)-N,N'-diphenylbenzidine (α-NPD) deposited by thermal evaporation
- ✓ *Polymer materials/Inks*: Polystyrene (PS), Polymethyl-Methacrylate (PMMA), N1400 Polyera deposited by spin coating or printing techniques.
- ✓ *Metal NPs*: chemically synthetized Au and Al NPs with controlled size, or metal deposition with sputtering, thermal evaporation or electron beam deposition.
- ✓ *Bottom Electrodes*: ITO coated glass or PET.
- ✓ *Top Electrode*: Ag, Au, Al deposited by thermal evaporation or printing.

A huge variety of in-situ and ex-situ experimental techniques was adopted to fully characterize the variety of organic semiconductors (polymers and molecules), metal NPs and metal contact.
In the first phase, the major efforts were focused to characterize the NP's size distribution, the oxidation state and the lateral homogeneity in a layered and homogeneous structure (see structure in WP2). To this end modern techniques like Atomic Force Microscopy (AFM), Scanning Electron Microscopy (SEM), X-ray Photoelectron Spectroscopy (XPS), X-ray Scattering (GISAXS and XRSR) and High resolution (Scanning) Transmission Electron Microscopies (TEM - STEM) were adopted. The investigation on hybrid layers or sandwich organic/metal/organic structures allowed reliably producing and depositing metal NPs with controlled size ranging from < 1 nm to 15 nm on various organic layers (see Figure 8 and Figure 9). Furthermore, the electronic structure of the selected materials, such as the electronic energy levels of the organic with respect to the electrode Fermi-level, the position of the frontier unoccupied levels (by using the charge transport gap), and the corresponding hole and electron injection barriers between organic semiconductors and electrode materials were studied (see Figure 10) with Ultraviolet Photoelectron Spectroscopy (UPS).

Following the contingency plan after month 15, WP3 efforts focused on the identification and characterization of metal filaments in hybrid NV-MEs provided by WP2, WP4, and WP5 partners. The filamentary nature of resistive switching, which resulted from the I-V characteristics of all device architectures studied in the first period of the project, allowed exploring low-cost and solution processed NV-MEs based on polymers or hybrid inks. In particular, Polystyrene (PS) and Poly(methyl methacrylate) (PMMA) based NV-MEs were selected for fabricating solution processed organic or hybrid (including chemically synthesized Au or Al NPs) NV-MEs. Inkjet-printed devices including printed top electrodes were extensively characterized in WP3.

WP3 particularly focused on describing filament formation in the materials and architectures, which were finally selected for array realization, based on Tris-(8-hydroxyquinoline)aluminum (Alq_3) and PMMA. In parallel, N1400 based hybrid NV-MEs were explored through the entire project, motivated by their interesting switching properties and air-stability. A comprehensive study of filament formation mechanisms and their evolutional stages during the electrical conditioning was provided by spectroscopic analysis with XPS and ToF-SIMS. ToF-SIMS 3D imaging was applied to detect atomic and molecular species with high sensitivity and spatial resolution, with an in-plane resolution of about 1 μm and in-depth resolution of about 1 nm.

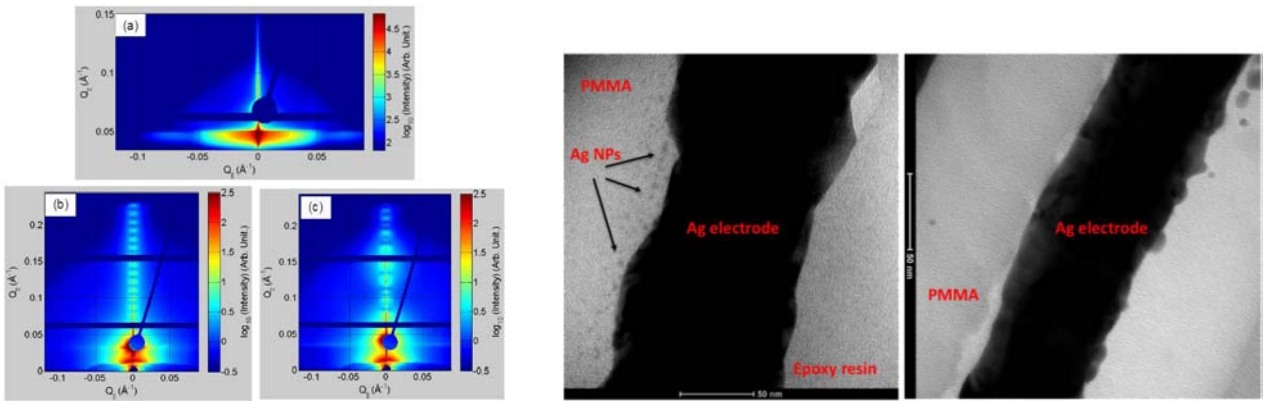


Figure 8: (left) GISAXS reciprocal space maps measured on chemically prepared Au NPs physisorbed on Si substrate (a), Alq3 layer (approx. 60 nm) on Si substrate (b), and Si/Alq3 (30nm)/Al (15nm)/Alq3 (30 nm) multilayer (c). (right) TEM micrograph on Alq3 thin layer top coated with different nominal Au thicknesses, resulting in Au NPs with defined size distribution.

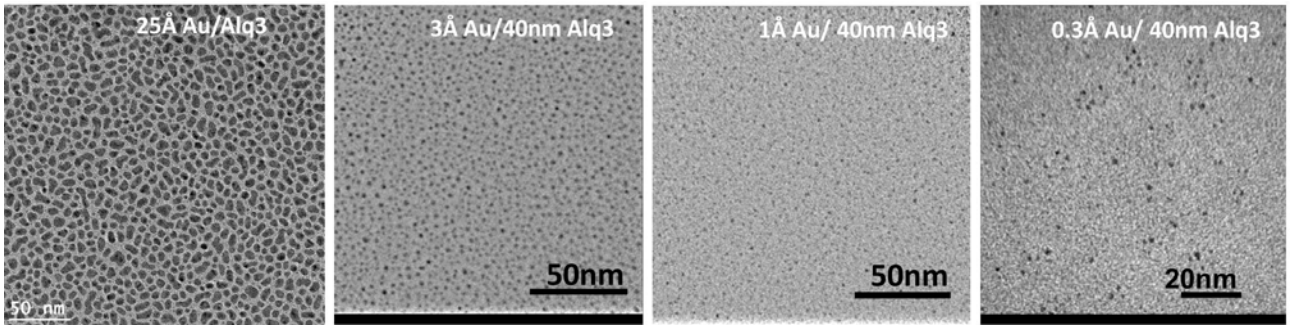


Figure 9. Cross-sectional views of the Ag/PMMA hybrid layers. The Ag was deposited at different evaporation rates. Clearly, for a slow (0.3 nm/min) evaporation rate, we observe the presence of Ag NPs beneath the Ag/PMMA interface. No metal diffusion is observed for the fast (60 nm/min) evaporation rate. The Ag NPs are formed over a 20-30 nm depth in the PMMA matrix and their size can reach a few nm in diameter.

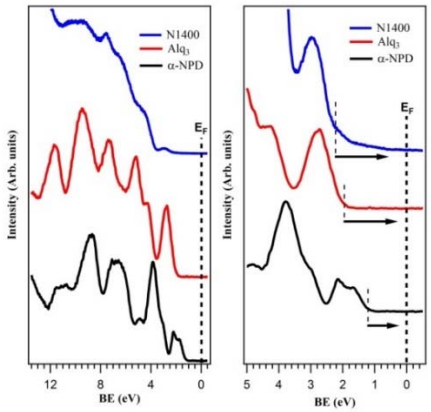


Figure 10. UPS spectra of 50 Å α-NPD, Alq_3 and N1400, respectively, on ITO. The right image shows a close up of the HOMO level region for all three materials.

Pristine (as deposited) and electrically stressed memory elements were analyzed with ToF-SIMS to discriminate between the metal diffusion in the organic layer due to the top electrode deposition process and the additional field-induced diffusion caused by the electrical addressing. This analysis allowed concluding on filament formation mechanisms in all the structures employed in WP2 and WP4.
Depth profile investigations were completed by more fundamental studies on metal and clusters diffusion by Electron Microscopy (TEM/SEM) tomography and X-Ray Reflectivity.

Filament formation and dynamics in Alq3 based NV-MEs

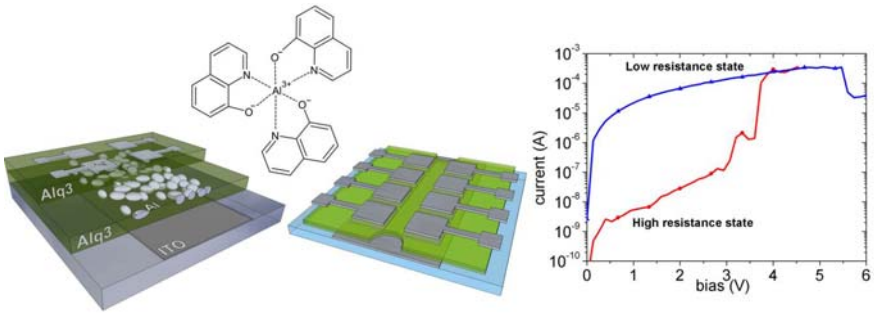


Figure 11. Example of NV-MEs devices structure (left) and typical I-V characteristic of an organic memory element with a printed silver bottom electrode (right).

Hybrid layers and devices based on Alq3 were investigated by numerous techniques to characterize metal diffusion and the processes leading to filament formation. Depth profile analysis with XPS on ITO/Alq_3/Ag NV-MEs evidenced that filament formation involves the diffusion of a small quantity of metals. The top electrode deposition leads to Ag diffusion in the organic matrix; very small differences could be detected between devices set in different final resistance state. The high indium (In) signal on the top electrode surface testifies the high mobility of In ions through the device.
By comparing the ToF-SIMS profiles from pristine and cycled devices, the Ag diffusion in the organic is found to increase up to 65% in cycled devices. 3D reconstructions suggest that such inhomogeneous diffusion occurs through abundant micron-sized tip-like regions, appearing as bright spots in the Ag XY maps. Silver XY maps, generated by integrating the signals from the Ag 2D images acquired at each profile step, reveal *spots* in pristine and electrically stressed devices. In pristine devices, these filamentary paths extend up to 150 nm beneath the Alq_3/Ag interface, whereas in cycled devices, the additional field assisted opposite diffusion of the top (Ag) and bottom (In, O, Sn) electrode ions, lead to the establishment of fully connected paths which electrically bridge the two electrodes. These filaments are thought to locally break at the memory erase, and new ones are formed in the successive memory reset process. The reliability of Alq3 based NV-MEs is suggested to rely on the abundance and easy forming of such *ready-to-switch* filaments.

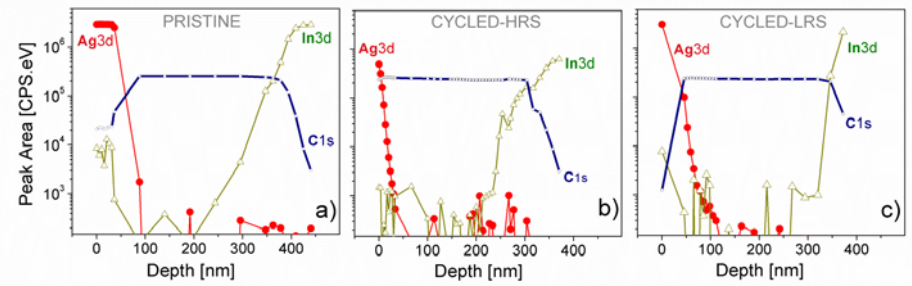


Figure 12. XPS depth profiles of ITO/Alq_3/Ag memory elements showing the Ag3d, C1s and In3d peak area as a function of the sputtering depth. The memory devices were as deposited (a), set after few cycles in the high resistance state (HRS) (b), and in the low resistance state (LRS) (c). Far beneath the Alq_3/Ag interface, the Ag atomic percentage is about 0.1 at% compared to carbon (99.9 at%).

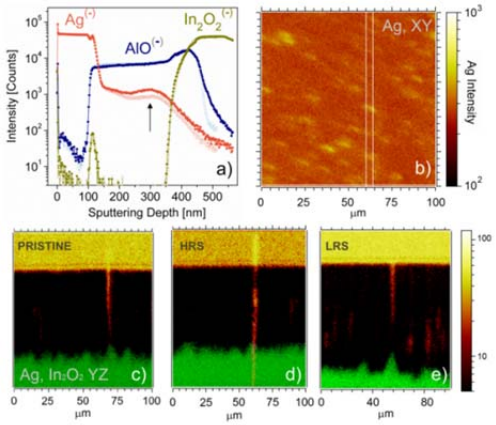


Figure 13. (a) ToF-SIMS depth profiles and imaging on pristine (open symbols) and cycled (solid symbols) ITO/Alq_3/Ag memory elements. The signal intensity of silver (Ag^-, in red), indium ($In^2O_2^-$, in green), and an Alq_3 molecular fragment (AlO^-, in blue) is shown as a function of sputtering depth. The black arrow indicates the enhanced Ag^- diffusion in the cycled device. (b) Silver 2D map from a cycled-LRS device showing the Ag^- signal integrated over the entire profile depth. The high intensity spots indicate areas of Ag diffusion. Very similar maps were obtained in pristine and cycled-HRS elements. Bottom panels show Ag filaments as observed in YZ cross-sections selected in the Ag maps, as indicated by the vertical lines in (b), displaying together the Ag^- and $In_2O_2^-$ signals distribution. Typical filaments observed in a pristine (c), cycled-HRS (d), and cycled-LRS (e) memory elements are shown.

Filament formation and dynamics in polymer based memory devices

The top electrode (TE) diffusion in ITO/Polymer/TE structures was determined in PS, PMMA and N1400 NV-MEs by XPS depth profile analysis. The metal distribution follows the general trend as shown in Figure 14. In electrically stressed devices, such diffusion was found to be slightly enhanced, but a quantification with XPS was not possible.

ToF-SIMS 3D Imaging of ITO/PPS/Ag (Figure 15) and ITO/PMMA/Au (Figure 16) NV-MEs indicate a fairly similar filament dynamics (formation/rupture). For both polymer devices, strong diffusion *spots* in XY maps of the top electrode material indicate the presence of filaments. The intensity, density and area of such spots were lower compared to what observed in Alq3 based NV-MEs, suggesting a different filament dynamics.

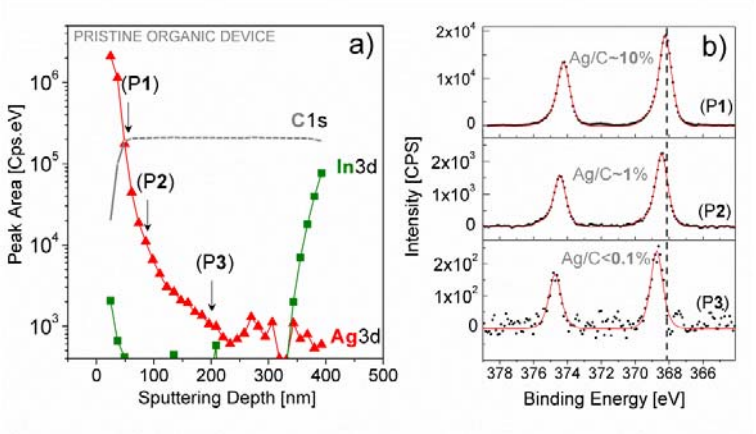


Figure 14. a) Typical XPS depth profile from ITO/PS/Ag memory showing the Ag3d, C1s and In3d peak area as a function of sputtering depth. b) Ag3d HR spectra obtained at the depths P_i marked in a); the vertical line evidences the binding energy shift of the Ag3d peak occurring in nm-sized supported clusters**.** The average metal concentration in the polymer layer decreases to about 1 at% (with respect to carbon) at about ~100 nm beneath the Polymer/TE interface.

In pristine polymer memory devices, *pre-filaments* are found to originate from defects in the polymer layer (seen by cross-sectional SEM analysis). Such inhomogeneous metal diffusion is enhanced by the I-V conditioning (forming step), and *ready-to switch* filaments are possibly formed. I-V characteristics suggest that one spot in the XY maps can include multiple individual conductive paths (filaments) which are activated and ruptured during the memory addressing. Filament inactivation is proposed to occur by a local degradation of the top and/or bottom electrode, or the entire spot region. The filament rupture was found to be strongly

influenced by the operating atmosphere; in reactive atmosphere filament rupture occurs at lower bias; when the erase occurs at a sub-threshold bias the device and functionality is lost, but it can be recovered by flushing the device with inert (N_2) atmosphere. This demonstrates the role of thermochemical processes in filament degradation.

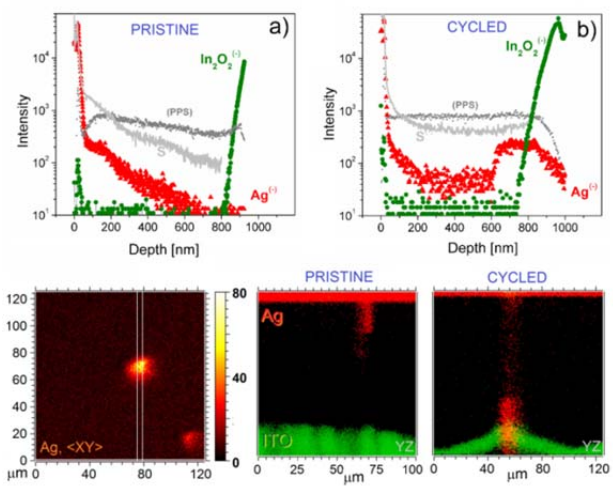


Figure 15. (**top** a-b) ToF-SIMS depth profiles and imaging on pristine and cycled ITO/PS/Ag memory elements. The signal intensity of relevant ions is shown as a function of sputtering depth. (**bottom**) Silver 2D map from a cycled device showing the Ag^- signal integrated over the entire profile depth. The high intensity spots indicate areas of Ag diffusion. Silver filaments as observed in YZ cross-sectional reconstructions selected from the Ag map, (vertical lines) displaying together the Ag^- and $In_2O_2^-$ signals. Typical filaments observed in pristine and cycled memory elements are shown.

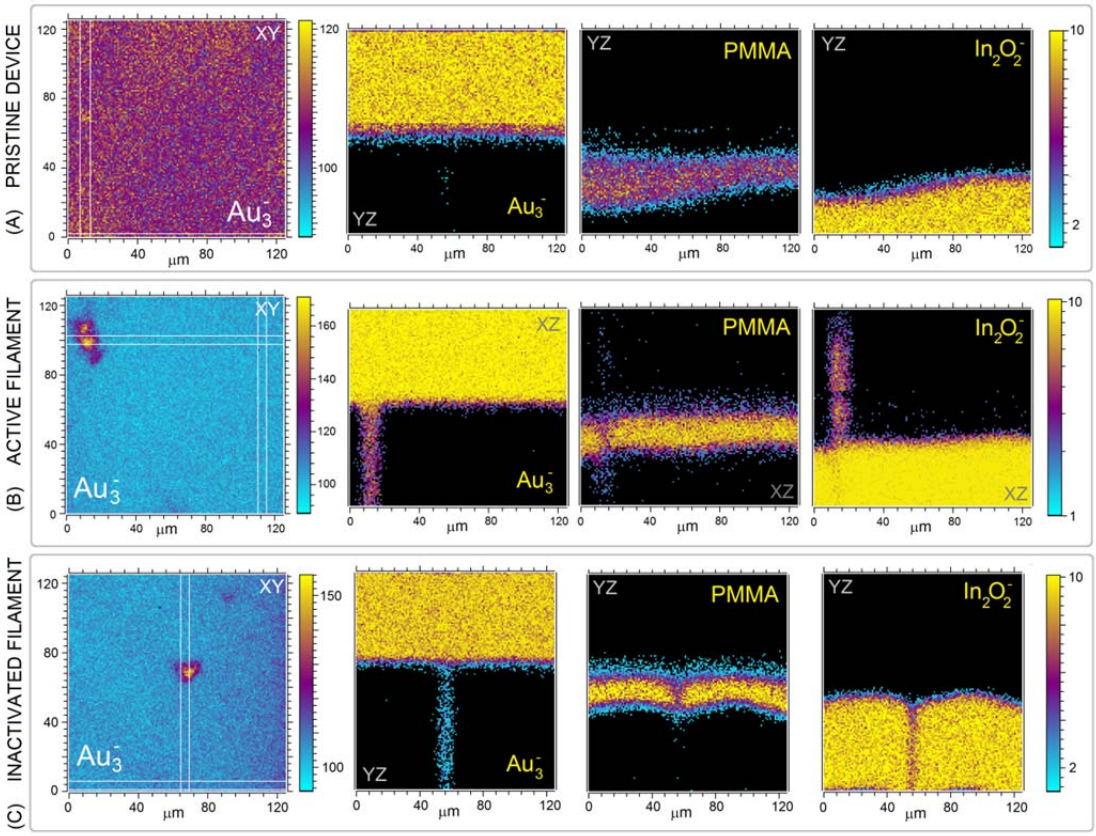


Figure 16. ToF-SIMS 3D imaging on a pristine (A), cycled-ON (B), and cycled-OFF (C) device. The left panel shows the Au_3^- XY map; the high intensity spots indicate the region where an enhanced Au diffusion occurred. The Au_3-, PMMA, In_2O_2- signals reconstruction along the YZ and XZ cross-sections as indicated in the images.

The cluster distribution/size was finally investigated in PS and PMMA hybrid layers and devices by cross-sectional TEM/STEM (Figure 17). In ITO/PS/Ag-IML/PS/Ag devices, bright-field (BF) STEM cross-sections reveal a bimodal distribution of Ag NPs in the IML confined within about a 50 nm wide stripe. High angle annular dark field (HAADF) STEM analysis allows detecting small NPs (<4nm) close to the bottom electrode in pristine and cycled devices. Such small Ag NPs may have the sufficient mobility to support the formation of Ag filaments that were evidenced by ToF-SIMS.

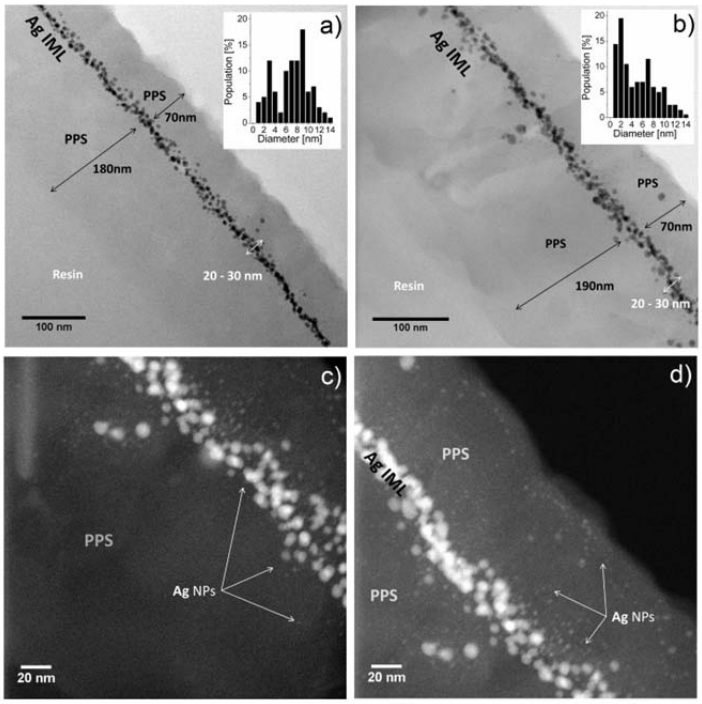


Figure 17. STEM cross-sections obtained on pristine (a, c, d) and cycled (b) hybrid devices. a) and b) are BF-STEM images; the size distributions of the Ag NPs evaluated on the respective micrographs are shown in the insets. c) and d) are STEM-HAADF images. Note that due to the poor metal adhesion the top electrode was frequently delaminated during the cutting procedure, thus does not appear in the top right part of the images.

ITO/PMMA/Ag (30nm) NV-MEs set in defined resistance states were analyzed with SEM (Figure 18). SEM images indicate that the PMMA layer contains some hollow cavities (dark round structures in the PMMA layer). Some of these cavities extend over almost the entire thickness of the PMMA film. These defects seem to correspond to trapped air bubbles in the PMMA films generated during the spin-coating process. Surprisingly, the top metal layer does not show any discontinuity at the level of the cavities in the PMMA film. This suggests that the metal stands on a very thin PMMA layer which is present over the cavity.

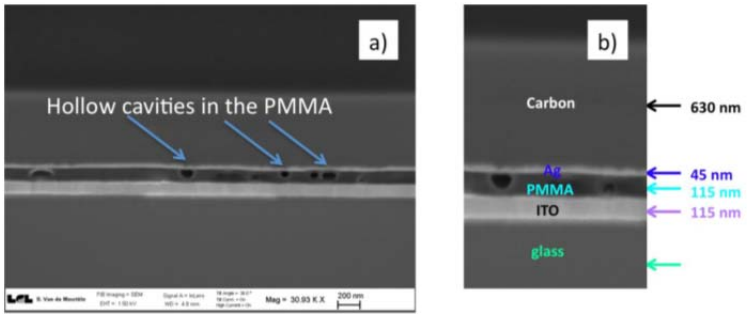


Figure 18. a) and b) SEM images of Ag/PMMA/ITO devices after Focused Ion Beam (FIB) thinning. The hollow voids in the PMMA films are highlighted.

List of deliverables and date of submission:

D3.1 Semestrial morphological/structural analysis report on model hybrid systems (planned for **month 6**, submitted **every 6 months**)
D3.2 Charge injection barriers for organic matrix materials on electrodes (planned for **month 12**, submitted in **month 12**)
D3.3 Chemical interaction of vacuum-deposited metal NPs with organic matrices from WP2 (planned for **month 16**, submitted in **month 16**)
D3.4 Energy level alignment in hybrids (planned for **month 18**, submitted in **month 18**)
D3.5 Report on basic packaging requirements of devices from WP4 and WP5 (planned for **month 24**, submitted in **month 24**)

List of milestones and date achieved:

M6: Experimental characterization methods are adapted (planned for **month 12**, achieved in **month 12**)
M7: Established reliability of HYMEC systems physical parameters for correlation with device function (planned for **month 18**, achieved in **month 18**)

4.1.3.4 **Work Package 4:** Memory element array fabrication and characterization (WP4)

The overall objective of WP4 was the realization of memory arrays from single non-volatile memory elements as fabricated, characterized and investigated in WP2. The focus of WP4 was:

- ✓ Fabrication and testing of NV-ME memory arrays (from 2 x 2 up to 32 x 32) demonstrating the possibility to integrate single NV-MEs to memory arrays in a crossbar wiring.
- ✓ Low cost fabrication of memory arrays (2 x 2 up to 32 x 32) by inkjet printing.
- ✓ Miniaturization of single NV-MEs and 2 x 2 memory arrays to nanoscopic levels to test for the overall limits and the corresponding electrical device parameters.
- ✓ Investigation of fabrication and production techniques for NV-MEs such as lamination to demonstrate alternative low cost fabrication processes for high storage density memory arrays.

General aspects of resistive array structures

Figure 19 (left) displays the unipolar N-shaped I-V characteristics of an organic resistive memory device, which is mainly independent on the specific device configuration and materials. The device is initially in its high resistance state (HRS, OFF-state). Upon a characteristic voltage (current threshold voltage, V_T) a steep increase in current can be observed, which is assigned to the formation of a highly conductive filament through the organic layer. The threshold is followed by a region of negative differential resistance (NDR) where a gradual increase of bias leads to a decrease of current. This distinct behavior is assigned to a local degradation of the filament. Reversing the voltage sweep direction, the memory clearly exhibits a low resistance state (LRS) for voltages below V_T. Typical devices show a ratio of several orders of magnitude between the ON and the OFF state. This ratio can be adjusted by changing the resistance along the organics (e.g., by increasing layer thickness) and thus reducing I_{OFF}. The individual memory states can be addressed by applying a voltage pulse around V_T to write (filament formed) or at the end of the NDR to delete (filament ruptured). The read-out is performed by measuring the resistance at a bias well below V_T (1.5 V). By selectively applying a voltage in the NDR-region or a current compliance during switching, intermediate states between the LRS- and HRS-state can be written, forming a quasi-continuum of memory states.
The integration of such a 2-terminal resistive device into crossbar arrays as depicted in Figure 19 (right side) would inevitably lead to parasitic cross-talk during addressing of single elements caused by current bypasses through adjacent non-addressed elements in their HRS. To overcome this issue, an additional selector device has to be integrated in series with each cell. For unipolar resistive switches this element can be a rectifying diode. In contrast to a planar transistor, a rectifier is also a 2-terminal device and therefore does not limit the $4F^2$ integration footprint. Due to the unique memory device properties the individual organic diode has to provide low onset voltage (< 1 V) and a forward current higher than I_{ON} of the ORS. The diode should not act as a bottleneck for any of the memory functionalities in forward direction. Also a low reverse current is required. Under reverse bias, all memory related properties should vanish and reverse current of the OD should dominate, enabling for a proper blocking of cross-talk stemming from neighboring elements.

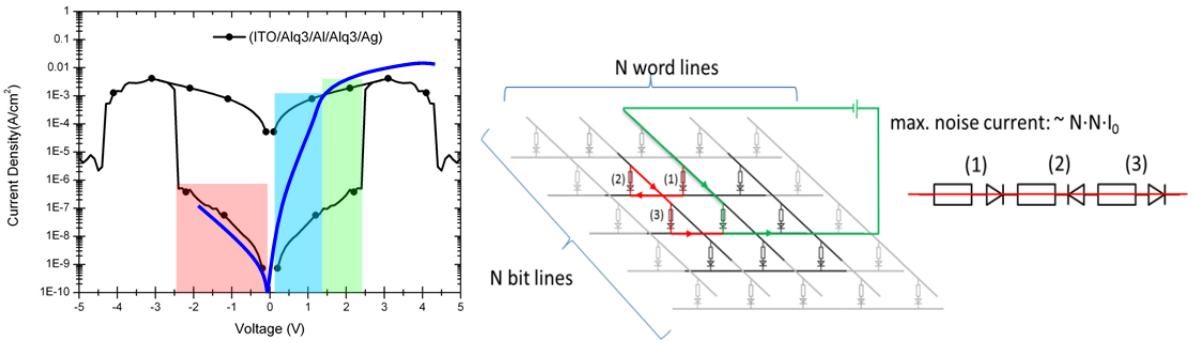


Figure 19. Left: The black I-V characteristic shows a typical unipolar memory device behavior. To operate the individual memory devices without limitations by the diode an ideal diode characteristic was added as indicated by the blue line. The individual operation modes are indicated by red (reverse direction), blue and green squares (read operation). Right: Illustration of the origin of parasitic noise current in crossbar array structures. The green line highlights the desired current pathway, while the red line shows one of the possible parasitic pathways (at least three

nodes - and always an odd number is involved in such a current bypass). A maximum noise current in the order of N^2*I_0 (with N, the number of bit and word lines) can be estimated from this argumentation.

Requirements for the diode:

- Reverse current (red region)
  The reverse current of the diode equals the maximum noise contribution from a single node in an array. If this value is too high, the total noise from all nodes in the memory array outnumbers the actual measurement signal (especially for the high resistance state), and a proper read-out of the state is not possible.
- Low onset voltage and steep slope (blue region)
  A low diode onset voltage guarantees that the full ON/OFF ratio of the memory device can be used without reducing the read-out margin.
- Forward diode currents (green region)
  Since the reset operation of a memory device requires a specific current typically larger than 500 µA to burn the filament the diode has to provide this current for proper operation. On the other hand a forward current smaller than the low resistance state current of the memory, shrinks the obtainable ON/OFF ratio.

A noise path must cross an odd number of elements (at least 3) with alternating polarity of the diode, which means that the path includes at least one diode polarized in reverse. Each node can thus provide a current limited by the reverse current I_0 of the diode. Any device collects the current from all the N-1 elements on the same electrode line, thus a maximum noise current for every element is in the order of $N \cdot I_0$. Multiplying this with N lines in the array an upper boundary (worst case) for the noise current in the order of $N^2 \cdot I_0$ can be obtained. Nevertheless, the state of a single memory element can be read out correctly, even if the HRS of the memory is below the noise threshold: If the read pulse leads to a high current, the element is in its LRS (ON state). If the maximum noise current (or smaller) is detected, the element can be considered to be in its HRS (OFF state). Therefore, for arrays an adapted I_{ON}/I_{OFF} ratio, the ON-to-maximum-noise ratio (R) is of interest (equation 1).

$$R \sim \frac{I_{ON}}{N^2 I_0} \quad R \sim \frac{I_{ON}}{N^2 I_0} \tag{1}$$

Already for rather small array sizes, equation 1 implies the need for a high performance rectifying diode with maximum reverse current in the order of several nA to ensure a moderate R value of 100.
To achieve these strict requirements with an organic schottky diode, several issues have to be considered:

- ✓ the **organic material** has to exhibit **high charge carrier mobility** (like Pentacene or P3HT)
- ✓ the **electrode configuration** has to be **highly asymmetric:** anode side high work function materials (e.g. Au, MoO_3); cathode side low-work-function materials (e.g. Ca, LiF)
- ✓ **low leakage current** of the diode (thickness of the organic layer > 500 nm).

With respect to the main array target applications:

- ✓ light inducted devices state manipulation,
- ✓ array sizes up to 32 x 32 (1024 single 1D-1R elements), and
- ✓ low cost printing production techniques

two different organic diode systems were investigated and optimized with respect to the memory device requirements. Apart from solution based P3HT:PCBM diodes, allowing for light induced memory device state manipulation, special emphasis was laid on pentacene diodes systems for the realization of structured array demonstrators.
For the described PCBM:P3HT photodiodes (Figure 20, left), I-V curves from devices with six different electrode sizes are shown in **Figure 20** revealing a clear dependence of the overall current on the size of the electrode area. In contrast to PCBM:P3HT photodiodes ITO/PEDOT:PSS/pentacene/Ca/Al Shottky (Figure 20, middle) diodes showed significantly enhanced forward currents as well as reverse currents with a less

pronounced dependency on the active electrode size. Additional, as shown in Figure 20 (right) TIPS pentacene based diodes have been prepared and characterized.

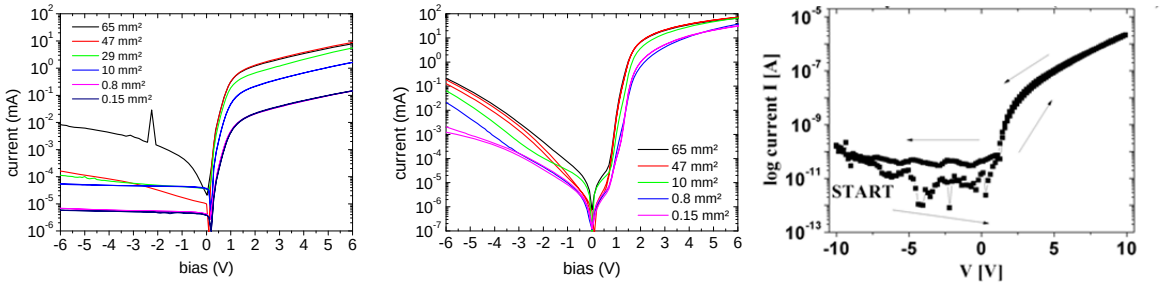


Figure 20. I-V characteristic of a ITO/PCBM:P3HT/Ca/Al (left) and a ITO/PEDOT:PSS/pentacene/Ca/Al device (middle) as a function of the electrode size and an a PET/Au/TIPS-pentacene (one layer 1 wt% toluene)/Al with an inkjet-printed active layer device.

Although successfully prepared, printed diodes with TIPS pentacene as active material shows a too small forward current (by several orders of magnitude) to switch the memory device from its LRS back to its HRS mainly due to the lack of a an inkjet-printable low-work-function ink for the cathode side. Since the current in the ON state of the resistive devices is mainly independent on the memory footprint the diode is the miniaturization bottleneck in a 1D-1R stack.

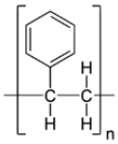
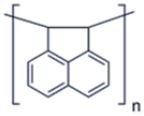
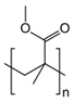
Preparation and characterization of inkjet-printed NV-MEs array structures

Apart from standard device preparation (spin coating and physical vapor deposition), alternative production methods such as inkjet printing are in the scope of this project and inkjet-printed single as well as array structures of memory devices were extensively characterized.

Ink formulation/characterization

In a first step, the interplay between the different surfaces and solvents on the film formation under various preparation conditions was investigated. The main focus within these activities was on the formulation and characterization of organic inks for the active device layer. Apart from pure organic inks mainly based on polystyrene (PS), polyacenaphthylene (PAH), poly(methyl metacrylate) (PMMA) (see physicochemical properties in Table 2), also blend systems of these materials with gold NPs were tested (Figure 21).

Table 2. The physicochemical properties of polymers used as a matrix for ink composition.

Property	PS	PAH	PMMA
Name	polystyrene	polyacenaphthylene	poly(methyl metacrylate)
Formula			
Molecular weight (M_w)	2,500	5,000 – 10,000	-
Density [g/cm^3]	0.96-1.04	1.05 – 1,10	1.18-1.20
Melting point [° C]	240	291	160
Glass transition temperature (T_g) [°C]	~ 90	~ 214	~105
Dedicated solvent	toluene	toluene	anisole, (1-methoxy-2-propanol acetate)

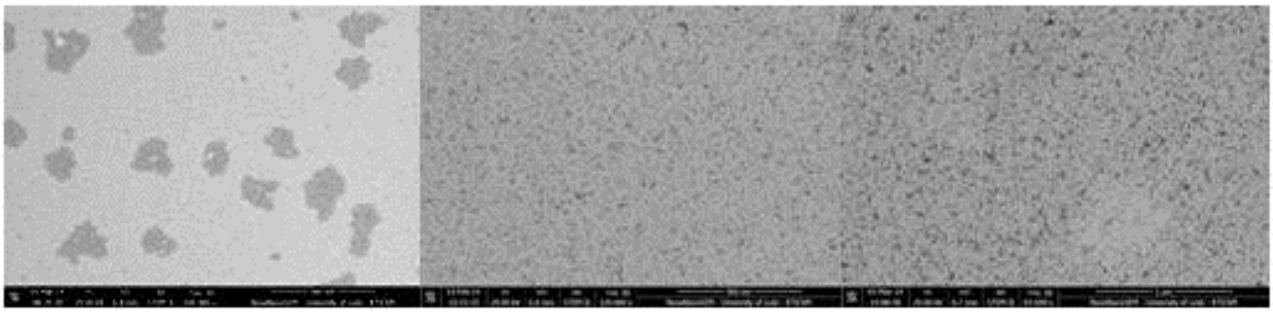


Figure 21. STEM images of the Au NPs in PS (left), PAH (middle) and PMMA (right) matrix. The scale bar of each micrograph is 1000 nm.

To enhance the film formation properties of the organic layer (coffee stain effect) as well as to increase the window of operation for the preparation temperature additional solvent blends of organic high and low boiling point materials were investigated. It turns out that the main problem of all investigated systems is based on the formation and collapse of bubbles at typical top electrode annealing temperatures.

All inkjet-printed memory devices

Due to significantly altered preparation conditions during the inkjet printing process, structural investigations were performed using AFM and profilometer measurements to reveal the interaction mainly between the top electrode (line width, electrode height) and the subjacent organic layer. In a first step, the evaporated bottom electrode was replaced by an Ag electrode printed from a NP-based Ag ink followed by a thermal sintering step to establish its conductive properties. The subsequent layers were spin-coated and evaporated, respectively. Compared to the reference devices, the I-V curve (Figure 22b) shows a clear deviation of I_{OFF}, which is assigned to the increased number of parasitic defect pathways in the HRS state caused by the higher surface roughness of the inkjet-printed bottom electrode. Consequently the I_{ON}/I_{OFF} -ratio is reduced to 6.5 10^4. The third device (Figure 22c) had a reversed built-up, i.e., an evaporated bottom electrode and a printed top electrode. Here, a further decrease in the ON/OFF ratio was found (2 10^3), which is ascribed to the solvent load during the printing of Ag ink onto the PMMA layer accompanied by a partial dissolution of the organic layer and interdiffusion of metallic particles. Further it is suggested that the postprocessing of the Ag electrodes leads to increased defect formation in the film due to interdiffusion of the metal. The fourth device combines the printing of the top and the bottom electrode, consequently also combining both I_{ON}/I_{OFF} ratio reducing effects and resulting in the lowest value of 2.8 10^2 (Figure 22d). A micrograph of such a device can be found in Figure 22e. A high-resolution TEM cross-section from the device with both electrodes printed is displayed in Figure 22f, clearly showing the granular morphology of the sintered Ag ink. It is evident that the poor I_{ON}/I_{OFF} ratio is mostly governed by localized defects in the organic film. A significant increase of the layer thickness can therefore also increase the I_{ON}/I_{OFF} ratio by decreasing the OFF-current. Therefore, in order to achieve a satisfactory ratio from the final all inkjet-printed device, a rather high PMMA layer thickness of about 500 nm was chosen and printed using a single nozzle print head. The whole fabrication process was carried out at ambient atmosphere.

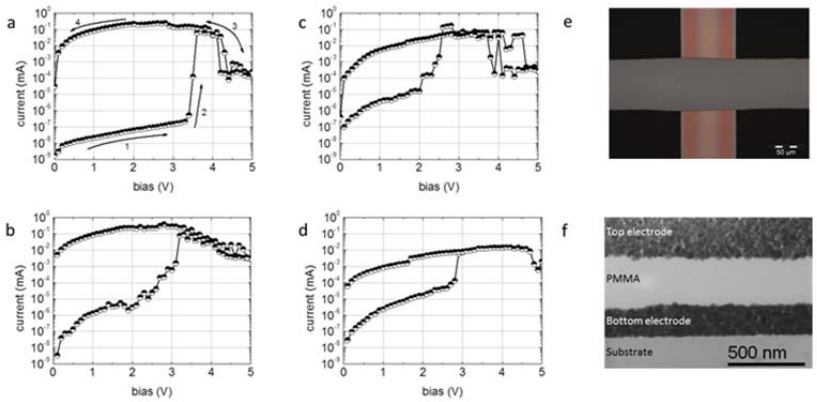


Figure 22. I-V characteristics of organic resistive switching devices with different inkjet-printed components. For all devices the organic layer was spin-coated with the same parameters. a) I-V curve of a standard fabrication device.

The bottom and the top electrode were evaporated, leading to an I_{ON}/I_{OFF} ratio of $3 \cdot 10^6$ (at 1 V). b) Only the bottom electrode is inkjet-printed - I_{ON}/I_{OFF} of $6.5 \cdot 10^4$ (at 1 V). c) Only the top electrode is inkjet-printed - I_{ON}/I_{OFF} of $2\ 10^3$ (at 1 V). d) Bottom and top electrode inkjet-printed - I_{ON}/I_{OFF} of $2.8\ 10^2$ (at 1 V). e) inkjet-printed memory element: both electrode line widths are in the range of 70 µm; f) high-resolution TEM cross-section through a memory with both electrodes inkjet-printed.

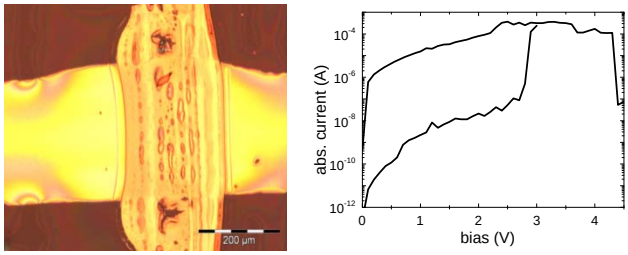


Figure 23. Left: Optical microscopy image of all-inkjet printed memory elements. Right: I-V characteristics of an all inkjet-printed memory device in a Ag ink / poly(styrene) ink / Ag ink structure.

Although all inkjet-printed devices were successfully prepared, the overall yield of working devices was significantly lower compared to spin-coated organic layer devices. Due to the low failure tolerance in array applications this is considered to be not sufficient. Therefore, for the devices presented in the following, the organic layer was spin-coated, while the electrodes were printed. Since a structured application of PMMA is not strictly advantageous (no impact on the memory array performance and no cost related issue w.r.t to PMMA), this approach can be seen as more practical.

Fully functional 2 x 2 array

Therefore, Au/MoO3/pentacene/Ca/Al diodes were chosen for the implementation into printed crossbar array structures. In detail, a 1R-1D cross point element consists of an Ag/PMMA/Ag memory element with inkjet-printed bottom and top electrodes and a rectifying element based on a device as shown in Figure 24.

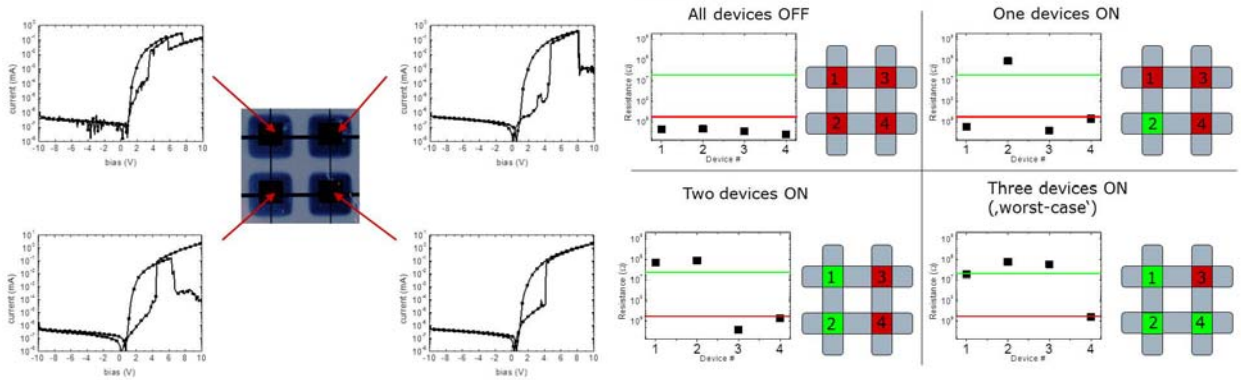


Figure 24. Left: I-V characteristics of four Ag/PMMA/Ag resistive elements with Au/MoO_3/pentacene/Ca/Al diodes in a 2 x 2 array configuration. Right: Permutation test of the information pattern in a 2 x 2 1D-1R array structure.

As the I-V characteristics reveal, each 1D-1R element shows a bi-stability in the forward direction and device state-independent characteristics in reverse direction. Additionally, Figure 24 (right) clearly indicates that independent of the actual information pattern stored in the array, a read out of each element is possible. Even the worst case scenario, one element in the HRS surrounded by 3 in LRS allows the determination of the device current of the element in the HRS. In this specific array/device configuration the ratio between the logic states was found to be 100.

32 x 32 array structure

Figure **25** shows an inkjet-printed flexible 32 x 32 (1024 bit) non-volatile memory array on polyimide (middle) as well transparent polyethylene terephthalate (PET) substrates (for photodetector applications).

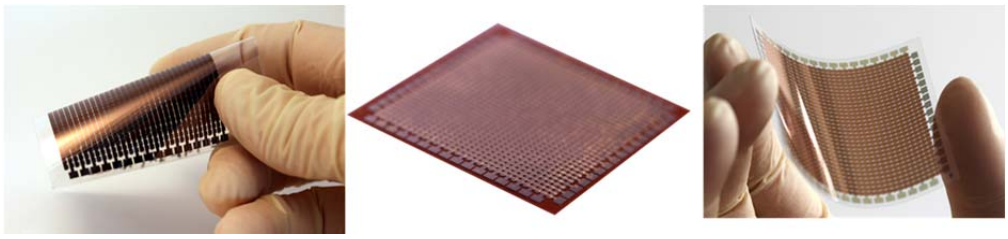


Figure 25. Flexible inkjet-printed 32 x 32 non-volatile memory array.

The Ag bottom electrode was printed with 600 dpi onto a previously cleaned Kapton HN500 foil, followed by a thermal annealing step at 150°C for 60 min. In order to achieve the required top electrode resolution (line width) the PMMA surface was exposed to an oxygen plasma for 6 s. This process step significantly improves the achieved feature size (deviation in the range between ±40 µm after annealing at 125°C for 180 min).
In Figure 26 (left), the I-V characteristics of different single elements are shown after establishing the bi-stable I-V characteristic. The device shows the typical threshold voltage at around 2.5 V and an ON/OFF ratio in the range of 10^3-10^4.

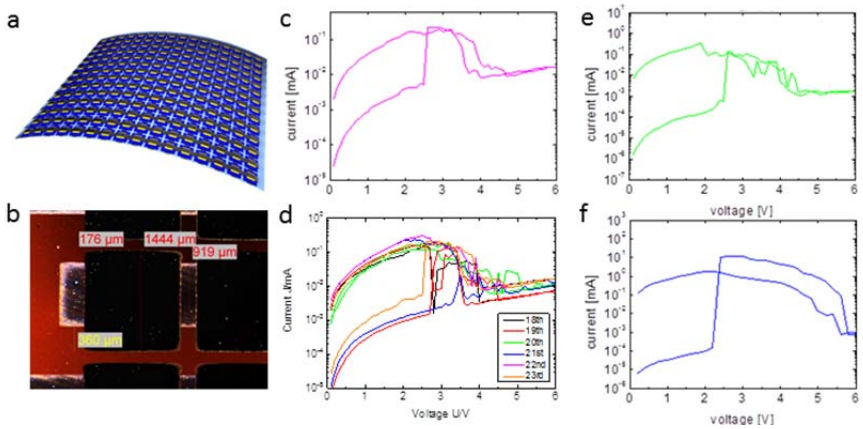


Figure 26. a) Schematic of flexible array demonstrator. b) Optical microscopy image of an inkjet-printed single element from 32 x 32 array; I-V characteristics of single elements, arbitrarily chosen from the array (numbers represent coordinates) c) 10,12, d) 5;4, e) 14,8, f) 20,20 inkjet-printed Ag/PMMA/Ag elements in the 32 x 32 array configuration.

Alternative preparation methods:

Apart from inkjet printing and physical vapor deposition alternative memory production techniques have been investigated. Special emphasis was laid on lamination based techniques with primarily focus on temperature assisted as well as metal transfer printing.
Thermal assisted device lamination was used for two polyimide substrates, each containing electrode structures coated with a PMMA film. For the lamination step the PMMA covered bottom half and the top half of the device were heated from room temperature to lamination temperature. Simultaneously the laminator, consisting of two solid metal blocks that are pressed together by means of disc springs was brought to temperature. For the lamination step the bottom half was placed in the lamination device, then the top half was properly aligned and placed on the bottom half. Finally, the lamination device is closed and pressure was adjusted by the springs. The lamination device was held closed for 10-15 minutes and subsequently brought down to room temperature. Although Ag/PMMA/Ag devices could be successfully fabricated via a thermal lamination the I-V characteristics showed well known features, i.e., a threshold voltage of about 3 V and an ON/OFF ratio < 10^3 at 1.5 V the yield of working devices was low and switching operation was not reliable calling for further optimization of lamination procedure.
To overcome some of the stability issues encountered by lamination (namely the high occurrence of short-circuited devices due to high pressure during the fabrication) we explored metal transfer printing (MTP). In this fabrication method the top electrode (TE) is not applied by means of high pressure but rather van-der-

Waals interaction under conformal contact of a soft stamp. The MTP ORS showed improved switching reliability and I-V characteristics (in terms of ON/OFF ratio >10^4 at 1.5 V). Multiple subsequent cycles are shown in
Figure **27**.

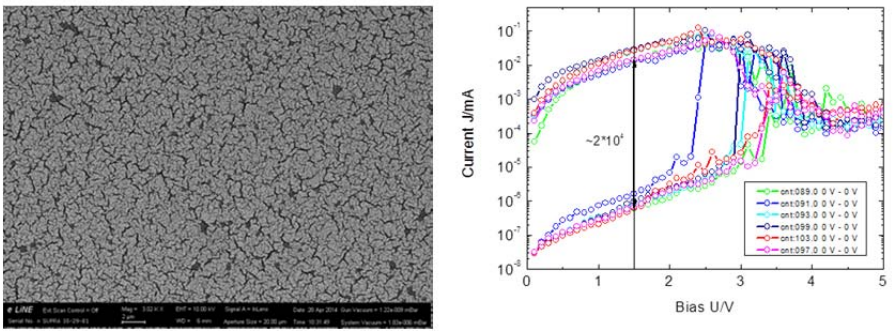


Figure 27. (left) Gold layer after stamping onto PMMA. The surface is covered with micro-cracks, but shows good conductivity. (right) I-V characteristics (multiple sweeps) of MTP ORS. Threshold is between 2.5 and 3 V with an NDR region between 3.5 and 5 V.

In summary, devices build up via MTP showed, compared to thermal assisted laminated devices, enhanced stability as well as a higher yield of working devices.

Miniaturization of memory devices and memory device applications

To test for the final limits of resistive memory devices an e-beam lithography unit was used to produce different structures of surface cell devices with and without additional organic layer on top (evaporated Alq3). As shown in
Figure **28** (left) such structures consist of two planar electrodes separated by a gap in the range of several tens of nm. Additionally, structures like nanowires and nanotips were implemented acting as seeds for a possible filament (
Figure **28** left insert a, b). Electrical characterization of such structures point out that after a forming step the same bi-stable I-V characteristic could be established as in the case of the macroscopic sandwich structures.
Figure **28** (middle) shows a nanowire device with an Alq3 layer on top after the formation of the electrical bi-stability. As it turned out during control experiments with an air gap, organic materials are not strictly required to establish a bi-stable I-V characteristic.

Figure **28** (right) shows a comparison between the I-V characteristics of a surface cell (red line) device and a macroscopic ITO/PMMA/Au device. Since there is no significant difference in the ON current of the two structures, these measurements clearly point out that the ultimate miniaturization is not limited by the size of the memory device itself but by the electrical performance of the diode. In order to switch the resistive device from its LRS to the HRS independent of the memory device size the diode has to provide a certain current which scales with the active area of the diode, thus limiting the overall minimal size of a 1D-1R device stack.

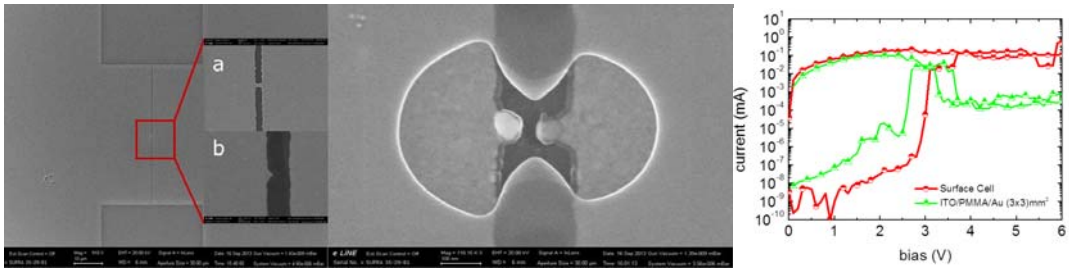


Figure 28. Left: Nanogap device (inset a: nanowire structure, inset b: nanotip structure). Middle: Scanning electron microscope image of an Alq3-covered nanowire device after establishing bi-stable switching in its HRS. Right: I-V characteristic of a surface cell device (red) and an ITO/PMMA/Au device.

Glancing angle deposition (GLAD)an alternative method for miniaturization of memory devices

Glancing angle deposition (GLAD) is a technique, which allows the tailoring of nanostructured morphologies through physical vapor deposition via controlling the substrate orientation with respect to the vapor source direction. When thin films are deposited onto stationary substrates under condition of *oblique deposition*, meaning that the vapor flux is non-perpendicular ($0° < \alpha < 90°$) to the substrate surface, an inclined columnar nanostructure is produced. The process is due to the ballistic shadowing of the morphology surface and amplified by the Volmer-Weber mode growth. The arrival of vapor flux and formation of film nucleation points is a random process. The nuclei grow into columns, and develop shadows. As a result, some nuclei will screen neighboring nuclei from incoming vapor flux, suppressing their growth. Given sufficient time, smaller columns can become completely shadowed and stop growing. This process, referred to as *column extinction* continues throughout the growth of a GLAD film. As the columns grow, more incoming vapor flux will deposit on them. Eventually, only the top parts of the nuclei are able to grow, developing into columns tilted towards the vapor source. The *column tilt angle* is defined by the angle between the surface normal and the columns direction, and is usually described by $\beta = \alpha - \arcsin\left(\frac{1-\cos\alpha}{2}\right)$ $\beta = \alpha - \arcsin\left(\frac{1-\cos\alpha}{2}\right)$. The substrate orientation is defined by two angles, namely the above-mentioned *deposition angle* α and the *substrate rotation angle* φ, which defines the azimuthal substrate position relative to an arbitrary starting position. By continuously rotating the sample (at a constant angle α) during the film deposition, vertically oriented columns can be obtained ($\beta = 0°$).
Figure 29 shows the comparison between Alq_3 thermally evaporated on coated ITO/glass substrate (cleaned by sequential sonication in acetone and isopropyl alcohol) deposited at normal incidence ($\alpha = 0°$) and applying the GLAD technique (at $\alpha = 80°$).

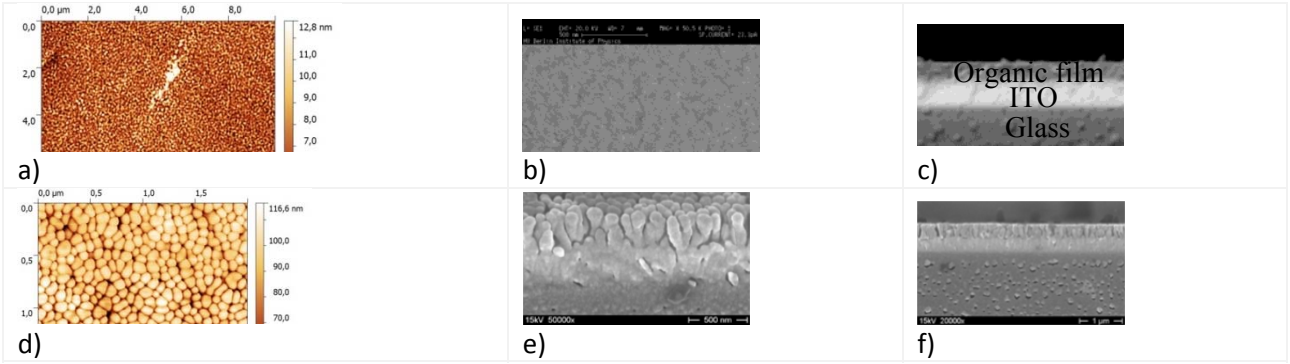


Figure 29. Planar (θ = 0°, a-c) and GLAD Alq3 (θ = 80°, d-f) films grown on ITO/glass. The images are recorded with AFM (a and d) and SEM (b, c, e and f), respectively.

The Alq_3 nanocolumns formed on ITO/glass exhibit an average radius of 50 nm with a large standard deviation (15%) from the mean value. The random nature of the nucleation process due to the ballistic shadowing leads to an irregular distribution in columns size and in their location on the surface. In order to avoid the randomness of the nucleation process and to control the size of the columns, the substrate can be covered with a regular pattern of nucleation points who will act as main mask for the formation of the nanocolumns. Employing a seed layer, the column uniformity is improved.
Figure 30 shows Alq_3 nanocolumns growth with GLAD techniques on an ITO/glass substrate, which was patterned with Au seeds having a lateral distance of 250 nm.

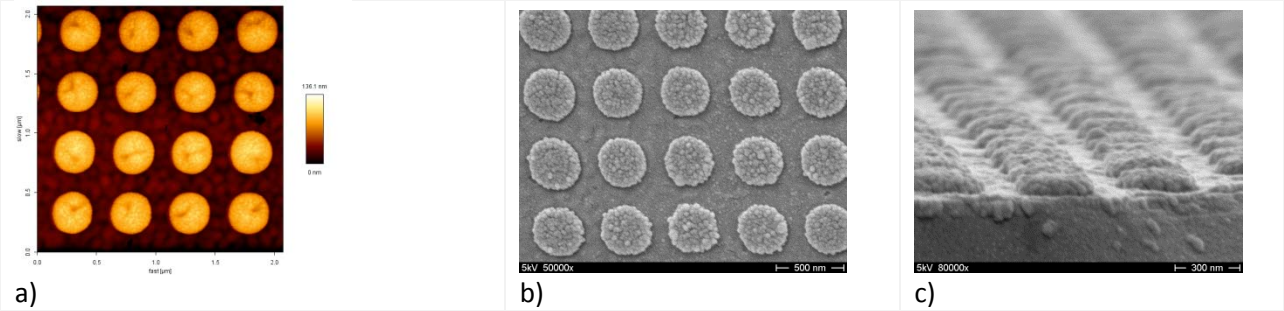


Figure 30. Alq3 nanocolumns grown on a Au patterned ITO/glass substrate: (a) AFM image, (b) SEM top-view image, (c) SEM cross-sectional image.

Glancing angle deposition techniques allows to downscale the device NV-MEs fabrication for proof of principle to the nanoscale.

Conclusion:

Apart from alternative preparation techniques, the main focus of WP4 lay on the integration of resistive memory elements into array structures. In accordance with the main objectives of WP2 (mainly dealing with the light-induced device state manipulation) and the tasks of WP5 and WP6 device setups, test stands and routines were successfully developed. Depending on the specific application (light-induced switching) or specific preparation method (inkjet printing) optimized setups were developed for each case and implemented into array structures. Due to significantly altered preparation conditions it turned out that the best performance could be achieved by a 1D-1R stack for the light sensitive element as well as 1R-1D stack for the inkjet-printed array structures. While in the former case an ITO/P3HT:PCBM/Ca/Al diode was used (see also WP6 - Demonstration) for inkjet-printed structures evaporated pentacene was chosen. Apart from evaporation and inkjet printing alternative lamination based techniques were evaluated and working resistive devices were demonstrated. Miniaturized elements in the nanometer range were realized in a surface cell structure via e-beam lithography and fully characterized.

List of deliverables and date of submission:

D4.1 Characterized basic NV-MEs array structures (planned for **month 20**, submitted in **month 20**)
D4.2 Characterized miniaturized NV-MEs array structures (planned for **month 24**, submitted in **month 24**)
D4.3 Characterized inkjet printed NV-MEs array structures (planned for **month 30**, submitted in **month 30**)

List of milestones and date achieved:

M8: Functional inkjet printed 2x2 array (planned for **month 24**, achieved in **month 24**)
M9: Functional miniaturized 2x2 array (planned for **month 24**, achieved in **month 24**)
M10: Functional inkjet printed 32x32 array (planned for **month 30**, achieved in **month 30**)
M11: Non-volatile storage capability of a 100 x 100 nm2 memory element (planned for **month 30**, achieved in **month 30**)
M12: Laminated 2x2 memory array with electrode widths in the range of 150 nm (planned for **month 36**, achieved in **month 36**)

4.1.3.5 **Work Package 5:** Integration with optical function and sensors (WP5)

The main goal of WP5 was the integration of the non-volatile memory elements (NV-MEs) developed in the previous WPs with optical functions, required for a direct addressing of each single memory element, and with different kinds of electrical sensors. Once assessed the best performing and reproducible NV-MEs architectures, which were developed in the first part of the Project, in particular in WP2 and WP4, these device structures were taken as a starting point for the development of the specific activities of WP5.

In particular, the activities carried out during the project were divided into two main tasks:

Task 5.1 Integration of light sources in NV-ME arrays and optical addressing in single memory elements.
Task 5.2 Integration of memory elements with electrical sensor devices.

Task 5.1 Integration of light sources in NV-ME arrays and optical addressing in single memory elements

Since within the first year of the project the investigations on single MEs revealed that the memory function of the majority of hybrid elements is based on filamentary nature, a direct manipulation of the resistance state by light cannot be achieved. However, as foreseen in the project proposal the implementation of single memory elements into a device network requires an additional rectifying device in series with the memory (i.e., a diode). By shifting the optical functionality from the memory resistor to the diode the whole proposed functionality could be achieved without limitations of the overall system performance (Figure 31).

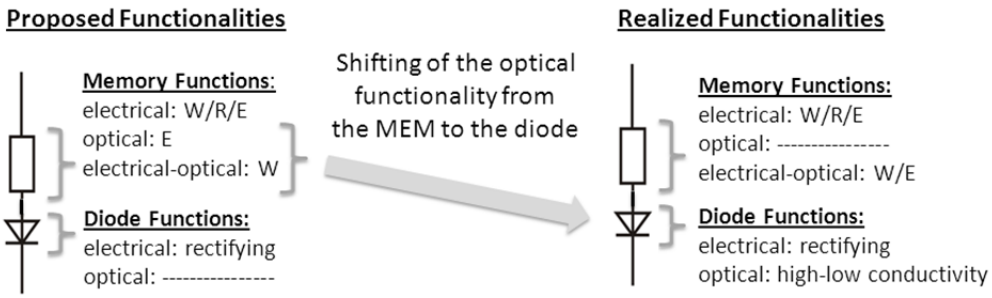


Figure 31. Proposed (left) and realized (right) functions of a 1D-1R element.

The new approach shifts the light sensitivity from the memory element to the rectifying element (diode) enabling full write AND erases functionality. Figure 32 shows the I-V characteristic of an already realized ITO/PEDOT:PSS/P3HT/PCBM/Ca/Al light sensitive diode.

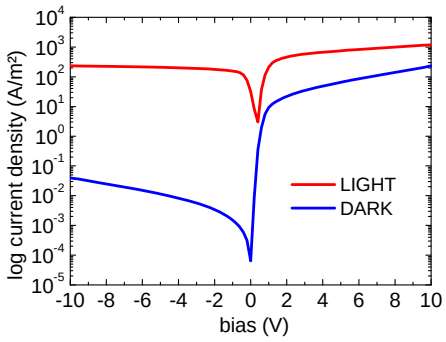


Figure 32. I-V characteristics of the PCBM:P3HT photodiode with illumination (i.e., light) and dark condition.

Therefore, task 5.1 focused on the integration of NV-MEs with a photosensitive layer/photodiode. Based on this rectifying device in series with an Alq3-consisting memory element all claimed functionalities were realized.

Electro-Optical Write Function: The device starts form the HRS (red line in Figure 33). Biasing the device at its threshold voltage (3 V) in dark condition does not change its resistance state (green line in Figure 33). Biasing the device at 3 V with additional illumination of the photosensitive diode leads to a switching of device to the LRS (blue line in Figure 33).

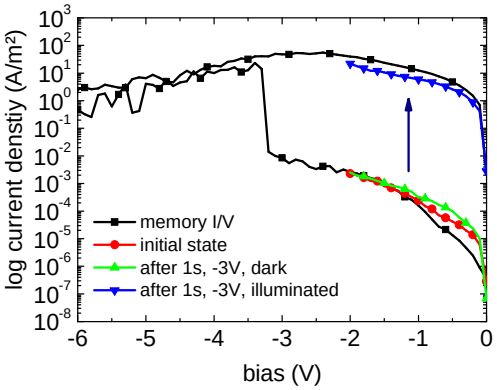


Figure 33. I-V characteristics of an optical induced device switching from the high resistance (HRS) to the low resistance state (LRS).

Electro-Optical Erase Function: The device initially in its LRS (red line in Figure 34) changes its state from ON to OFF while biasing at 10 V with additional illumination of the photosensitive element (blue line in Figure 34). Biasing the device at 10 V in dark condition does not change its resistance state (green line in Figure 34).

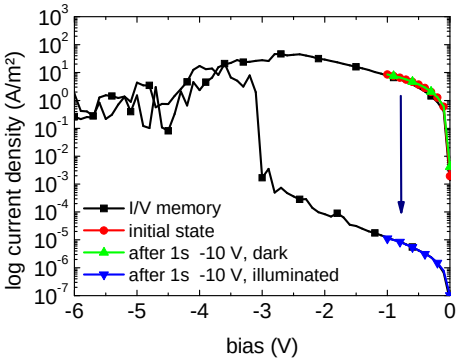


Figure 34. I-V characteristics of an optical induced device switching from the low resistance (LRS) to the high resistance state (HRS).

Using this approach it was possible to achieve ***Milestone 14 "Optical addressable single NV-MEs".***

Starting from the results as mentioned above, the same approach was employed for the development of a novel X-ray detector. In this case, the series of NV-ME and photodiode was integrated with scintillator material. Among different choices, a commercially available X-ray intensifying screen, which is typically used in medical X-ray diagnostics, was used, according to the following scheme (intensifying screen G 400 obtained from Primax Berlin GmbH).

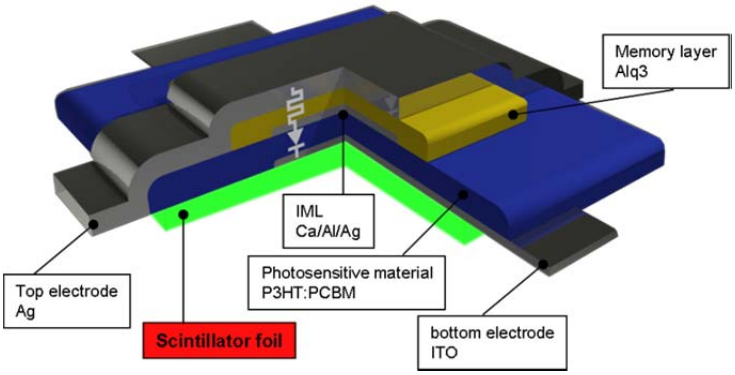


Figure 35. Schematic representation of the novel X-ray detector, which could be developed on the basis of the results of this project.

At first, the system is initialized by applying the RESET voltage (+ 6 V). Then the stack is set to the detection - bias of - 4 V (well above the specific threshold voltage). The resistive switch changes its resistance state in dependence of the light exposure. Afterwards, the written information can be read by measuring the resistance of the system (at 1.5 V) under dark conditions. The procedure is finished by resetting the system and making it ready for a new exposure (+ 6 V).
Figure 32 demonstrates a full cycle including a 'dark' reference measurement (noise level detection) at the beginning. As it is obvious, the device does not change its resistance state without illumination (and thus without X-rays). After switching on the X-ray source, the device changes its resistance from 7 * 108 Ω to 1.6 * 106 Ω (equals a factor of ~ 450). This cycle was repeated several times on different devices.

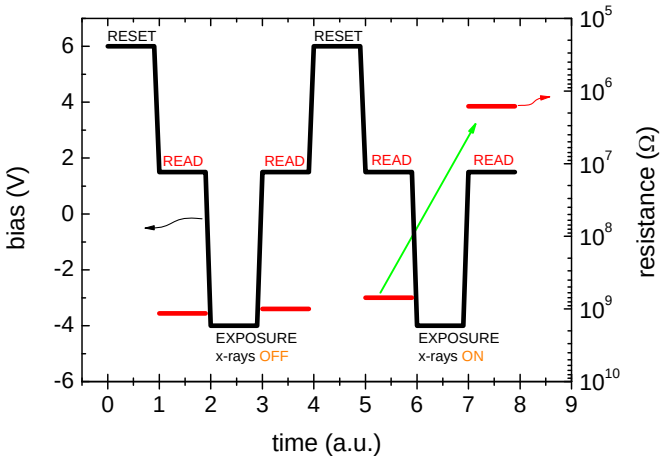


Figure 36. Detection capability of 8 kV X-rays. In the first part, the device was set to its exposure mode (- 4 V) while the X-ray source was switched off. As expected, no significant change of the resistance state was found. In the second part, the X-ray source was switched on and a change of the resistance state of the resistive switching element was detected afterwards (factor of ~ 450).

In this way, it was possible to achieve the ***Milestone 13 "Hybrid X-Ray Detector".***

Task 5.2 Integration of memory elements with electrical sensor devices

The aim of the activities developed within the task 5.2 concerns the integration of NV-MEs with different kinds of electrical sensors and the characterization of the electrical behavior of the developed integrated system. As demonstrated in the WP2 and WP4, the memory elements developed in this project are characterized by a bi-stable electrical behavior, which, in other words, means that it is possible to change the electrical conductivity (resistance) of a resistive element by applying a certain external voltage (program voltage). Moreover, this change in the conductivity remains constant even when the device is no longer biased

and can be restored to its previous value by applying a different external voltage (erasing voltage). Due to the ease of fabrication, the external stimulus for triggering the ME can be taken from the output of different kinds of sensing systems, according to the scheme reported in Figure 37.

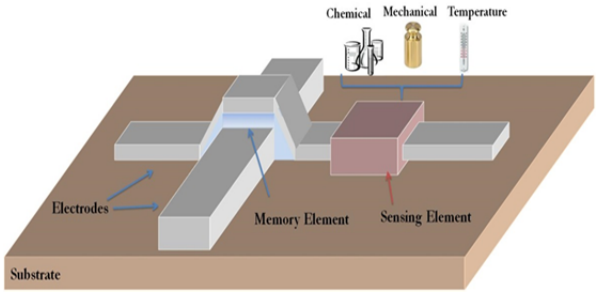


Figure 37. Schematic representation of a sensing system coupled with a non-volatile memory element (NV-ME).

It was demonstrated for the first time that by connecting a resistive memory element with a resistive sensing devices (thermo-resistor, chemo-resistor or piezo-resistor) in series, it is possible to trigger the memory element state, according to the scheme reported in Figure 38.

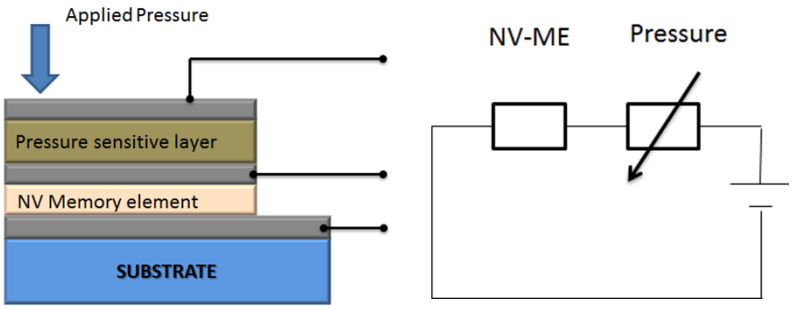


Figure 38. Schematic representation of the integration of one NV-ME with one pressure sensor.

The pressure sensor was realized using a piezoresistive rubber, called ZOFLEX®. In Figure 38Figure 38, the typical response of a piezoresistive rubber film to an applied pressure of 10 kPa is shown. In this case the pressure sensor is connected in series with a NV-ME produced according to the following procedure (developed in WP2). The MEs were fabricated on a glass substrate with patterned ITO electrodes. Afterwards, a first layer of an organic semiconductor, namely N1400, was deposited by thermal evaporation. A layer of gold NPs was subsequently deposited by electro-spraying, a second layer (of the same thickness) of N1400 was deposited at the top of the following structure, and finally a top electrode was deposited in order to obtain the final device in a crossbar configuration, as depicted in Figure 39. As can be observed from the plots reported in Figure 40 the NV-MEs can be written at a V_{prog}= + 4 V and can be erased at V_{erase}= -4 V

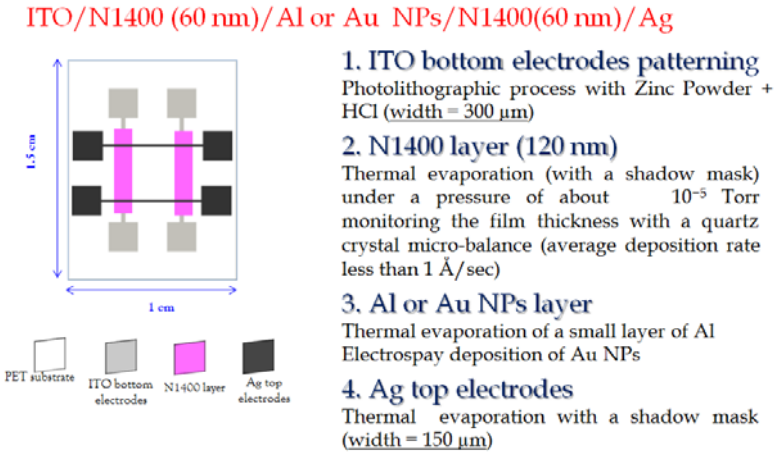


Figure 39. Schematic representation of the fabricated NV-MEs.

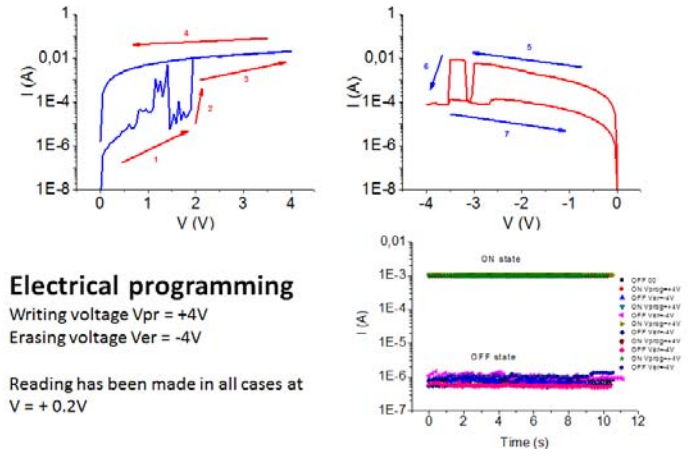


Figure 40. I-V characteristics of the NV-MEs showing how the electrical state can be switched between a high conductive and a low conductive state just by applying different external voltages.

Afterwards, the NV-MEs were connected in series with the previously mentioned pressure sensitive rubber. As can be noticed from Figure 41 (left) the resistivity can be changed by more than 5 orders of magnitude when pressure is applied. Using this configuration, if V_{prog}= + 4 V is applied to the series of the devices, no changes in the electrical state of the memory can be obtained, according to the fact that the entire voltage drops on the high resistive rubber element. When V_{prog}= + 4 V is applied and pressure is exerted on the rubber element, its resistivity drops down by orders of magnitude, as a consequence, in this case all the voltage is applied directly on the memory element that can be written (see Figure 41, right). A similar procedure can be applied for erasing the memory element.

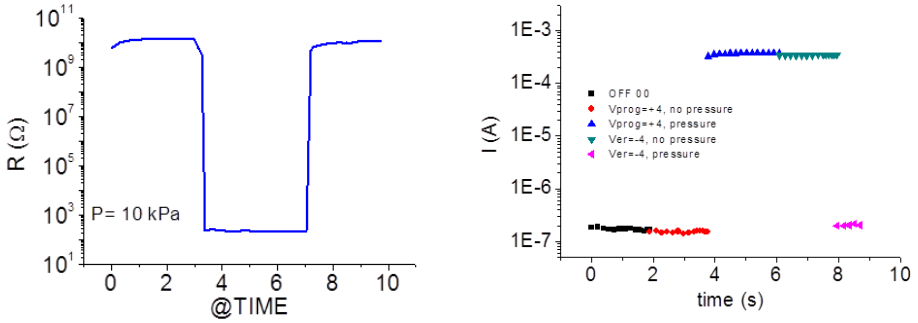


Figure 41. Resistance change in a typical piezoresistive rubber film, when an external pressure of 10 kPa is applied (left). Pressure induced resistance switching in the NV-ME/pressure sensors system (right).

Starting from these results, we designed a layout for the fabrication of a 2 x 2 array of NV-MEs integrated with a pressure sensor. In this case all the NV-MEs were fabricated on flexible plastic substrates with patterned ITO electrodes. The fabrication process is the same than that of the previous experiments with the only difference that in this case we employed Al NPs deposited by thermal evaporation. Concerning the integration with the pressure sensor, among several possible layouts, we decided to employ the configuration reported in Figure 42. In this case a layer of piezoresistive rubber is laminated over a selected region, overlapping the top electrodes of the NV-MEs array. Finally, a thin metallic layer was deposited on the top of the piezoresistive rubber (top electrode).
In Figure 42 we show how it is possible to program each ME just by exerting pressure on a certain area of the device. Initially, all the MEs are in the high resistance state (HRS), and a small current flows in all the devices. A constant voltage (V_{prog}) is then applied between the top electrode and the four bottom electrodes which are all grounded. When pressure is applied on the area highlighted in red in Figure 42 (right), a voltage drop will be induced only in those specific areas, thus allowing the writing of the two memory elements according to the procedure reported in the previous section.

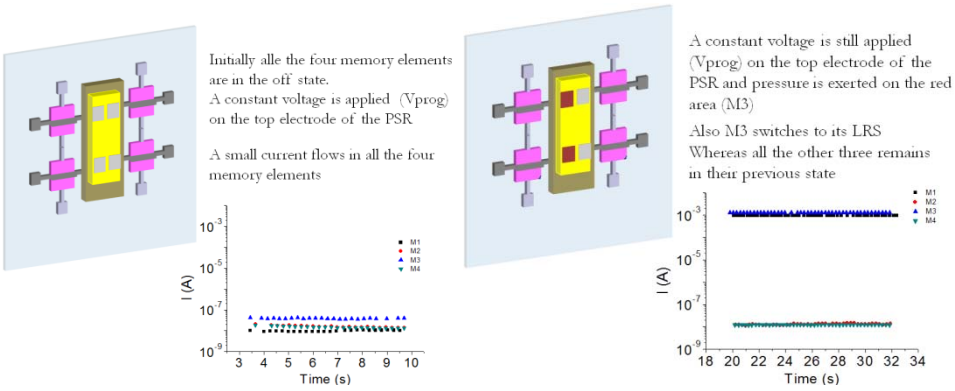


Figure 42. Schematic representation of the 2 x 2 array and electrical behavior of all the four MEs before (left) and after (right) pressure induced switching.

As can be noticed from the plots reported in Figure 42 the developed approach allowed obtaining a first example of a well performing and reproducible pressure addressable NV-ME array, allowing us to fulfill the milestone M15: NV-ME sensor system with an electrical sensor for one target parameter.

List of deliverables and date of submission:

D5.1 Fabrication guidelines for a hybrid X-ray detector (planned for **month 24**, submitted in **month 24**)
D5.2 Design of NV-ME-sensor systems (planned for **month 24**, submitted in **month 24**)
D5.3 Characterized memory elements integrated with electrical sensors (planned for **month 30**, submitted in **month 30**)

List of milestones and date achieved:

M13: Hybrid X-ray detector (planned for **month 24**, achieved in **month 30 as agreed with EC after the contingency plan approval**)
M14: Optical addressable single NV-MEs (planned for **month 32**, achieved in **month 32**)
M15: NV-ME-sensor system with an electrical sensor for one target parameter (planned for **month 36**, achieved in **month 36**)

4.1.3.6 Work Package 6: Demonstration (WP6)

With the changes in specifications that came up during the project, the scope of the demonstration WP shifted as well. It turned out that the developed technology can not only be applied as an optically erasable (and writeable) resistive memory, but also as a full scale optical detector array. The actual shift thereby does not concern the functionality of the device (which is superior to the previously targeted), but only the fabrication process. The new device is not inkjet-printed, but fabricated by an evaporation process. All other technical targets specified for the demonstrator in this deliverable meet or even come out better than specified. As it was shown, inkjet printing based techniques can in principle be used for the preparation of single elements as well as array structures. However, to allow for a full functional array, a rectifying diode needs to be included in the stack giving a 1 Resistor – 1 Diode device. Moreover, it was demonstrated that the fully functionality of the memory array can only be achieved with an evaporated pentacene diode with according well-matched electrodes. An according printing process for the needed low-work-function electrodes was not available at that time in the consortium and there was no good example of such a process which could have been adapted given the remaining resources in the HYMEC project. However, memory arrays with P3HT:PCBM photodiodes are well functioning, actually showing technical functionalities, which are far beyond the expected specifications. In addition to an *"an optical erasing function" we can also "program the array with light and store information in the detector-memory pixel including grey scaling (4-bit).*
This feature makes the optically addressable array a technical viable demonstrator, which will also be of interest for end-users such as Siemens or Thin Films. The most important issues in this relation are the technical capability of the device. It was therefore meaningful to concentrate on the development of the technical specifications using evaporation-based techniques instead of inkjet printing techniques.

Implementation of a Demonstrator

With the combined achievements from all WPs (especially WP4 and WP5) a demonstrator was fabricated. Details on this novel device are given in the following. As illustrated in
Figure 43, a single pixel of the presented image detector concept comprises a vertical stack of an OPD and an ORS. As OPD, a well-known system based on a photoactive layer consisting of a blend of regio-regular poly(3-hexylthiophen-2,5-diyl) (rr-P3HT) and phenyl-C61-butyric acid methyl ester (PCBM), forming an p-n bulk-heterojunction in between the two electrodes, was used. A typical I-V curve of the OPD at different illumination conditions is shown in Figure 44a.

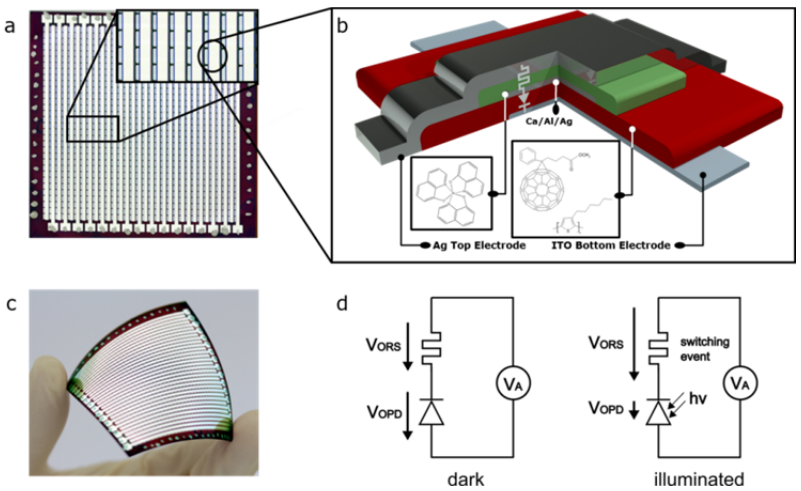


Figure 43. Photographs and illustration of the assembly and the image detection principle. a) Micrographs of the 32 x 32 pixel detector array. The ITO bottom electrodes (perpendicular oriented to the Ag top electrode lines) are not visible due to the opacity of the photoactive layer (dark red). b) Schematic cross-section through a single pixel and the materials used. c) Photograph of the image detector array on a flexible substrate. d) Detection principle of a single pixel: illumination of the OPD leads to a redistribution of the voltage drops across the two devices. This is used to trigger a threshold event which leads to a non-volatile resistance change in the ORS.

Single Detector Pixel. A stack of an OPD and an ORS represents a serial connection. When applying a voltage across the this stack, the setup can be considered as a voltage divider: According to Kirchhoff's laws, a fixed applied voltage ($V_{APPLIED}$), splits up into a voltage drop across the OPD (V_{OPD}) and across the ORS (V_{ORS}), depending on the resistance of the two individual building blocks ($V_{APPLIED} = V_{OPD} + V_{ORS} = R_{OPD} \cdot I + R_{ORS} \cdot I$). V_{OPD} decreases as the resistivity of the OPD decreases upon increasing irradiance, resulting in a corresponding increase of V_{ORS}. As illustrated by Figure 43d, this principle is used to trigger the threshold event in the ORS: As soon as V_{ORS} exceeds V_T, the resistive switching element changes its resistance state. This resistance state is preserved, even if illumination and the voltage is turned off and can be read-out at any time later. Thus the image information is stored in each pixel until a reset pulse (+ 7 V) is applied. Compared to CCD detectors, which exhibit a destructive read-out, unlimited access to the image information is possible.
Based on this principle of operation, a vertical stack consisting of an Alq3 - ORS on top of an rr-P3HT:PCBM - OPD, resulting in an ITO/rr-P3HT:PCBM/Ca/Al/Ag/Alq3/Ag assembly, was realized. The I-V curve of the vertically stacked combination of both devices is shown in Figure 44c and can be described as follows: Initially the ORS is in its HRS. The I-V – sweep was started at - 6 V and bias was decreased to 0 V, detecting only the reverse current of the diode. In forward direction (0 V – > 6 V – > 0 V), the photodiode is conductive and does not act as current-bottleneck for the ORS. The typical shaped I-V characteristics of a single ORS can be observed. When going back to - 6 V again, the low reverse current of the diode dominates, although the ORS element was switched to its LRS.

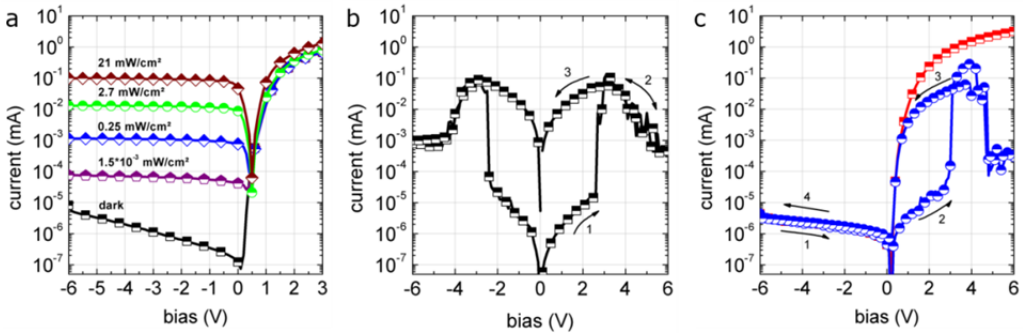


Figure 44. I-V characteristics of the OPD, the ORS and a stack consisting of both devices. a) I-V curve of the OPD under dark conditions (black line) and different illumination conditions. b) typical I-V curve of an Alq3 based ORS device. Device relevant figures of merit can be deduced from this curve: read-out region < 2 V, threshold voltage ~ 3 V, negative differential resistance 3 V - 5 V, delete voltage > 5 V. The measurement sequence is indicated by the arrows. c) I-V curve of a stack of an ORS on top of an OPD (blue) and I-V curve of the OPD solely under dark conditions (red). Under reverse bias conditions, the I-V curve is dominated by the reverse current of the OPD. In forward direction, the OPD does not limit the distinct characteristics of the ORS. The measurement sequence is indicated by the arrows.

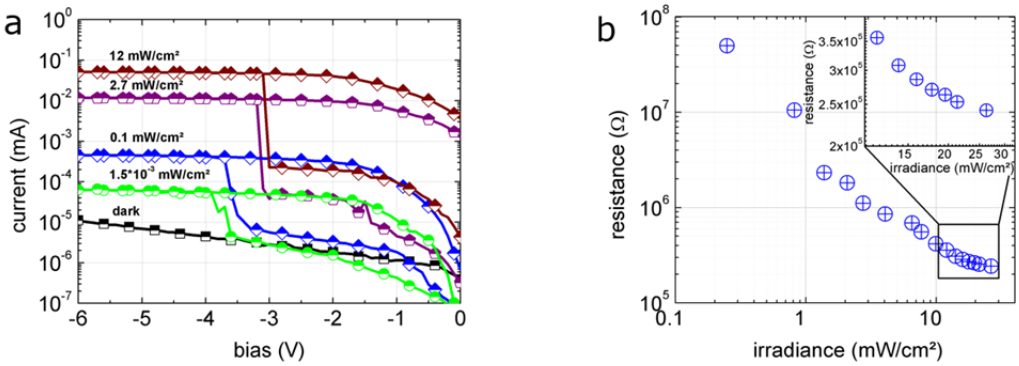


Figure 45. Grey scaling mechanism and capability of a single pixel of the memory array. a) I-V curve (reverse bias) of the OPD-ORS stack for various illumination conditions. In dark, the I-V curve is dominated by the low reverse current of the OPD and no threshold event can be observed (black curve). Under illumination, a threshold can be observed and the generated photocurrent in the OPD determines the resulting resistance of the ORS. By means of this principle, b) 16 different resistance states (4-bit) were written.

ORS typically have an ON/OFF ratio (LRS-to-HRS ratio) up to 10^7 and a high amount of intermediate resistance state in between these two extremes can be addressed. This gives the system a distinct grey scaling capability. An intermediate state can be written by applying a voltage pulse in the NDR region. The same effect can be obtained by adjusting a suitable current compliance value during the switching event which programmes this resistance into the memory element. Photoconductivity of the OPD at certain illumination conditions renders an 'intrinsic' current compliance for the ORS in the OPD-ORS stack allowing storing various greyscale values.

Figure 45**Error! Reference source not found.**a shows the I-V curve at reverse bias of the OPD-ORS stack under different illumination conditions. A voltage applied to the detector element leads to voltage drops across OPD and ORS depending on their specific resistance. Under reverse bias, the resistance of the OPD (dark) typically exceeds the resistance of the ORS in its HRS by a factor of more than 10 and therefore most of $V_{APPLIED}$ drops across the OPD. The remaining small voltage drop across the ORS is not sufficient to trigger a threshold event (**Error! Reference source not found.**a, black line). Under illumination, the photoconductivity of the OPD leads to a modification of its resistance resulting in a redistribution of V_{ORS} and V_{OPD}. If $V_{ORS} > V_T$, the ORS changes its resistance state determined by the photocurrent supplied by the OPD. Figure 45a demonstrates this principle for four different irradiance values where four corresponding resistance states between 60 MΩ and 100 kΩ are programmed into the ORS. 4-bit grey scaling was realized in this way**Error! Reference source not found.**.

One detection cycle of a single pixel can be summarized as follows: 1) the stack is set to a bias of - 5 V (well above V_T). 2) Depending on the light exposure, the ORS element changes its state. 3) The written information can be read by measuring the resistance of the system (at 1.5 V) under dark conditions. 4) The procedure is finished by resetting the system and preparing it for a new exposure (+ 7 V).

Array Integration. Irrespective of the specific application case, a passive 2-terminal crossbar array structure suffers from parasitic sneak current caused by adjacent non-addressed elements, bypassing the addressed one. To avoid this problem, an additional element with a particular non-linearity in its I-V characteristics has to be integrated in series to each node. For a passive array of ORS, this element can be a rectifying diode, matching with the absolute current levels of the ORS. As a distinct feature of the presented concept, the rr-P3HT:PCBM photodiode is not only used as a photosensitive element, but also fulfills the desired requirements (high forward current, low reverse current and low onset voltage) under dark conditions (**Figure 44**a). Thus it can also be used as non-linear rectifying device, enabling a proper read-out of the stored image information in the resistive switch. Figure 44c clearly indicates that the diode current does not limit the I-V curve of the ORS in forward direction, ensuring that the full ON/OFF ratio of the ORS is available to store image information. Under reverse bias, the low reverse current of the diode dominates the circuitry, guaranteeing a proper blocking of current contributions from neighboring elements. To verify for an appropriate sneak current handling in the detector array, the worst case scenario - being an element in its HRS surrounded by elements in their LRS - was imitated. Figure 46 demonstrates this issue for 2 x 2 cells of ORS without and with photodiode in comparison. Figure 46a shows the read-out contrast of an array of solely ORS (no OPD): devices 1-3 are in their LRS and device 4 is in its HRS. During read-out of device 4, however, a low resistance is apparently measured from the periphery caused by the low resistance of the three adjacent elements. Thus, no proper read-out is possible. The same pattern was written in a 1 photodiode – 1 resistor array (Figure 46b). Here, parasitic current is effectively blocked by the diode and the read-out of device 4 in its HRS is not significantly influenced by the other three elements.

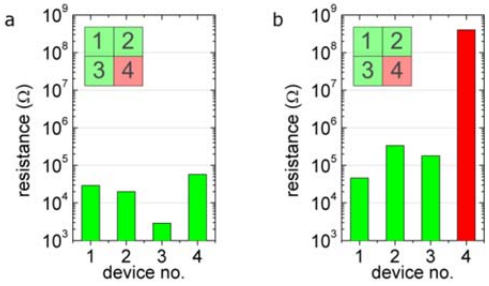


Figure 46. Demonstration of the necessity of a rectifying element in arrays of ORS. Devices 1 – 3 are in their LRS, device 4 is in its HRS a) Obtained resistance values of an array of ORS solely – a proper read-out is not possible, due to the bypassing of the addressed element via non-addressed adjacent elements in their LRS. b) Obtained resistance

values of an array implementing an ORS and the rectifying (photo) diode in each pixel. A proper read-out is thus possible.

Although a slight increase of sneak current (dark current) was observed during the characterization of the 32 x 32 pixel detector array, it was possible to show the full functionality of the cells. Due to fact that the thicknesses of both organic layers (rr-P3HT:PCBM and Alq3) are larger than 300 nm, the effect of thin-film defects was limited and the number of short devices was kept at an minimum.
A detection cycle in the array is basically equal to that of the single element: 1) all pixels are set to a constant bias of - 5 V simultaneously (by connecting all word and bit lines, respectively); 2) only illuminated pixels change their resistance state; 3) the detected pattern is read by sequentially measuring the resistance of each cell (+ 1.5 V); 4) a reset bias of + 7 V, again simultaneously applied to each cell, makes the system again ready for the next frame. Figure 47 shows four different illumination patterns, sequentially written into 3 x 3 cells by using the described routine. It can clearly be observed that only the illuminated devices change their resistance state by orders of magnitude.

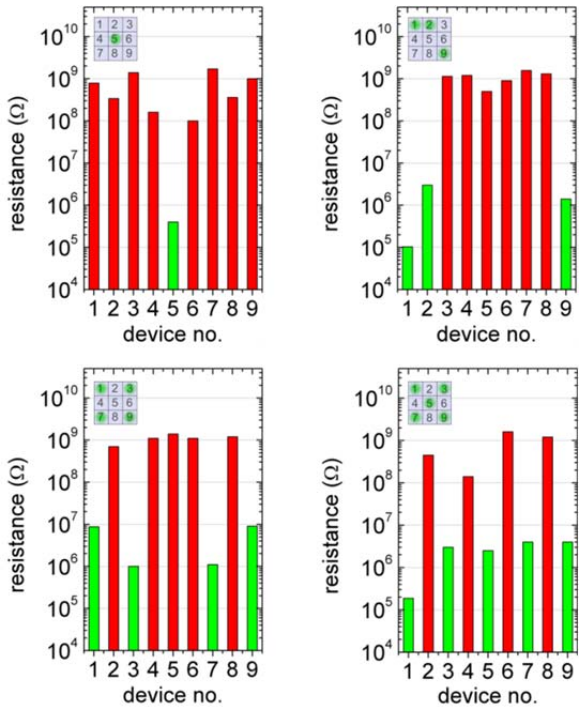


Figure 47. Patterns written in a 3 x 3 pixel detector according to the presented detection scheme. A voltage of - 5 V was applied to all elements, simultaneously during light exposure. For illumination, green emitting LEDs were directly placed below the selected elements (see inset). The written patterns were properly stored in the detector array.

For the demonstration activities a test stand for the characterization of this 32 x 32 pixel detector array was fabricated using a drop on demand 3D printer (OBJET 30 Pro). Vero White (Objet) was used as ink. The wiring was done using basic electronic components. In the final design each bottom and top contact was simultaneously contacted. Each wire is then connected to a switching system, which was used to connect individual bottom and top electrodes with the source-measure unit (Figure 48).

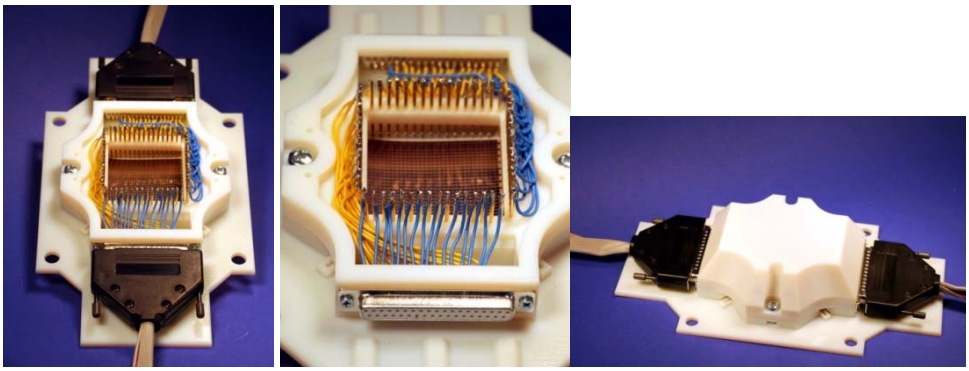


Figure 48. Photographs of the 3D-printed measurement stand for a 32 x 32 memory array with optical addressing and greyscaling capability.

Market Search

Although the exact market share of hybrid/organic NV-MEs and devices with expanded functionality cannot be precisely predicted for the next years, the increasing number of activities in this field clearly shows that this technology shifts more and more into the industrial focus. Very recently, ThinFilm Electronics (Norway) demonstrated the first integrated and printed system with a rewritable memory. The system is basically a printed electronic label, consisting of printed memory, sensor and logic that is able to detect whether a critical temperature threshold has been exceeded and records data digitally for later retrieval and display. Such labels can deliver item-level tracking of quality data for goods such as pharmaceuticals and perishable foods. Such an integrated system shows how low-cost, disposable printed electronic technology will provide information about product history based on data stored in Thinfilm Memory^{TM}. In this case, a NV-ME is directly interfaced with a temperature threshold sensor, when the temperature threshold is reached, the electronic system writes the element, and the data is retained for a long time for later inspection and can be used for transferring information to a display.

Companies like Siemens or Philips, on the other hand, are intensively working on organic X-ray detection systems. The main interests - from a medical point of view is for example the availability of this material class for new detector systems for different imaging modalities and applications - from a technical point of view for example curved detectors as required for computed tomography;- form an economical point of view a reduction of the production costs. Due to these fundamental medical, technical as well as economical requirements organic our application seems to be an ideal candidate, addressing all these requirements.
Our achievements clearly a show that the combination of a photodiode and a resistive switch can expand the functionality of memory devices which has not been shown before. We directly established contact to Anton Paar GmbH which declared their interest on the presented photo and X-ray detector.

Conclusion

Within this WP we demonstrated a unique organic light-addressable memory array technology. By vertically integrating an organic photodiode and an organic resistive switching element in one pixel, no additional building blocks such as transistors are needed for addressing the single nodes in an array. The 2-terminal wiring of two vertically stacked devices significantly reduces the footprint of a single pixel down to the theoretical limit of $4F^2$, allowing integration with a high fill-factor. The presented features of simultaneous detection and storage of the photonic/image information directly in one pixel is closely related to the properties of inorganic CCD technology, but unlike CCD this technology does not show a destructive read-out and does not exhibit any integrating behavior. With these essential features, the easy fabrication and simple wiring in combination with the advantages of organic electronics, the presented light-addressable array is a substantial step towards industry imposed specifications.

List of deliverables and date of submission:

D6.1 Market search and potential industrial contacts (planned for **month 22**, submitted in **month 22**)
D6.2 Requirements for devices/demonstrators from end-user (industry) point of view (planned for **month 24**, submitted in **month 24**)

D6.3 Assessment of production process and costs (planned for **month 30**, submitted in **month 30**)
D6.4 Characterized demonstrator (planned for **month 32**, submitted in **month 32**)
D6.5 Inkjet printed memory array on a flexible substrate including an optical erasing function (planned for **month 36**, submitted in **month 36**)

List of milestones and date achieved:

M16: Declaration of interest from industrial end users (planned for **month 22**, achieved in **month 22**)

4.1.4 Potential impact and the main dissemination activities and exploitation of results (not exceeding 10 pages).

The continued dimension and function scaling (in the end the realization of a system in an alternative technology such that it performs the identical function as the original system and offers improvements in at least one of size, power, speed, or cost) of CMOS is driving information processing technology (transmission, storage, manipulation and processing, and output of data) into a broadening spectrum of new applications.
Since dimension scaling of CMOS will eventually approach fundamental limits, several new alternative information processing devices and microarchitectures for existing or new functions are being explored to sustain the historical integrated circuit scaling cadence and reduction of cost/function into future decades.

This is accomplished by addressing two technology-defining domains:

- Extending the functionality of the CMOS platform via heterogeneous integration of new technologies
- Stimulating invention of a new information processing paradigm

The expansion of the CMOS platform by conventional dimensional and functional scaling is often called "More Moore". For example in 1954, the average selling price of a transistor was $5.52. Fifty years later in 2004, this had dropped to a billionth of a dollar decreasing further within one year to one nano-dollar per bit for dynamic random access memory (DRAM).
Alternative CMOS platforms can be further extended by the "More-than-Moore" approach. Functional diversification may be regarded as a complement of digital signal and data processing in a product. This includes the interaction with the outside world through an appropriate transduction (sensors and actuators) and the subsystem for powering the product. These functions may imply analog and mixed signal processing, the incorporation of passive components, high-voltage components, micro-mechanical devices, sensors and actuators, and micro-fluidic devices enabling biological functionalities.
As depicted in Figure 49, it is the heterogeneous integration of digital and non-digital functionalities into compact systems that will be the key driver for a wide variety of application fields, such as communication, automotive, environmental control, healthcare, security, and entertainment.

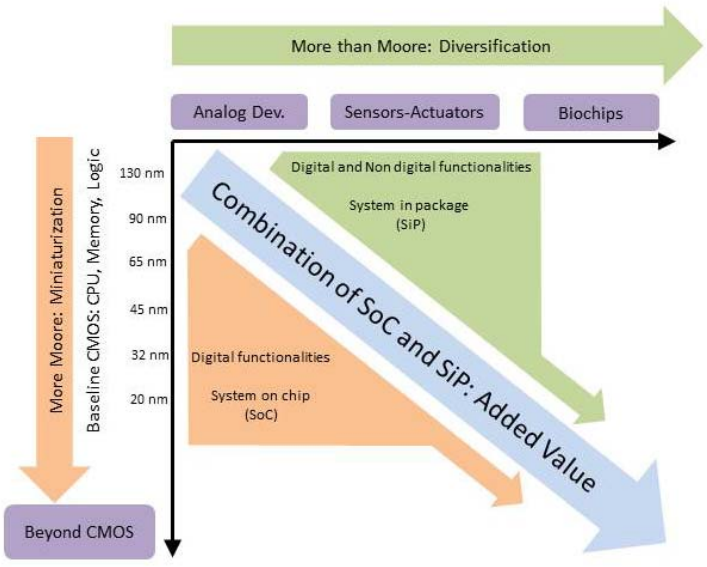


Figure 49 Combined digital and non-digital funtionalities in integrated systems (Taken and modified from the International Technology Roadmap for Semiconductors).

"More-than-Moore" based technologies have already made a considerable contribution to the world wide microelectronics market and the opportunities are still huge. Since it is expected that the relative weight of the "More-than-Moore" component in the industry evolution will increase over time, a new "virtuous cycle" must be established to relay the industry expansion, based not only on device scaling but on many innovations at the system, technology, device and circuit levels. Those innovations will have to address not just frontend technologies but backend/packaging technologies as well recognizing an increasing importance of the interaction between frontend and backend technologies for System on a Chip (SoC) and System in Package (SiP) systems.
Whereas "More Moore" may be viewed as the brain of an intelligent compact system, "More-than-Moore" refers to its capabilities to interact with the outside world and the users (Figure 50).

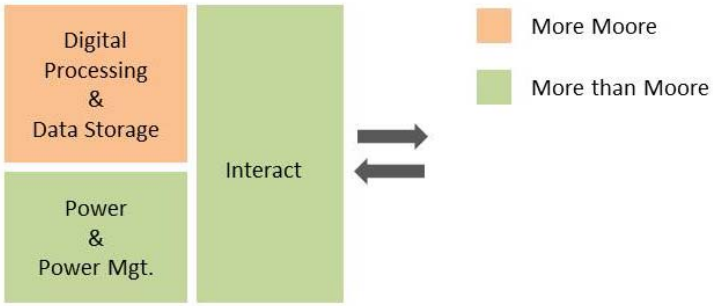


Figure 50 "More-than-Moore" devices complement the digital processing and storage elements of an integrated system in allowing the interaction with the outside world and in powering the systeme (Taken and modified from the International Technology Roadmap for Semiconductors).

The typical embodiment of these more complex products is realized as an assembly of various components (ICs, passive components, etc.) on a printed circuit board (PCB).
However, the present progress in both, process technology and design, is enhancing the compatibility of CMOS and non-digital technologies, which enables the migration of non-digital components from the PCB into the package containing the integrated circuit SiC, or even into the chip itself SoC.
Especially the latter technology could significantly improve the functionality of modern personal computer architectures since it allows the direct implementation of the cache memory on top of the central processing unit. Another example is represented by the imager chip in a digital camera, which combines "More Moore" (image signal processing) with "More-than-Moore" (image sensor, through silicon via) technologies including smart and/or (ultra-fast) pixel electronics, and exhibiting low power consumption and small footprint, suitable for integration within a portable device such as a mobile phone.

The flash memory market landscape is shifting rapidly, with increasingly sophisticated mobile handsets playing a leading role in driving industry trends and determining future memory technologies (IHS iSuppli Mobile & Embedded Market Tracker Report).
According to the "Flexible Display Report" from HSBC (April 2013) flexible, bendable and transparent mobile handsets will be one of the leading markets drivers in the future.[i]
Although flash memory has not reached its ultimate limits up to now companies like Samsung or HP have put significant efforts into new emerging memory technologies mainly based on resistive elements to face this new application requirements.
In general, resistive switches can be subdivided in three classes namely phase change RAMs (PCRAM), resistive RAMs (RRAM) and magnetic RAMs (MRAM).
So far MRAM and PCRAM are quite commercialized and have a reasonable market share whereas it still has to be seen when RRAM enters the market. Even though major global players are involved in the development of resistive memory devices the proposed market launch of RRAM technology by HP and Hynix in Q1 of 2013 has been shifted to the end of 2013 due to financial considerations since the new technology would have cannibalized the classic flash memory market in which Hynix is already heavily involved.[ii]

Due to invested capital in production facilities for already established memory technologies the extent of replacement of conventional MEM-devices by new technologies remains unclear for the next years as implicated in Figure 51.

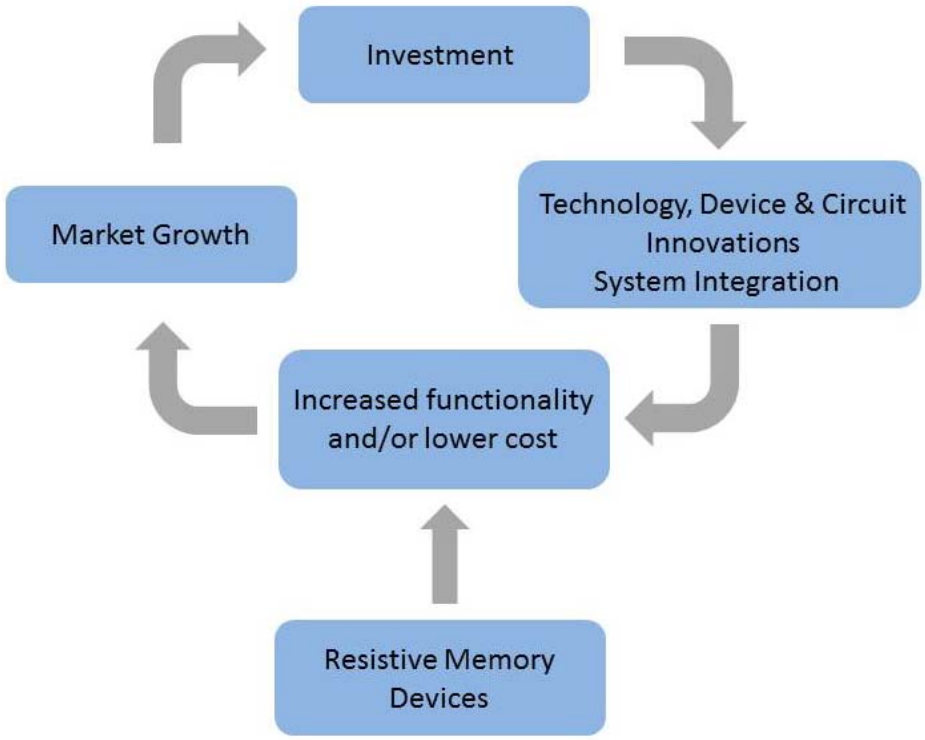


Figure 51 Possible impact of resistive memory devices on the virtuous cycle of digital microelectronic industry systeme (Taken and modified from the International Technology Roadmap for Semiconductors).

Novel non-volatile memory technologies like resistive NV-MEs will have a significant impact on future applications. It is believed that in a first step, these next generation non-volatile memory technologies are expected to replace NAND flash applications.
Although the individual technologies are not completely established up to now it is believed that this next class of NV-MEs can fulfil all requirements of a so called 'universal memory', which has the potential to replace established volatile (fast memory applications, e.g., DRAM) and non-volatile NV-MEs (storage applications, e.g., NAND flash based memory cards, hard disk drives, etc.) due to their unique properties.
Combining these unique storage properties with the predicted increase of flexible transparent mobile handheld applications organic and hybrid memory devices can probably fulfil the new device requirements.

Organic-based Resistive Devices

In contrast to inorganic resistive devices, which have already been reported in 1964 by Nielsen and co-workers[iii], only a decade ago organic-based resistive memory devices attracted a substantial amount of attention from scientists and engineers working in organic electronics due to their excellent memory performances and low production costs. Although metal-oxide-based resistive memory devices have several advantages, such as scalability, low power consumption, and fast switching speeds, their use with large-area flexible substrates is limited because of their intrinsic material properties and high-temperature fabrication process.
Printable organic and hybrid materials are amongst the most important emerging technologies for the mass production of large flexible electronics and have been used in two-terminal-based organic resistive memory devices, printed circuits boards, RFID tags, large-area sensors, flexible displays, and many other emerging electronic applications.[iv]

Due to their simple structure organic-based memory devices are ideal candidates for low-cost large-area production techniques; according to IdTechEX[v] a substantial market for printed logic/printed nano-particle conductive structures as summarized in Tab. 3.

Table 3. IdTechEx forecast for the printed logic market (2012-2022)

Logic Market 2012-2022 (IdTechEx)			
	Logic/memory US$ Bn	**Logic/memory % printed**	**Logic/memory %Flexible**
2012	0,002	75	80
2017	0,06	88	85
2022	3,5	90	90

Resistive switching phenomena have been correspondingly demonstrated for a variety of organic materials, and different switching mechanisms have been proposed based on experimental evidence and supposedly established theories.
Despite of considerable progress in the advancement of novel memory technologies within the last few years, there remain some challenging tasks to be resolved to reach the final goals in the technological development of organic-based hybrid memory devices.

All of these tasks are addressed by the HYMEC consortium

- Obtaining a detailed understanding of the fundamental science behind switching phenomena
- Identifying and systematizing critical fabrication parameters for the control and optimization of switching characteristics
- The adoption/development of fabrication techniques
- Expand of the resistive device functionality according to “More-than-Moore”

By resolving the scientific and technical issues described above, this memory technologies will facilitate the development of new flexible memory applications but will - from today's perspective - not completely replace conventional flash memory devices, for reasons of footprint area (minimum current needed to disrupt filaments).

Based on the progress in the project consortium as well as on the continuous market monitoring process of all involved partners the following competitor/potential partner was identified:

Thin Film Electronics ASA: The Norwegian company demonstrated organic-based NV-MEs with ferroelectric polymers[vi]. According to company information they are mainly targeting:

- NFC (near field communications) tags
- RFID (radio-frequency identification) tags
- Sensor labels
- Programmable and disposable price labels

Up to now a pre-commercial roll-to-roll 6×6 ferroelectric memory array demonstrator has been presented by Thin Film Electronics ASA.

[i] HSBC “Flexible Display Report” B. Sohn, R. Seo, J. Tsai” April 2013 *www.research.**hsbc**.com/R/20/Pm97sCt*
[ii] http://www.tomshardware.com/news/ReRAM-memristor-Kavli-Foundation-Stan-Williams-Hynix,17986.html
[iii] Nielsen et al. IEEE Tran. elect. Dev. 1964, 11 243
[iv] B. Cho et al. Adv. Funct. Mater. 2011,21, 2806
[v] www.idtechex.com stand July 2013
[vi] www.thinfilm.no stand July 2013

<u>Publications in peer-reviewed journals:</u> see 4.2 Section A1

<u>Contributions at national and international conferences:</u> see 4.2 Section A2

4.1.5 Project public website, contact details.

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Project logo: