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PROJECT FINAL REPORT

Publishable summary report: attached documents

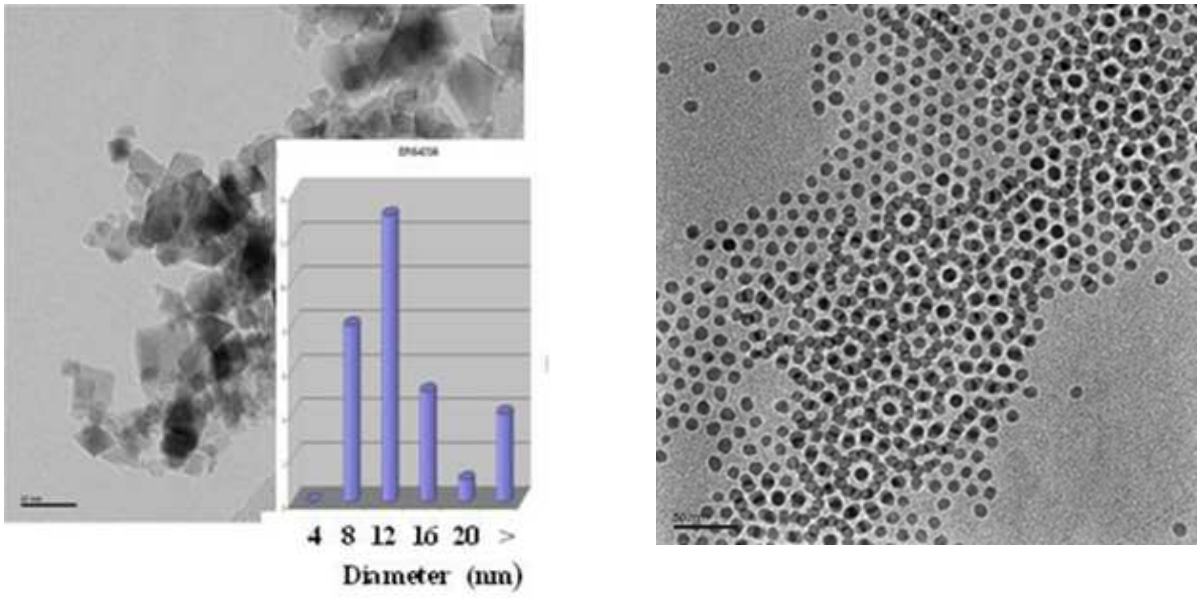


Figure 1: Nanoparticles obtained by Flame Spray Pyrolysis (left) and associated size distribution (inset left); Mono-dispersed nanoparticles obtained by wet routes (9nm mean size) for future incorporation in host matrix powders

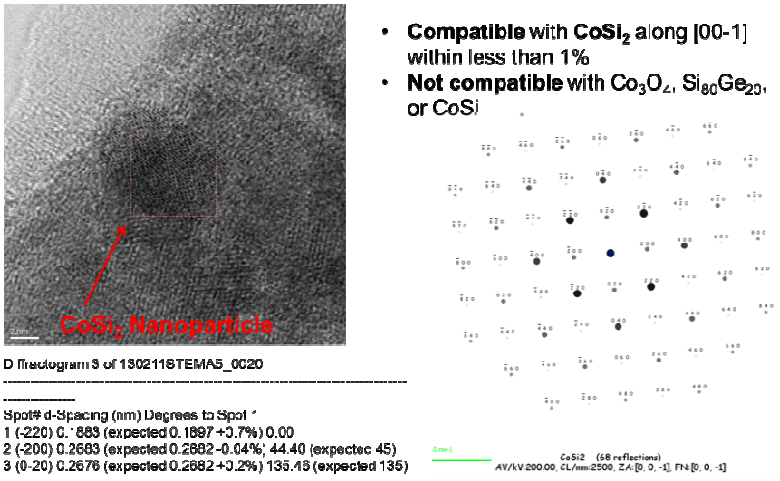


Figure 2: Showing $CoSi_2$ nanoparticles post-processed within the n-$Si_{80}Ge_{20}$ lattice identified by x-ray diffraction and EDX.

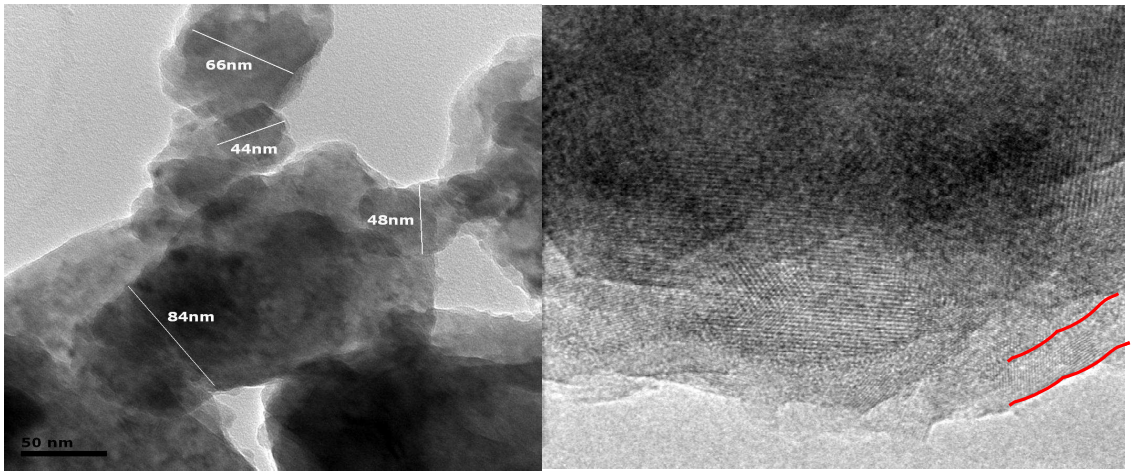


Figure 3 : As-milled SiGe matrix powders characteristics (Transmission Electronic Microscopy): a. typical particle size constituting elementary grains; b. Oxide layer at the grain surface;

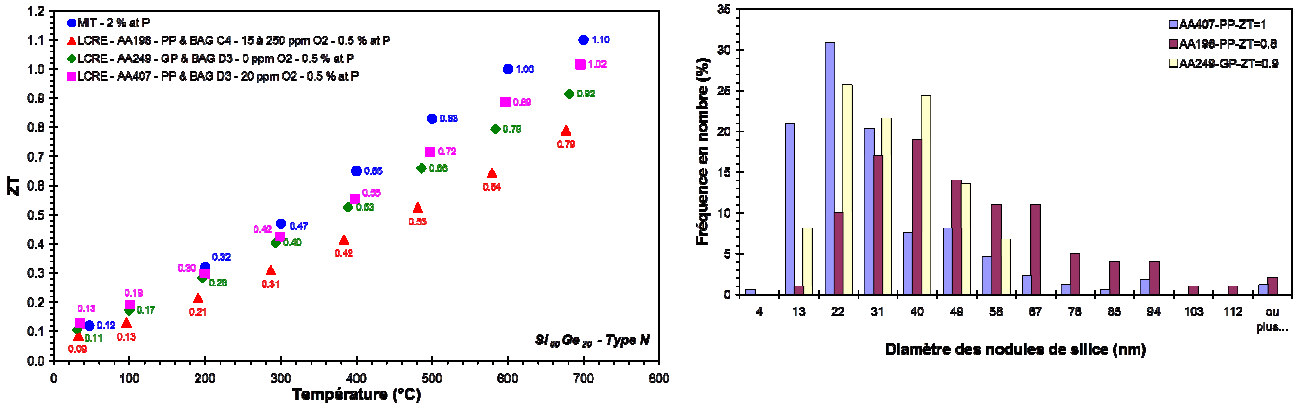


Figure 4: Comparison of ZT of $Si_{0.8}Ge_{0.2}$ host matrix alloy figure of merit as a function of the oxygen content in the synthesis and pre-sintering environment (left); Correlation with the diameter and number of silica nodules present in the microstructure (right)

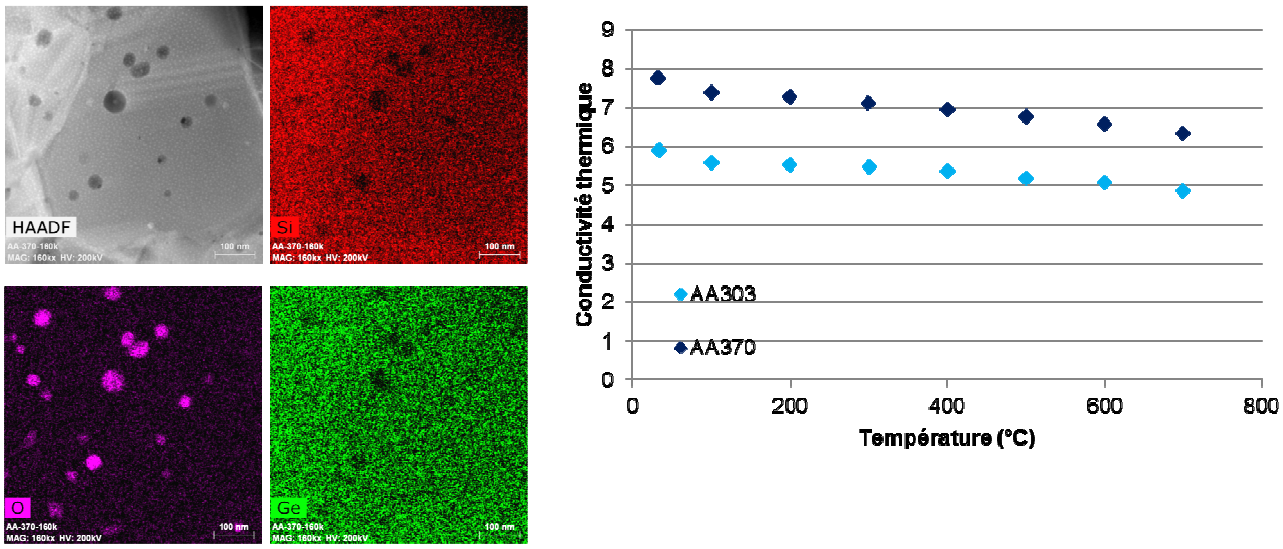


Figure 5 : HRTEM picture and chemical analysis of N-type $Si_{0.92}Ge_{0.08}$ host matrix, showing the existence of numerous nanoscale silica nodules in the microstructure (left) ; effect on thermal conductivity for the oxygen rich (clear blue) and poor (marine blue) samples (right).

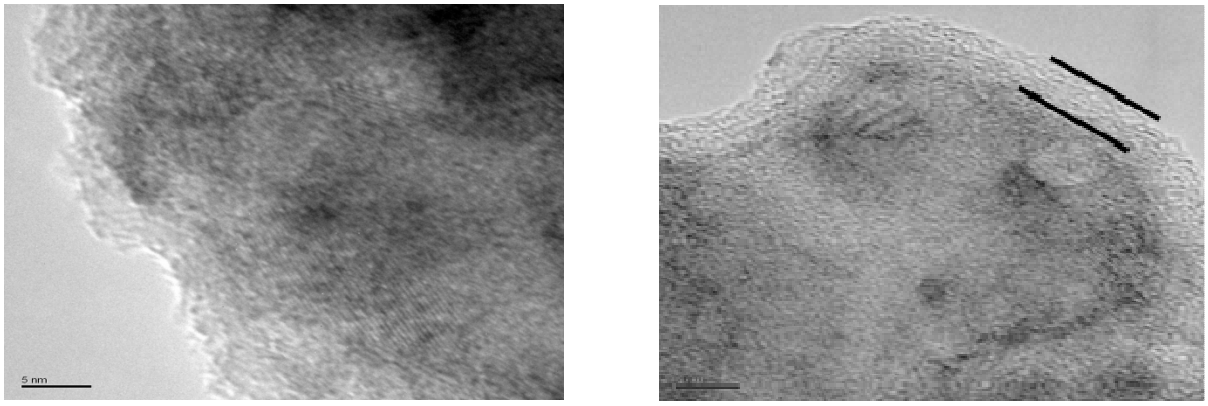


Figure 6: TEM picture of (left) Mg2Si0.4Sn0.6 before air-exposure and (right) Mg2S0.4iSn0.6 after air-exposure.

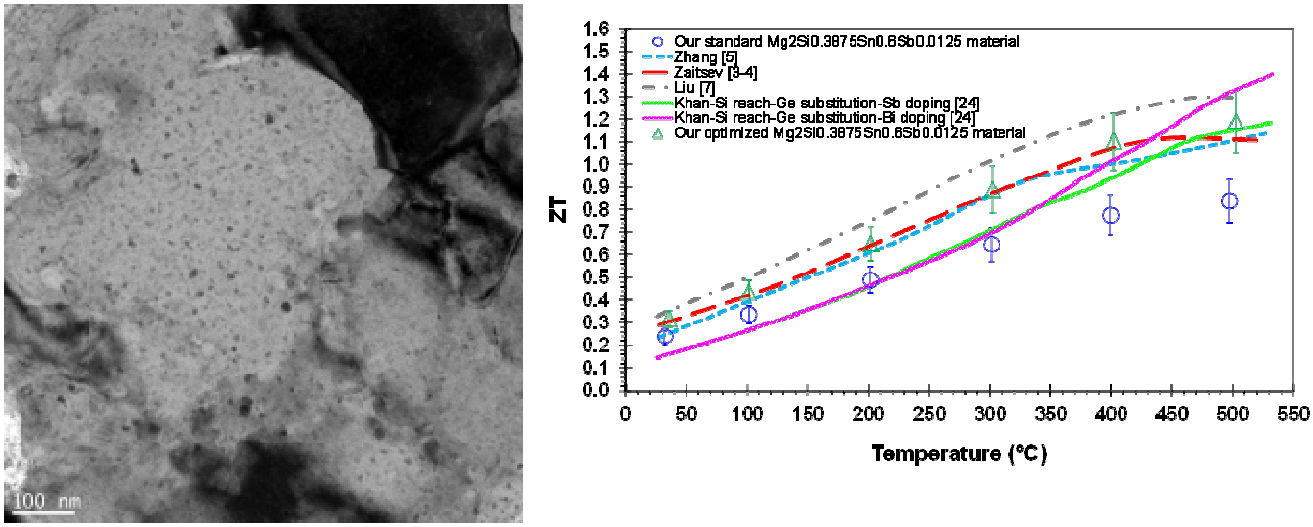


Figure 7 : (left) Detailed microstructure of n-$Mg_2Si_{0.375}Sn_{0.6}Sb_{0.125}$ obtained by mechanical alloying at high resolution ; (right) Figure of merit of the optimized phase (2d period) compared to the standard one (1st period) after optimization of SPS and comparison with reported values.

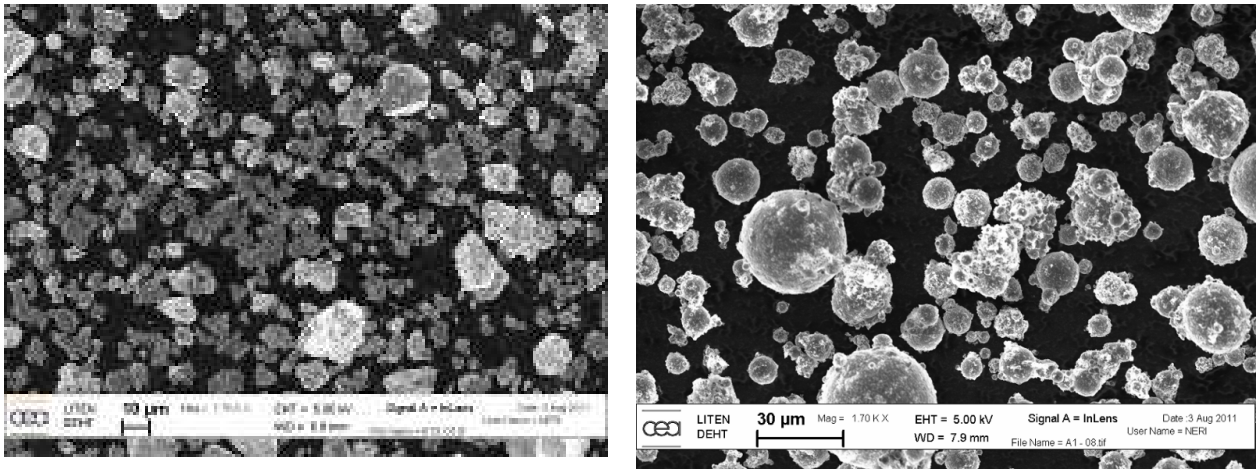


Figure 8 : Morphological differences of Mg2SiSn powders mechanically alloyed (left) and synthesized by a scale-up compatible technique (right)

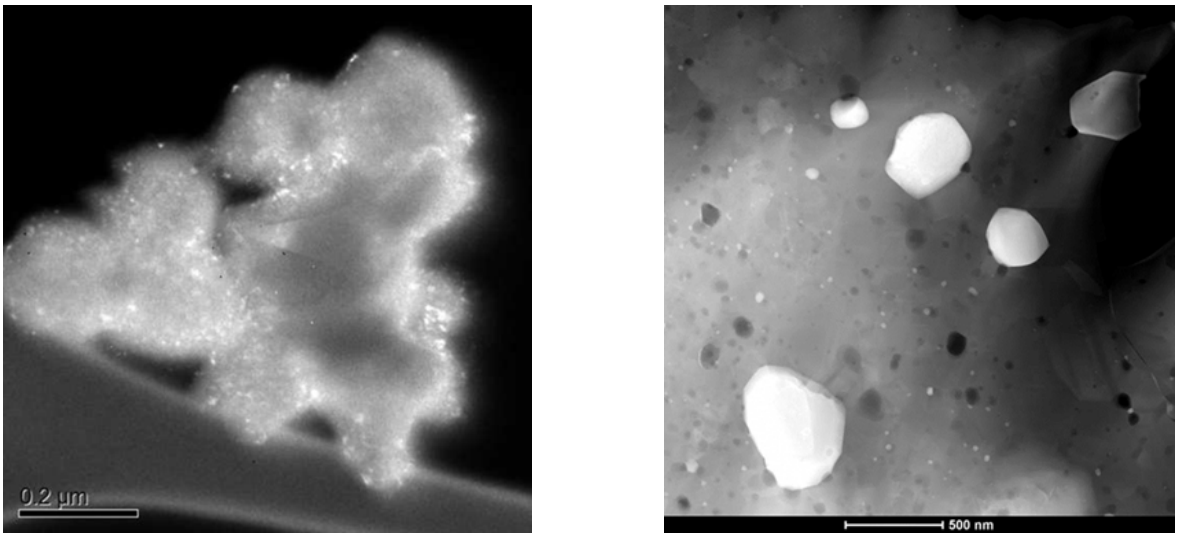


Figure 9 : TEM Off-axis Dark field Image of post reduced Co_3O_4:n-$Si_{80}Ge_{20}$ nanocomposite powders,(left); Dark field TEM picture of $MoSi_2$ nanoparticles embedded in a $Si_{0.92}Ge_{0.08}$ host matrix after sintering. Apart from a few very large agglomerates the inclusions population is dominated by 20-30nm range inclusions.

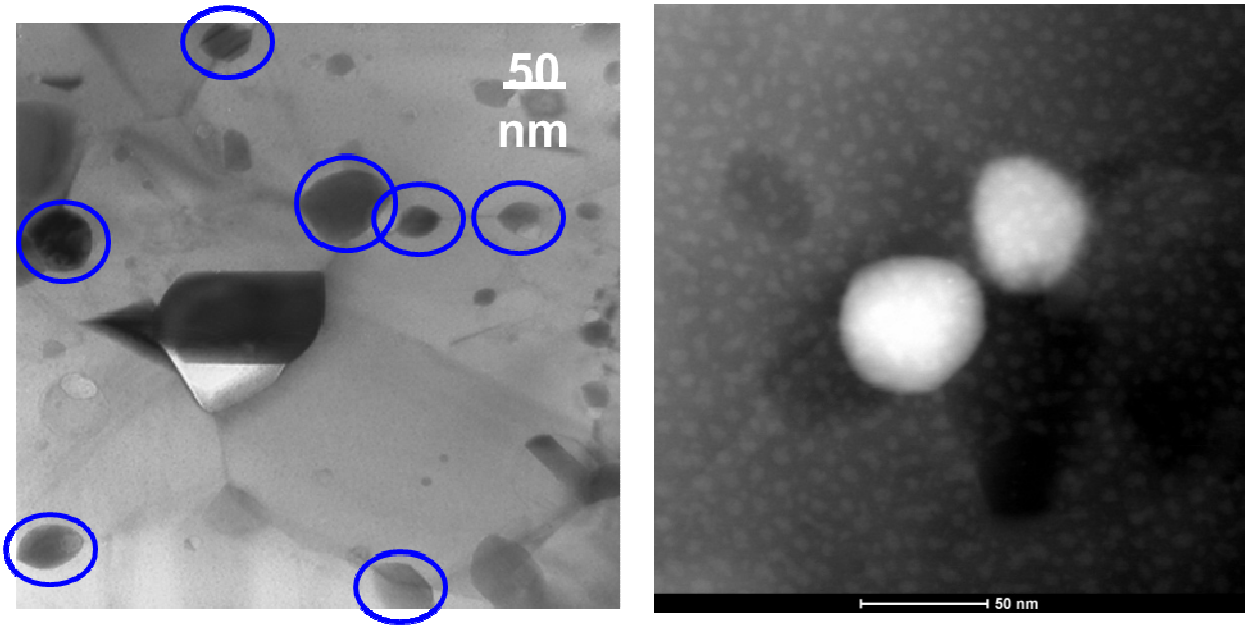


Figure 10: TEM Image of nanoparticles incorporated into host matrix, and located at triple points.

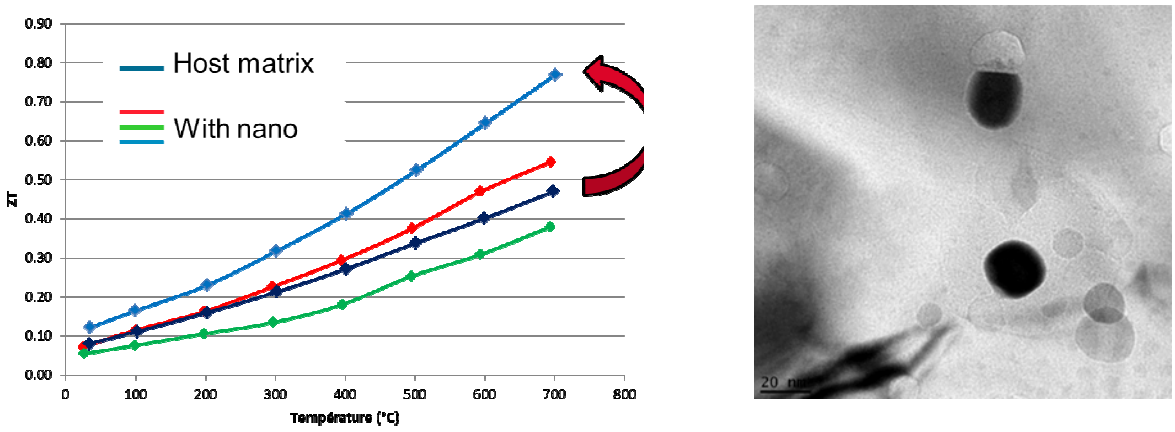


Figure 11 : Thermoelectric figure of merit (left) of 1.3% vol $MoSi_2$ P-$Si_{0.92}Ge_{0.08}$ nanocomposites sintered in varying conditions as a function of temperature; nanoinclusions HRTEM picture of inclusions in host matrix (right).

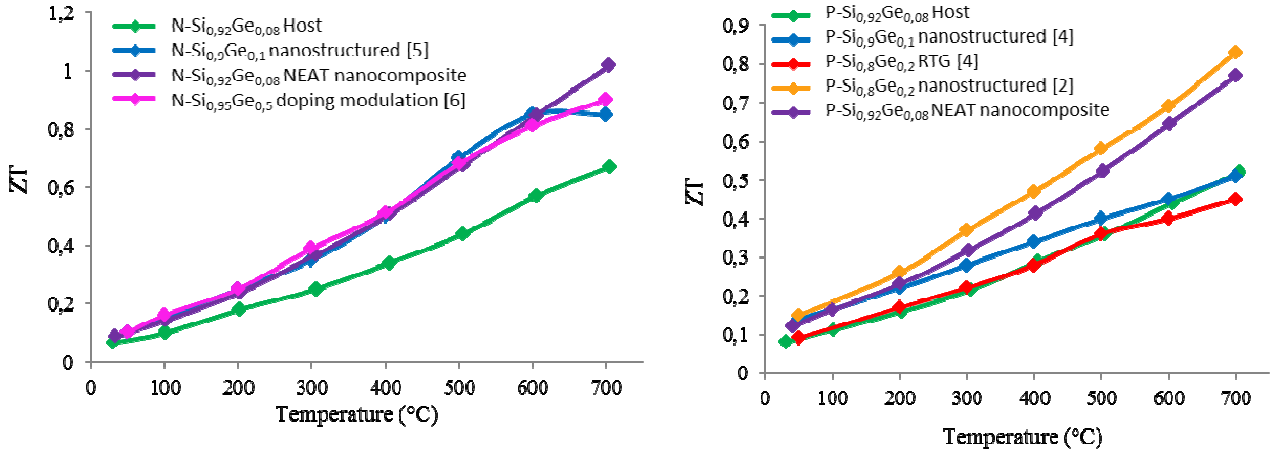


Figure 12 : Final comparison of the thermoelectric figure of merit of best NEAT $MoSi_2$-$Si_{0.92}Ge_{0.08}$ N (left) & P-type (right) nanocomposite with the state-of the-art SiGe alloys

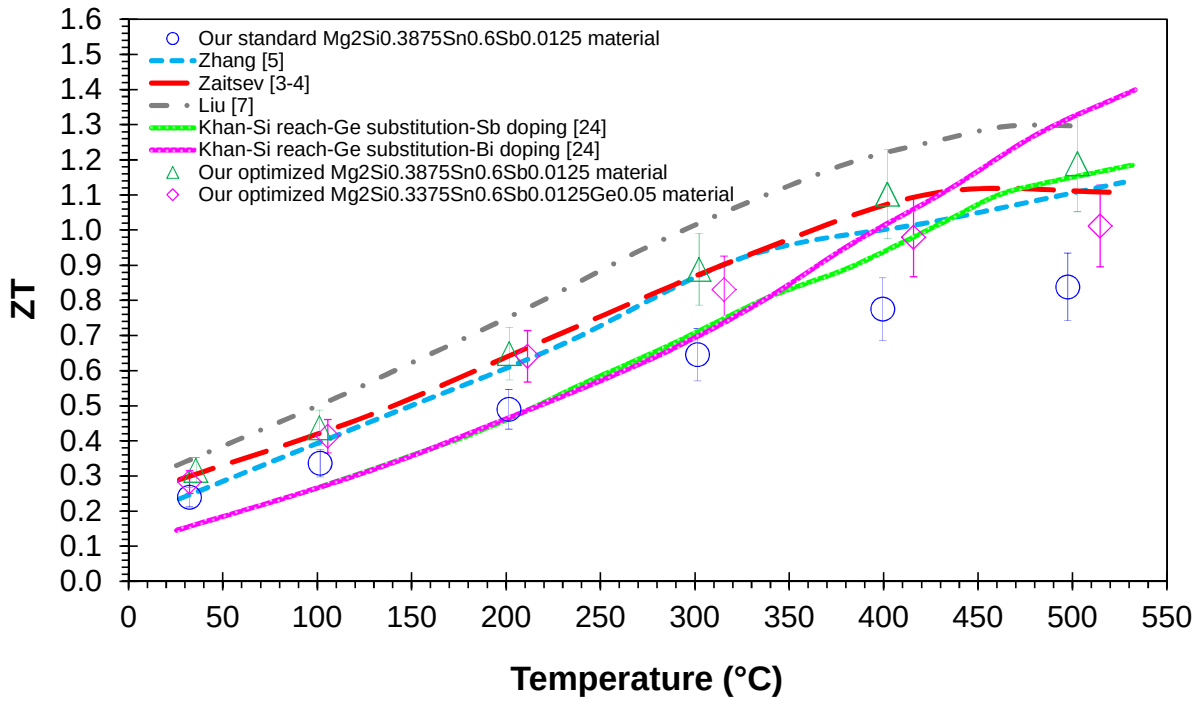


Figure 13: ZT parameter as a function of temperature of N-type $Mg_2Si_{0.3375}Sn_{0.6}$ $Sb_{0.0125}Ge_{0.05}$ nanocomposite, obtained by self-precipitation approach

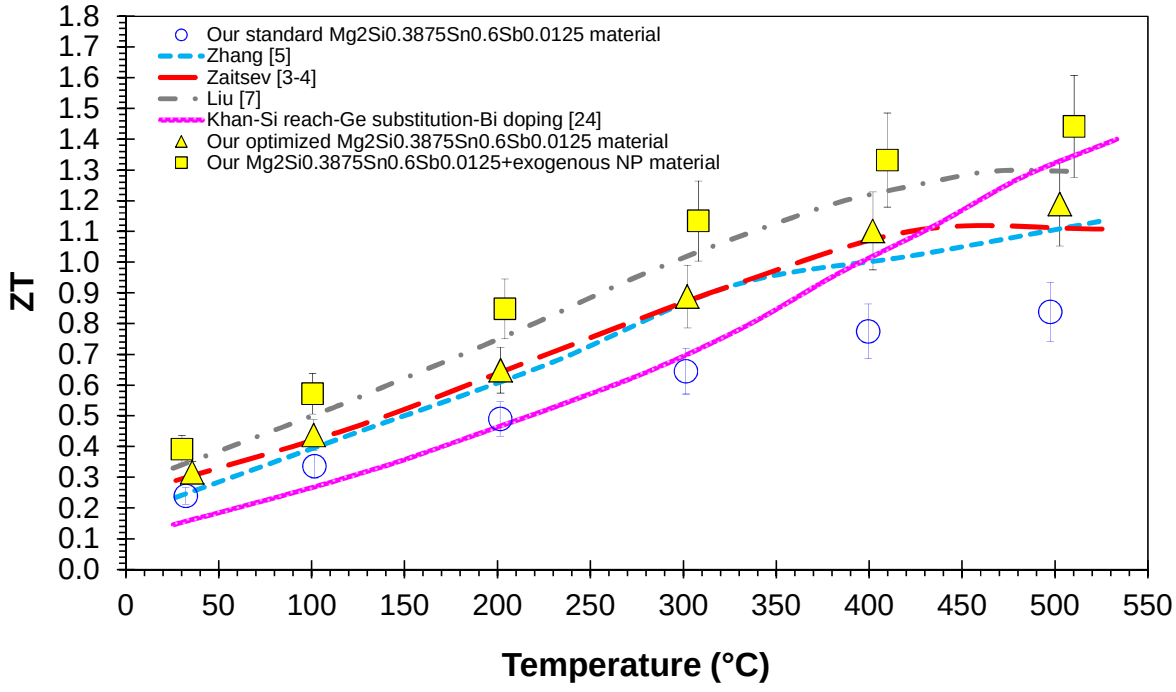


Figure 14: : Final comparison of the thermoelectric figures of merit of best NEAT N-type $Mg_2Si_{0.3875}Sn_{0.6}$ $Sb_{0.0125}$ nanocomposite as compared to the state-of the-art

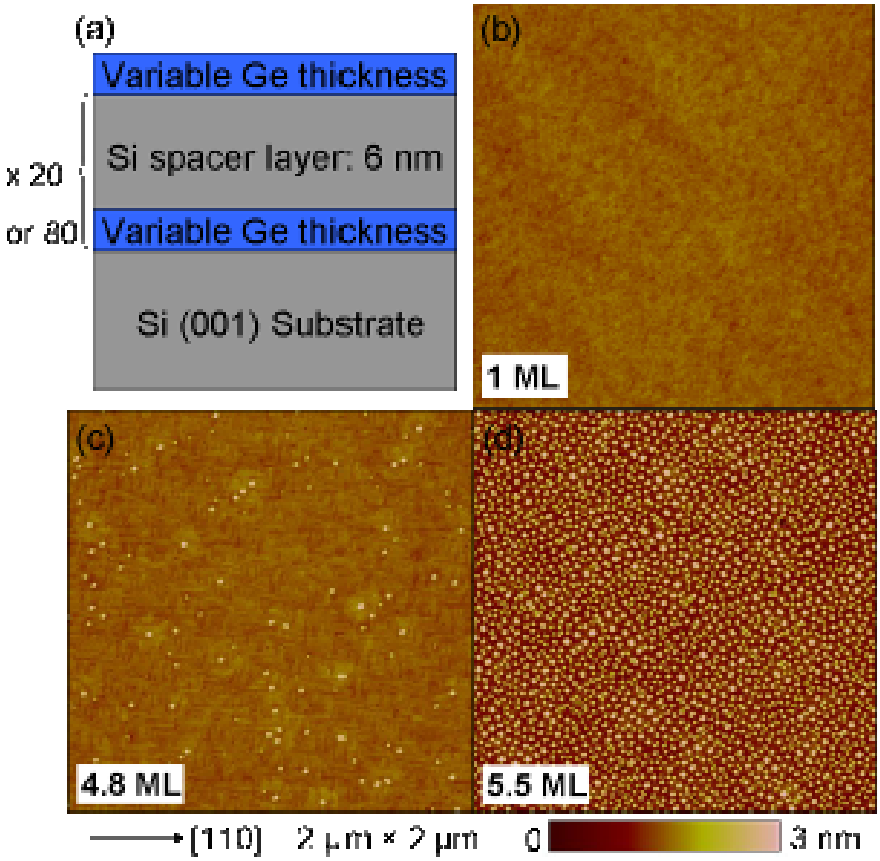


Figure 15: (a) schematic illustration of a Ge/Si multilayered structure; AFM image of the surface of Ge/Si multilayers with 20 periods when the Ge amount per period is (b) 1 ML, (c) 4.8 ML, (d) 5.5 ML. Dots start appearing at a critical thickness of about 4.4 ML.

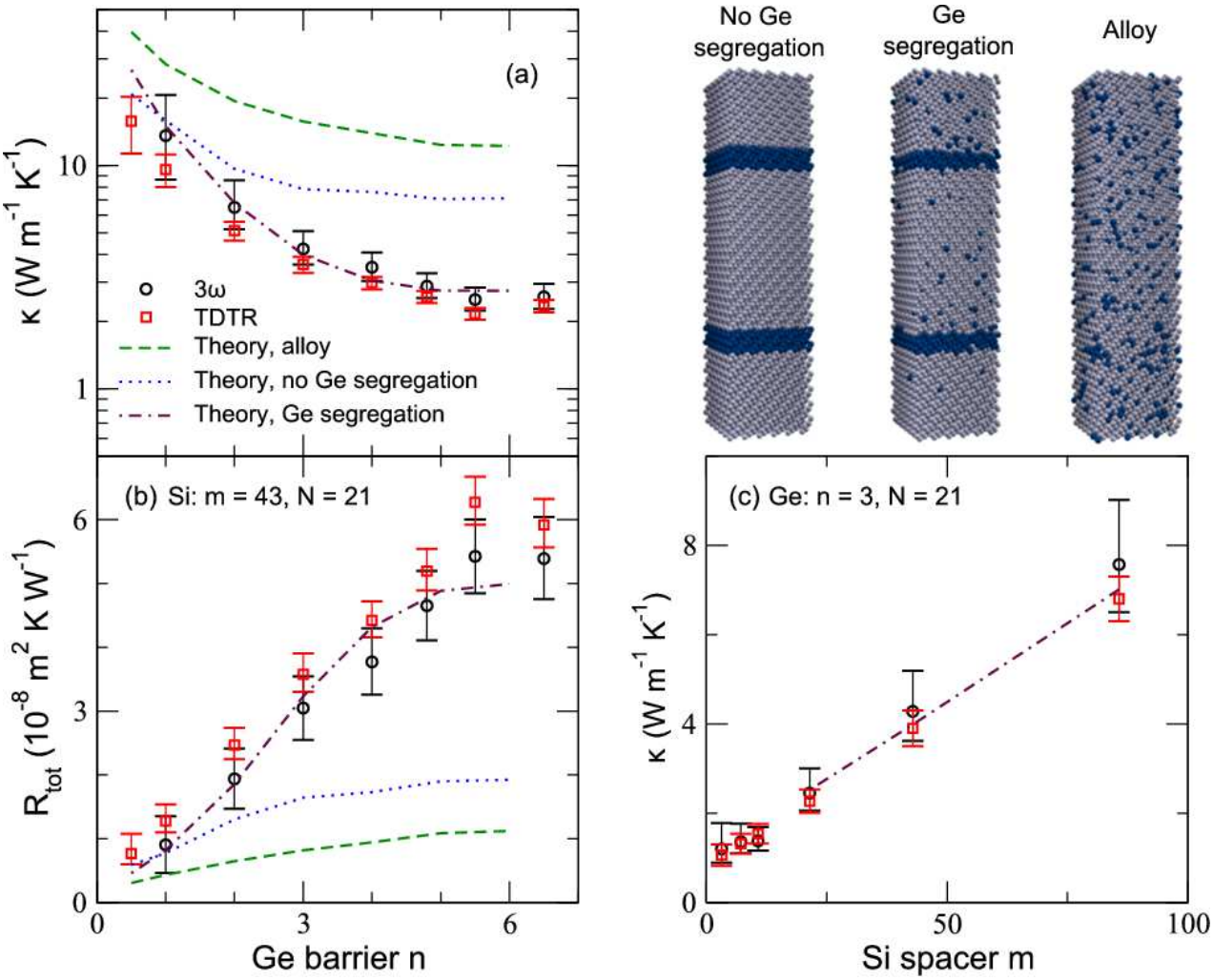
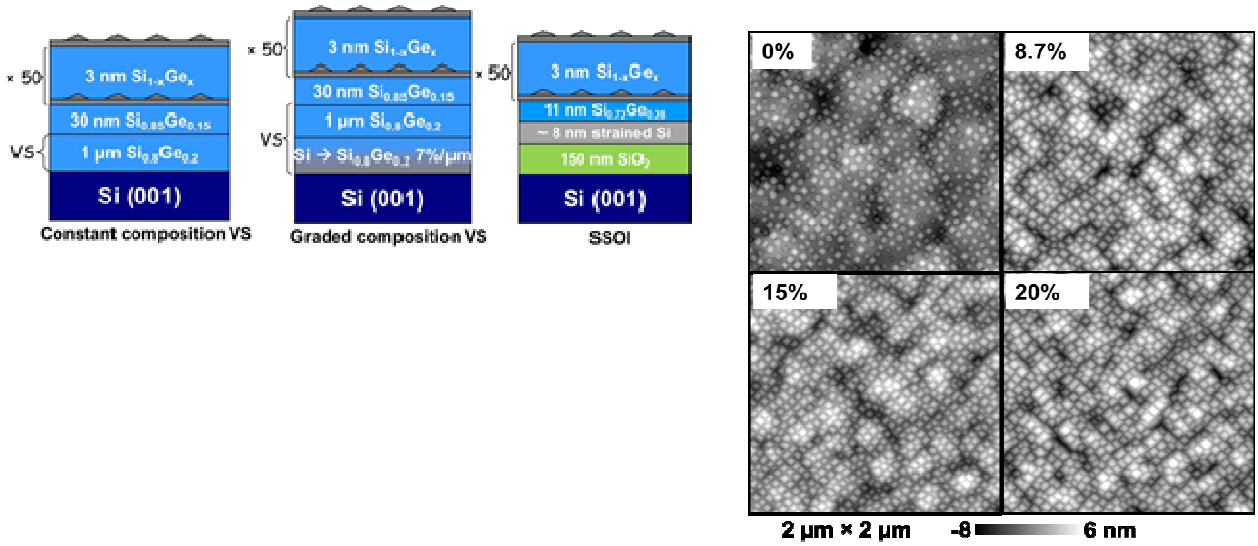


Figure 16 (a,b) : Comparison of experimental and theoretical thermal conductivity and total thermal resistance R_{tot} of thin film Ge/Si superlattices model systems for different Ge barrier thicknesses n, with a constant Si spacer thickness m=43. (c) Comparison of experimental and theoretical thermal conductivity as a function of Si spacer thickness m, for a constant Ge barrier equivalent thickness n of 3 ML.



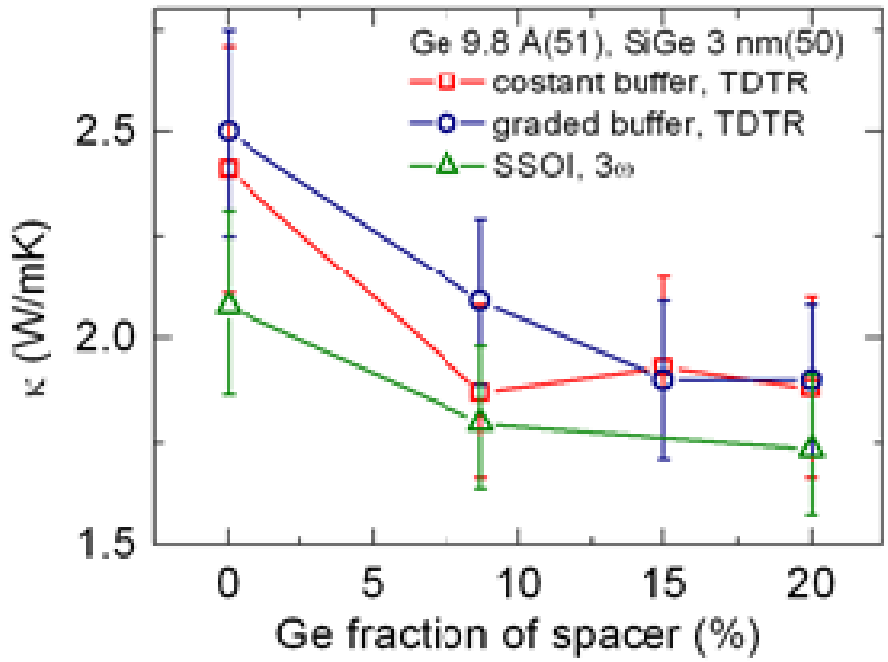


Figure 17: (a) Sketches of Ge/SiGe nanodot multilayers grown on two kinds of virtual substrates and on a SSOI wafer. (b) AFM images of the topmost layer grown on SSOI wafer. Similar to the multilayers grown on SiGe VSs, the Ge fraction in the matrix was systematically varied. The observed roughness stems from the roughness already present before multilayer growth. (c) Measured thermal conductivity as a function of Ge fraction in the SiGe matrix.

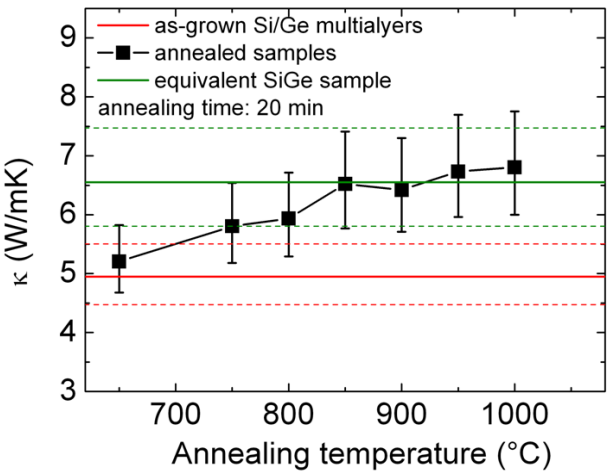
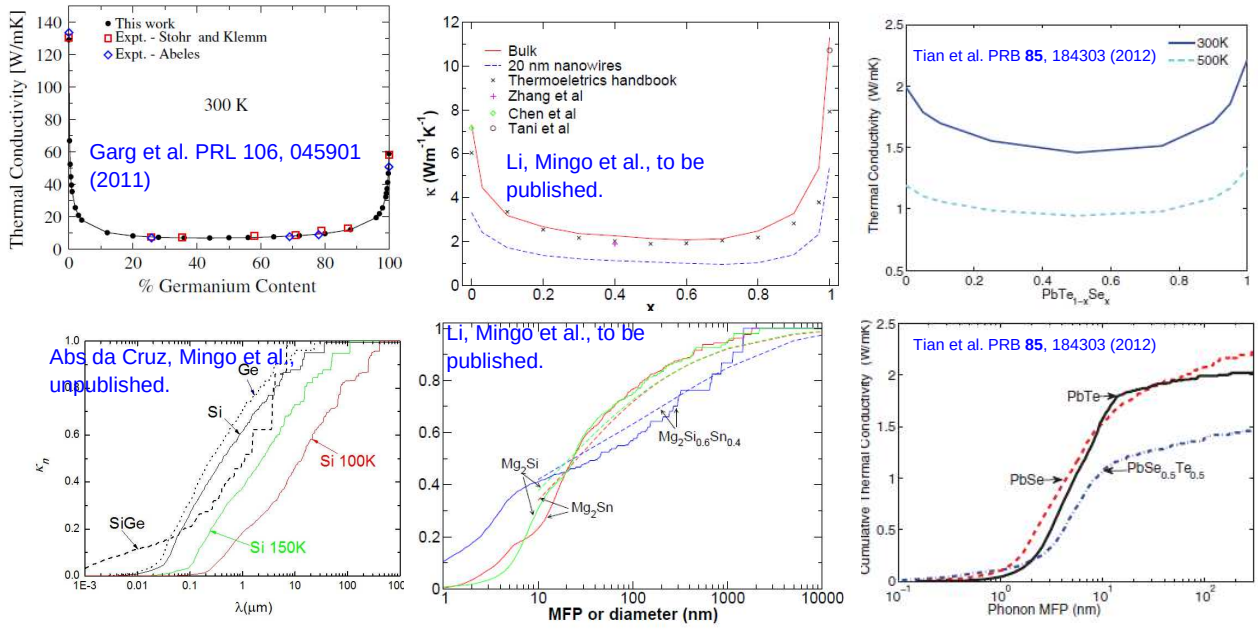


Figure 18: Thermal conductivity of annealed samples as a function of annealing temperature. The red and green lines are the thermal conductivities of as-grown Si/Ge multilayers and the equivalent SiGe alloy, respectively. The dashed lines represent the uncertainties of the measured thermal conductivity. The black symbols refer to annealed samples from 650°C to 1000°C for 20 min. The cross-plane thermal conductivities are measured by differential 3ω method at room temperature.



Si: 140 W/m-K **Mg$_2$Si: 11 W/m-K** **PbTe: 2 W/mK**

SiGe alloy: 10% of pure phase. **Mg$_2$SiSn alloy: 25% of pure phase.** **PbTeSe alloy: 75% of pure ph.**

Figure 19: Cumulative thermal conductivity as a function of phonon mean free paths or nanostructure diameter for SiGe (keft), Mg2siSn (center), PbTeSe (right)

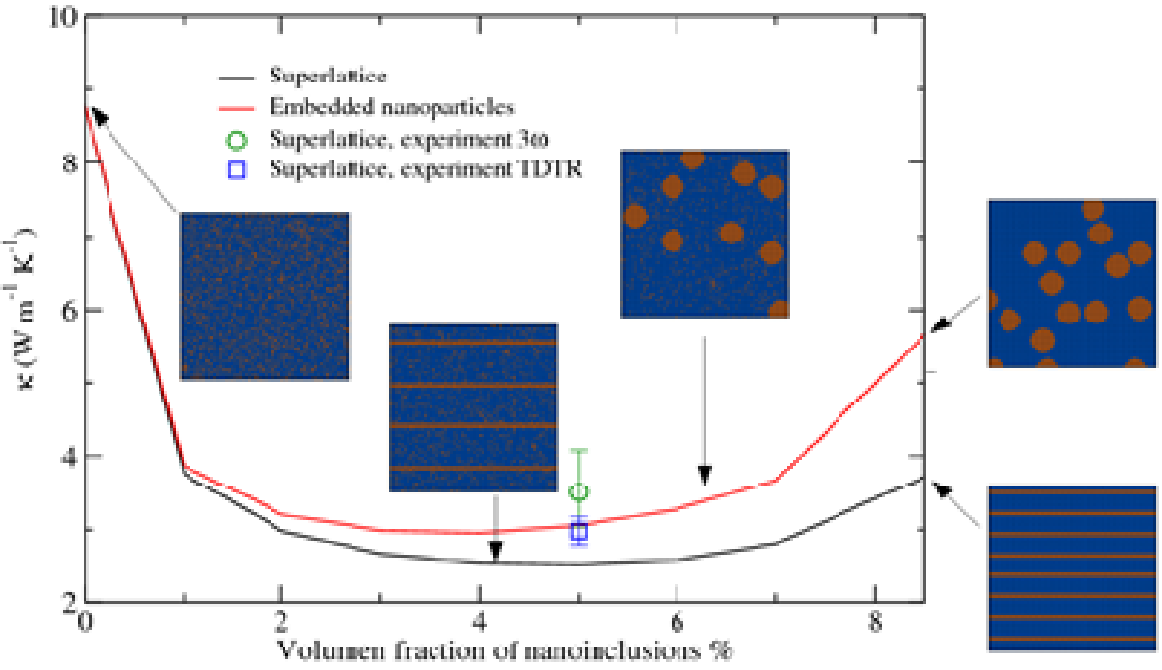


Figure 20 : Computed thermal conductivity of SiGe nanostructures with different Ge distribution (alloy, nanodots, superlattices) as a function of the volumic fraction of nanoinclusions. The symbols indicate experimental results on thin film samples.

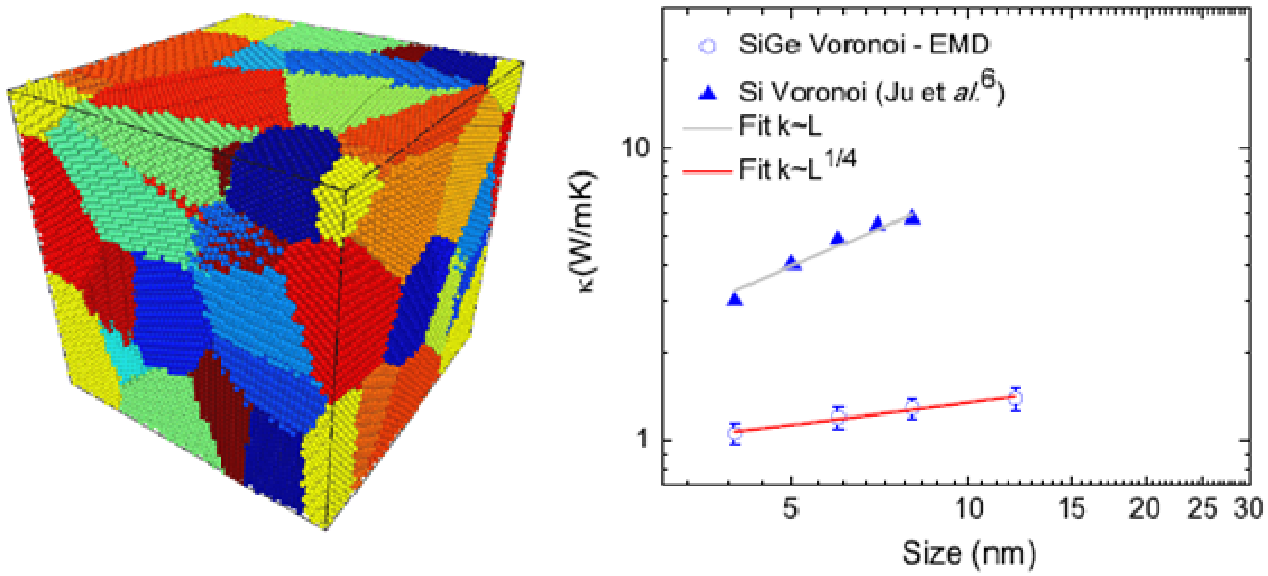


Figure 21 : Nanocrystalline model created using the Voronoi tessellation method (left) and resulting thermal conductivity computed by Molecular Dynamic as a function of average grain size (right)

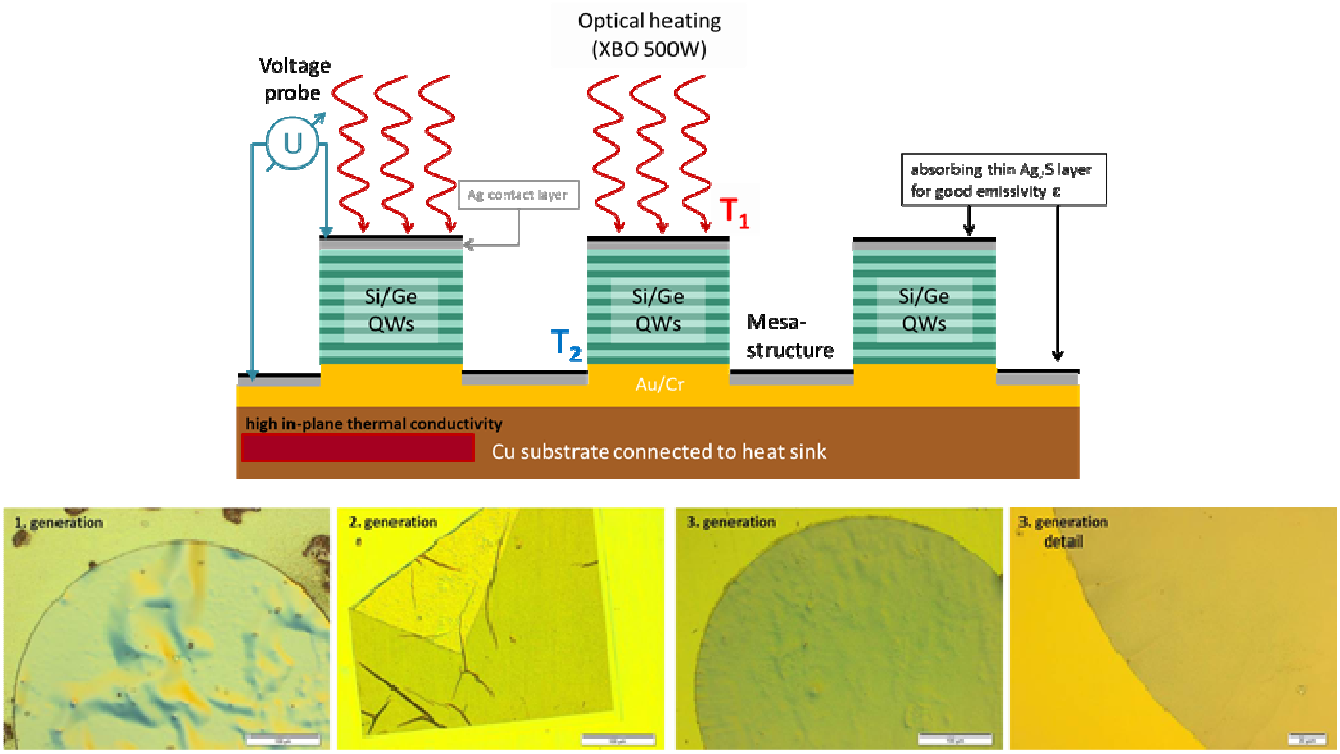


Figure 22: Sketch of an alternative approach developed within NEAT to determine the cross-plane Seebeck coefficient of SiGe multilayers (top) using Ge/Si multilayer membranes on Au-coated copper. The process has been optimized concerning problems with voids, wrinkling or folding. Smooth and flat membranes are obtained finally (bottom).

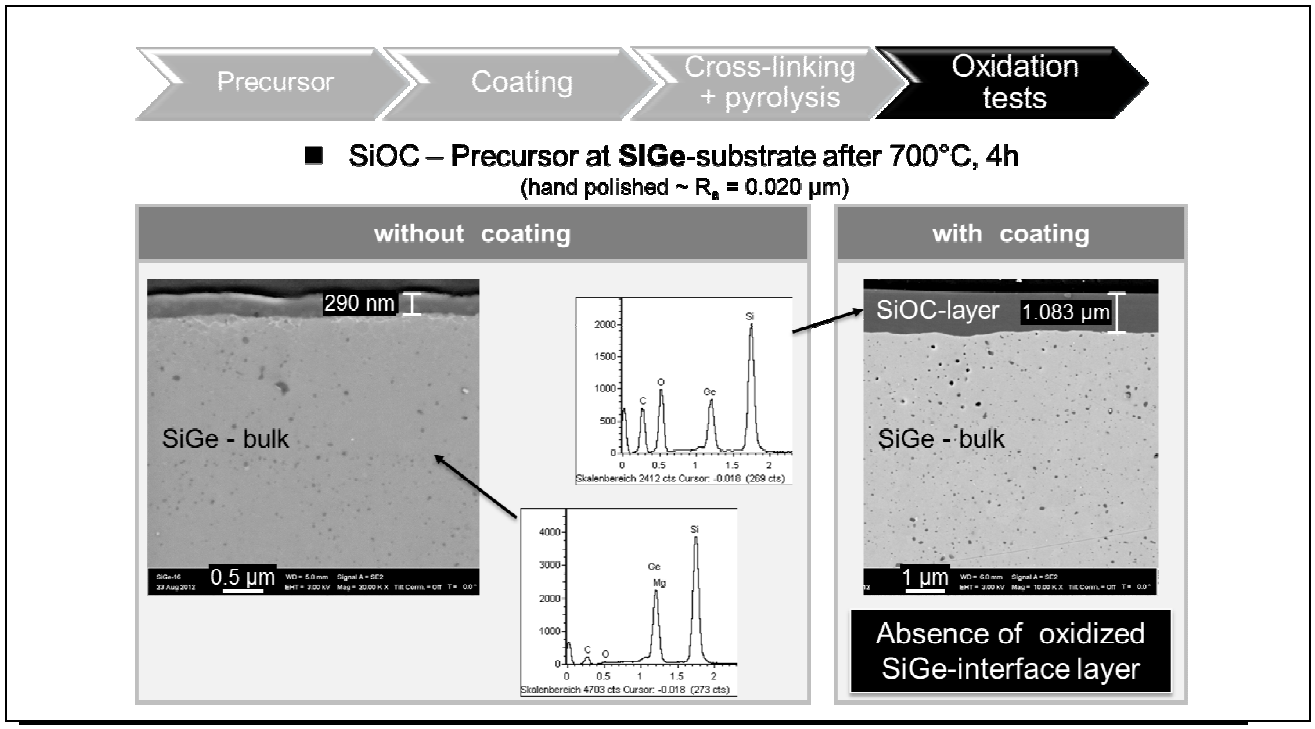


Figure 23 : SEM cross sections of $Si_{0.8}Ge_{0.2}$ thermoelectric leg after oxidation without protective coating (left); and with protective coating (right)

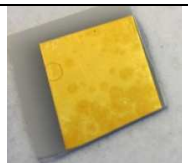
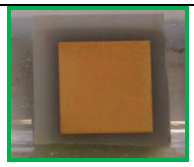
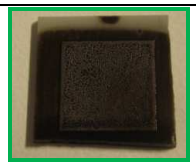
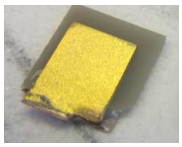
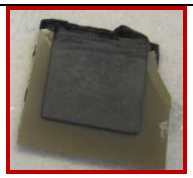
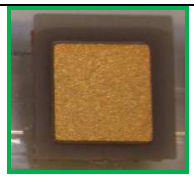
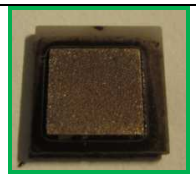
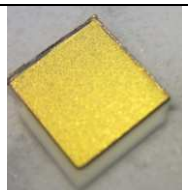
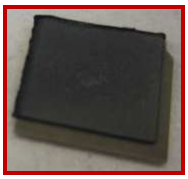
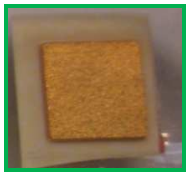
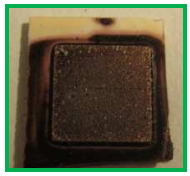
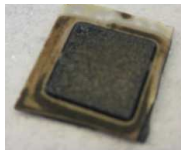
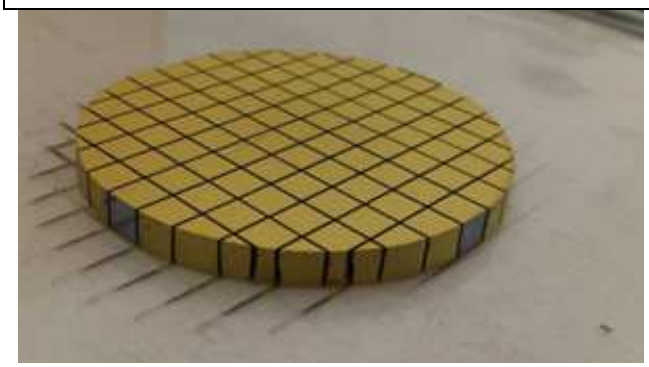
	As received	Uncoated after oxidation	Dip coated	Pyrolized	Dip coated after oxidation
AlN-W-Au					
AlN-Cu-Au					
Al_2O_3-Cu-Au					

Figure 24 : Pictures of AlN-W-Au, AlN-Cu-Au and Al_2O_3-Cu-Au substrates as received, after oxidation without protective coating, after dip coating, after pyrolysis and after oxidation with protective coating



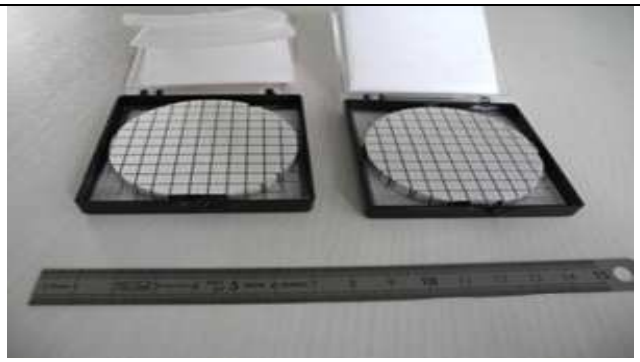
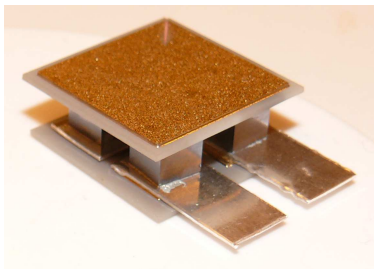
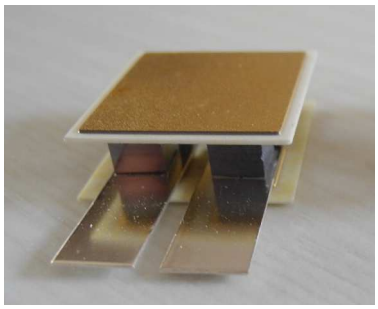
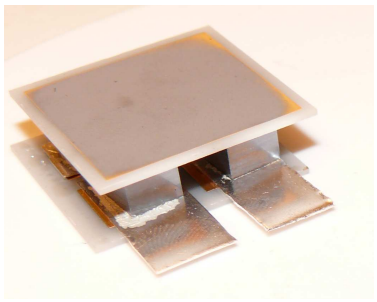
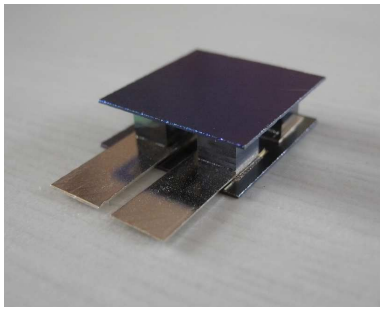


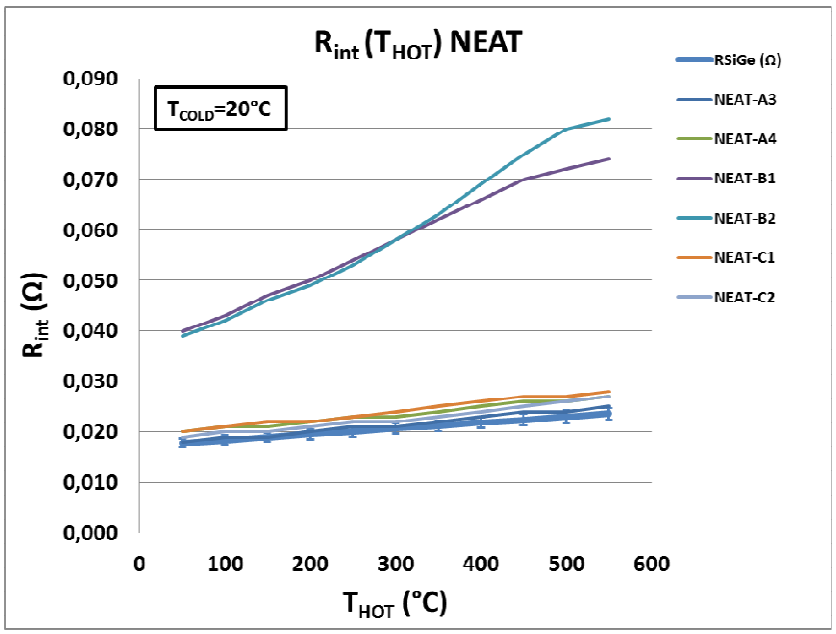
Figure 25 : 60mm pellets of P-type Ti/Au $Si_{0.8}Ge_{0.2}$ (left) and P&N type $MoSi_2$/Ag $Si_{0.8}Ge_{0.2}$ (right) for TEG fabrication.











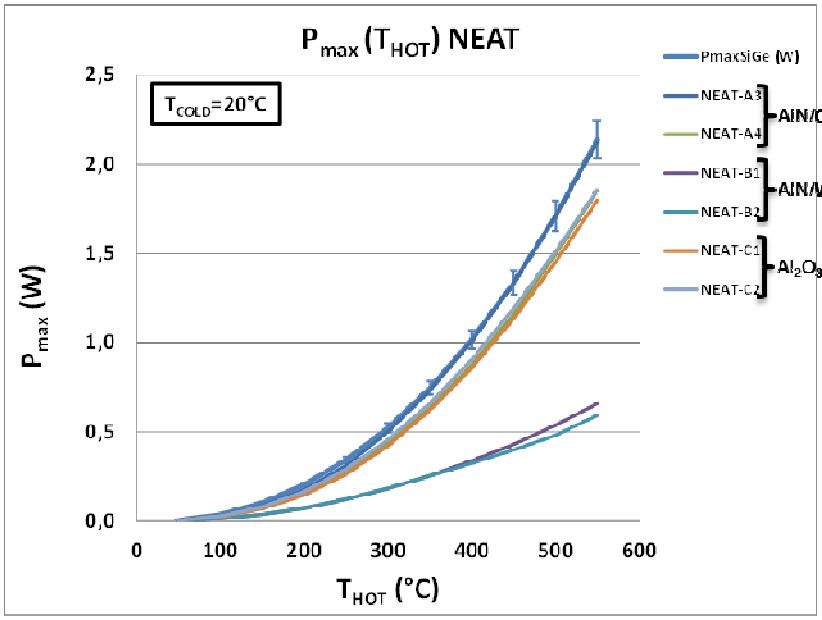


Figure 26: Pictures of the different TEG architectures developed in NEAT using (from top to bottom left) AlN/Cu and Al_2O_3 commercial DBC substrates or NEAT developed alternative AlN/W and Poly-Si/Ag substrates; Internal resistance of these TEG modules (top right) and Maximum output power (bottom right) as a function of hot side temperature (cold side temperature=20°C) for $Si_{0.8}Ge_{0.2}$ reference host matrix.

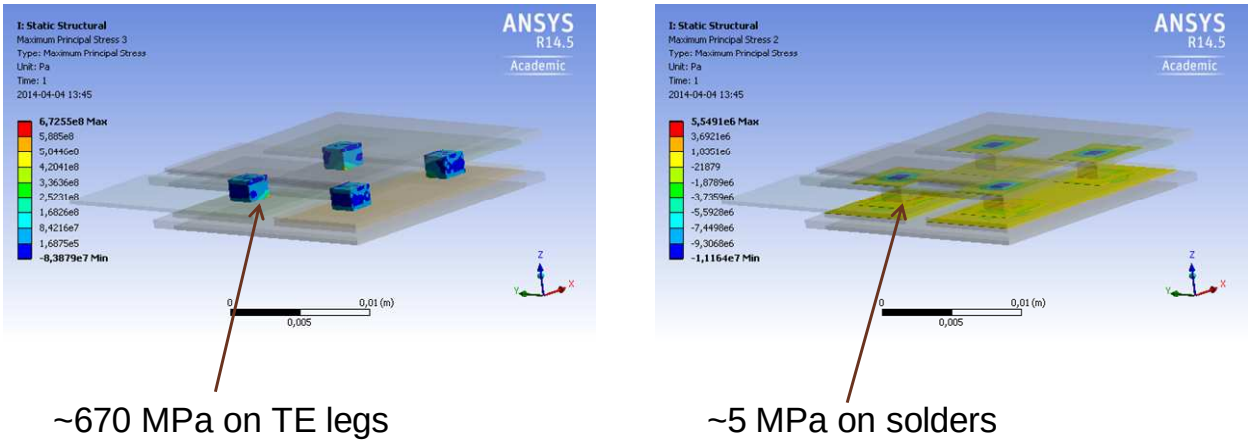


Figure 27: Results of thermo-mechanical models for final proof of concept TEGs : the maximum stress on the TE legs (left) and the maximum stress on the solder joints (right) in a representative load case.

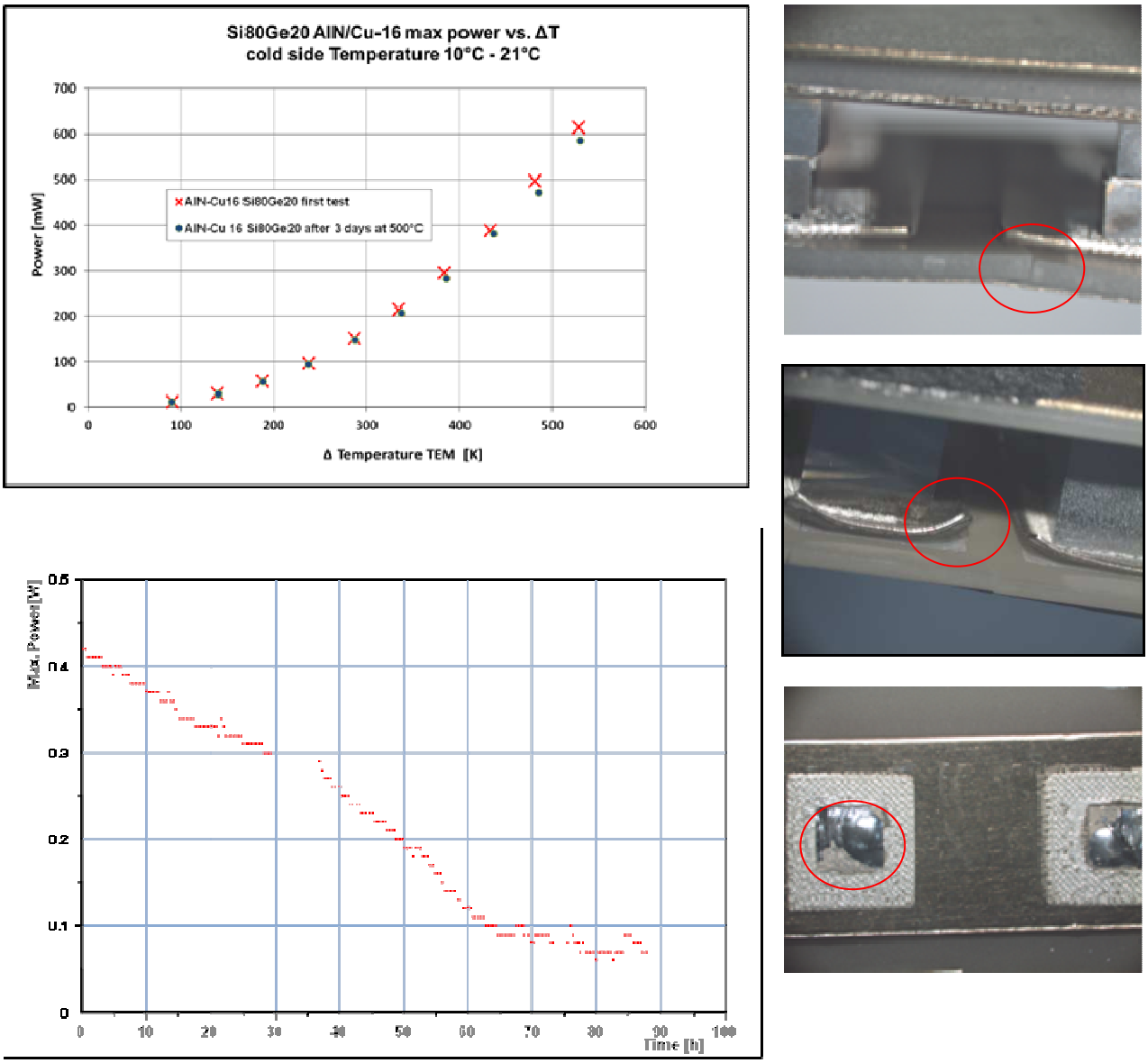


Figure 28: Maximum output power versus thermal gradient of $Si_{0.8}Ge_{0.2}$ AlN/Cu TEG : before and after 3 days at 500°C (top left) and as a function of time during a 100h thermal cycling test without encapsulating (bottom left); Detailed views of some observed failure mechanisms in TEG modules after steady-state test (top right), thermal cycling tests (center right) and after cold shake tests (bottom right)

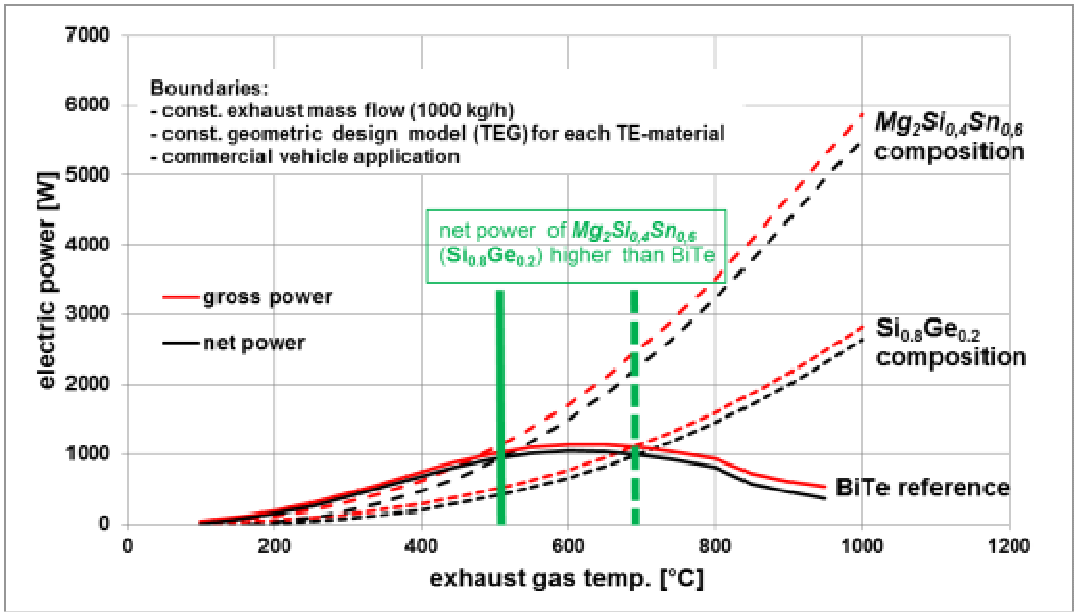


Figure 29 : Comparison of NEAT silicon based materials performance with Bi_2Te_3 commercial material reference in an automotive use case

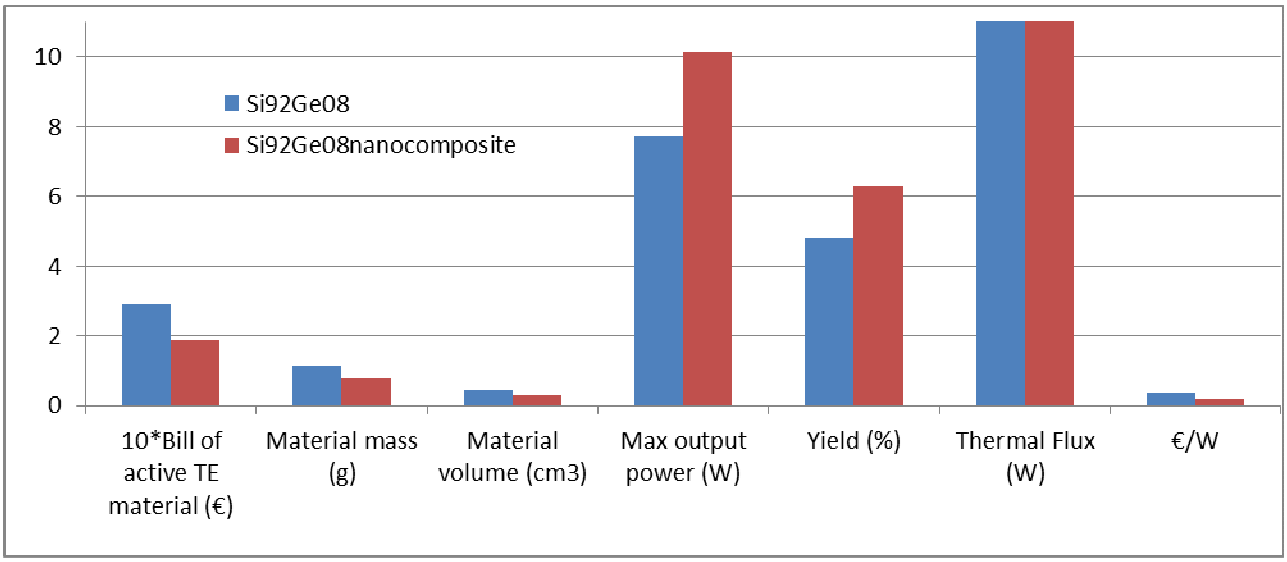
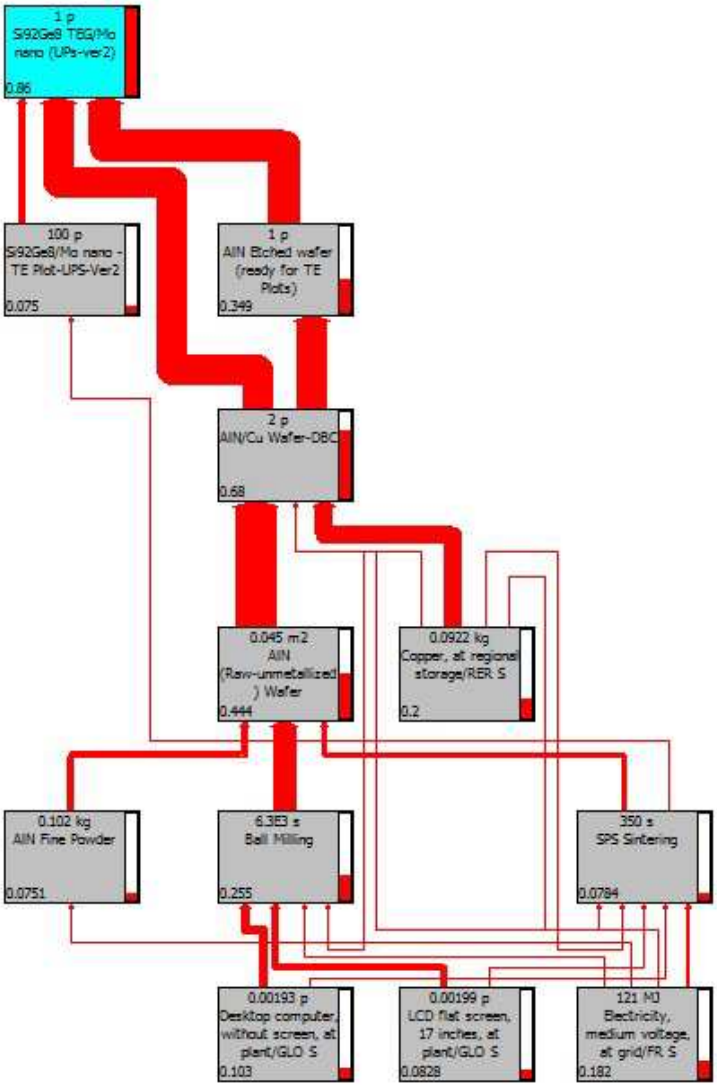


Figure 30 : Comparison of the 2 Proof of Concept TEGs performance based on $Si_{0.92}Ge_{0.08}$ host matrix (blue) or best NEAT $Si_{0.92}Ge_{0.08}$ nanocomposite (red)



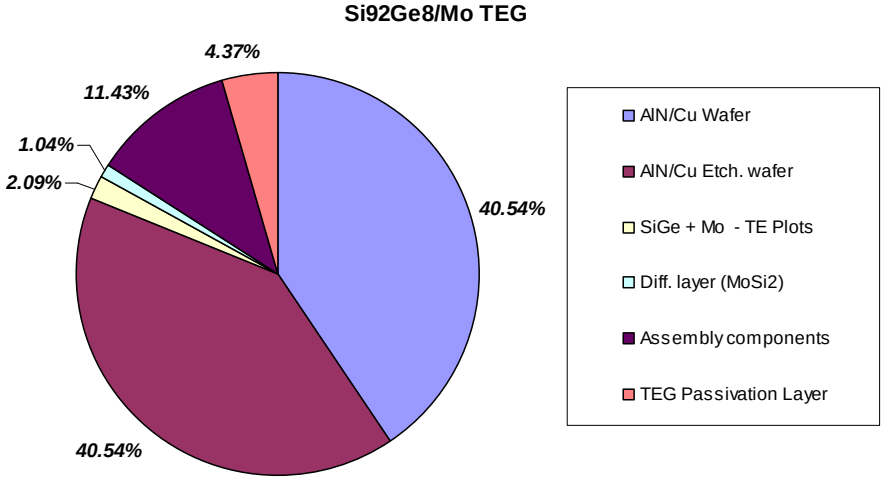


Figure 31: Life cycle Analysis models output of NEAT $Si_{92}Ge_8$ nanocomposite TEG processes : production process tree (top); and cost distribution (bottom)

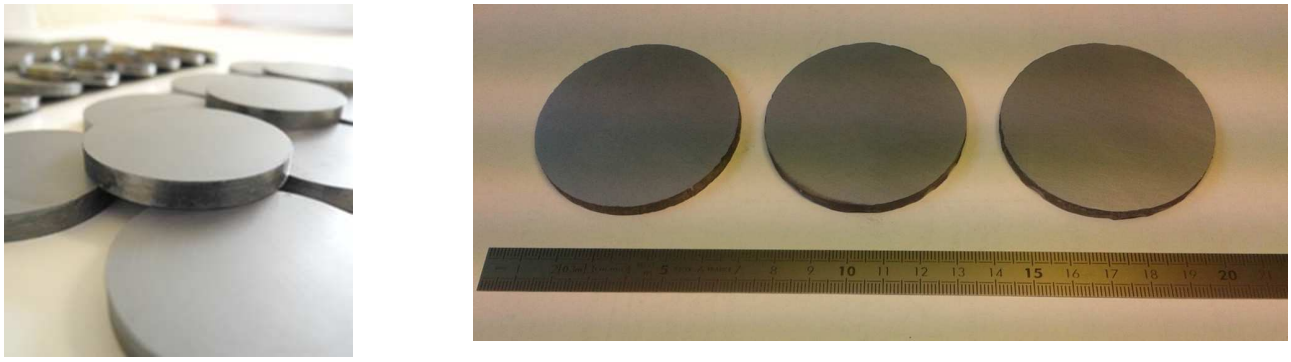


Figure 32: Demonstration of synthesis (3kg batches) and sintering scalability of the host matrix processes developed with NEAT : 60mm diameter pellets sintered by SPS of P-type $Si_{0.8}Ge_{0.2}$ host matrix alloys (left) and, N-type $Mg_2Si_{0.4}Sn_{0.6}$ (right)

Additional information regarding the project is in the project web-site at the following url: http://www.neat-project.eu/. For further details, contact NEAT coordinator Dr Julia Simon at julia.simon@cea.fr.