4.1 Final publishable summary report

4.1.1 Executive summary

Intensive research and development work on carbon nanotubes (CNTs) has been ongoing for over a decade, whereas commercial products available for exploitation by society are limited. Products on the market typically feature CNTs in composites for lightweight reinforced structural materials, taking advantage of the highly desirable mechanical properties of nanotubes. The CNTs used for these purposes do not need to have good electrical properties, and can be mass produced cheaply. In contrast, making nanotubes available for consumer electronics (processors, memory devices) and niche electronics (ultrasensitive sensors, very low power devices) applications will require pristine, single walled CNTs where the electrical properties are as close to the theoretical best values as possible. The properties to consider include carrier mobility, which is affected by not only the defect density on the tube itself, but also its interfaces with the environment.

This project focused on optimizing process flows for carbon nanotube based transistor in order to achieve low contact resistances and high device performance. The main points to consider were the stability of the materials used, preservation of the high quality CNTs throughout the process, and scalability of any developed process to a large enough scale for commercial applications. While there are several obstacles remaining in the way to having practical commercial products featuring CNTs, this project contributes to our understanding and coping with a key challenge: having a pristine nanotube at the end of the process flow. Very often, nanotubes are exposed to a variety of chemicals and harsh treatments throughout the fabrication process of a transistor. These include was photoresists, plasma cleaning steps and oxidation.

The approach taken in this project was to invert the flow of the conventional transistor fabrication process, thus making the nanotube growth the last step executed. In this way, the CNT came into contact with none of the chemicals nor the cleaning procedures. The results present a process for transistor structures, as well as an evaluation platform for arbitrary post-processing and coating experiments. The resulting process is a 2-mask, photolithography based fabrication flow, using deep-UV illumination and image reversal to achieve small features (down to 1.6 µm). Batch fabrication of hundreds of transistors is possible at chip level, and scaling up to wafer level is foreseen to yield thousands of transistors per run. In its current state, the process takes 4 days to complete from blank wafer to transistors.

The results demonstrated through the project are: a process flow that yields ultraclean carbon nanotube transistor stuctures, and a platform for evaluating the effects of specific treatments on

structural and electrical properties of nanotubes. The platform can be a basis for controlled experiments for isolating and understanding the way specific processing steps (such as exposure to chemicals, plasma, various atmospheres) change transistor behavior. Additionally, it can be used for studying transport properties in nanotubes and sensing mechanisms in gas sensors based on CNFETs.

4.1.2 Project Context and Objectives

Intensive research and development work on carbon nanotubes (CNTs) has been ongoing for over a decade, whereas commercial products available for exploitation by society are limited. Products on the market typically feature CNTs in composites for lightweight reinforced structural materials, taking advantage of the highly desirable mechanical properties of nanotubes. The CNTs used for these purposes do not need to have good electrical properties, and can be mass produced cheaply. In contrast, making nanotubes available for consumer electronics (processors, memory devices) and niche electronics (ultrasensitive sensors, very low power devices) applications will require pristine, single walled CNTs where the electrical properties are as close to the theoretical best values as possible. The properties to consider include carrier mobility, which is affected by not only the defect density on the tube itself, but also its interfaces with the environment.

The main objective of this project, as stated in the Annex I to the Grant Agreement, is optimizing contacts to carbon nanotube field effect transistors (CNFETs), whereby the resistance between the channel and the source/drain contacts of the device were articulated. Contact resistance, along with threshold voltage, gate coupling, subthreshold swing and hysteresis effects, is a major parameter to be controlled in order to make CNFETs realistically available for commercial use. During the first half year of the first (and only) period of the project, interfaces with insulators surrounding the nanotube and the source/drain contacts were identified as a significant area to improve, and thus the project objectives were widened to include this goal, as well. Figure 1 shows a schematic of a CNFET, where relevant resistances and interfaces are observable. In this project, we pay close attention to the four interfaces surrounding the CNT: the source and drain contacts, the gate dielectric and the passivation layer.

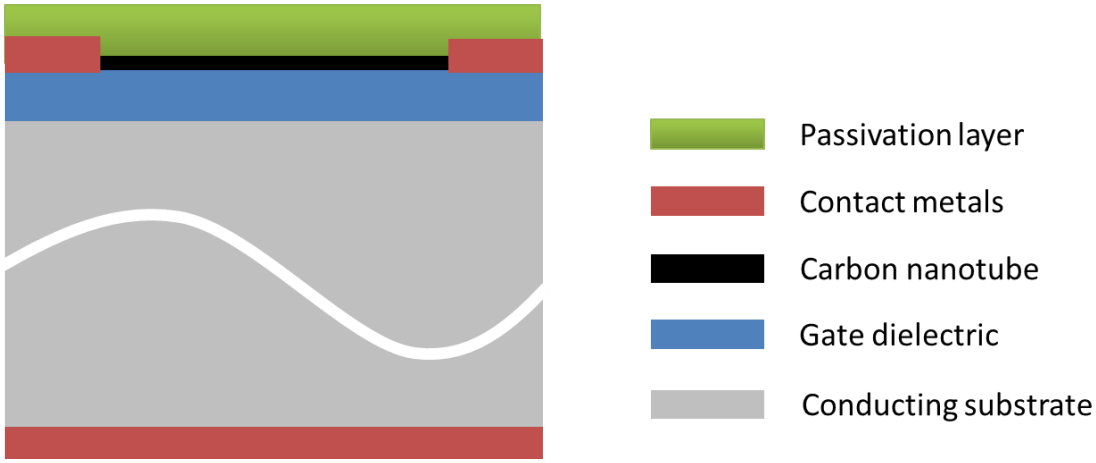

Figure 1: Schematic of a typical carbon nanotube field effect transistor

The process flow for fabricating CNFETs has a determining effect on the resulting contact resistances and quality of the interfaces with insulators. Conventional transistor fabrication techniques, both with photolithographic and electron-beam based processes, include photoresist materials in contact with the nanotube. Complete removal of these organic resins is difficult, and often requires harsh cleaning steps which would be deleterious to the quality of the nanotube itself. Therefore, an alternative approach is chosen in this project, where the nanotubes are grown as the last step of the process flow. Therefore, there is no contact with chemicals, and interfaces are kept ultraclean. A comparison of the metallization-last and nanotube-last approaches to CNFET fabrication is presented in Table 1.

Nanotube growth last	**Source/drain metallization last**
Nanotube does not contact any chemicals	Nanotube exposed to photoresist, solvents, bases
Thermal budget for metal contacts critical	Metals deposited at low temperature
Choice of contact materials limited	Large variety of contact materials available
Pristine, high quality nanotubes expected	Defects can be introduced on CNT via processing

Table 1: Comparison of CNT-last and metal-last process flows

A nanotube-growth last process was developed following these arguments. As an important feature of the process, it must be noted that additional objectives of batch process-compatibility and suspended nanotubes (no contact to the substrate) were added. These objectives are well in line with the desired progress toward making CNTs viable for commercial use.

4.1.3 Main Results

The first experiments carried out during the project period were designed for the evaluation of doped semiconductor materials as contacts to carbon nanotube transistors. These materials were envisioned as candidates for source and drain contacts to the CNT, the rationale being that their bandgaps can be tuned to give the desired band line-ups for optimal conduction. ZnO doped with Aluminum was selected as a prototype highly doped semiconductor, due to its compatibility with processes with CNTs. Additionally, Al:ZnO was expected to give high conductivity and an ohmic contact with an Au/Al metal stack, which could be deposited subsequently.

Several challenges were identified early in the project, namely, high density doping of ZnO with aluminium ($N_D=10^{19}$ cm^{-3}) yielded low mobility in the material (100-300 $cm^2/V \cdot s$). As a result, the conductivity of the material was significantly lower than that of metals. It became clear that the development effort would give high contact resistances, even after the process complexity was increased to accommodate the doped semiconductor deposition with atomic layer deposition. The material was replaced with high work function metals in order to approach the problem from another angle: instead of attempting to eliminate the Schottky barrier at the contact regions, we instead focused on the smallest possible Schottky barrier and minimizing the contact resistances coming from process non-idealities. Platinum was the prototype high work function metal used for the rest of the project.

In order to optimize the contact resistance and the interfaces of the CNT with surrounding dielectrics, an ultraclean process flow was developed. Existing processes and designs from the fellow's host group, the Micro and Nanosystems group at ETH Zurich, were taken as a starting point. Specifically, designs and preexisting processes from Kiran Chikkadi were taken to serve as the first iteration of the process. In addition to saving valuable time, this ensured a pre-approved initial state for use in the cleanroom facilities. Major changes to the process came as migration from on-substrate to suspended tubes was achieved through trench structure fabrication. A nanotube-growth-last flow was adopted during the second year of the project period, leading to further significant changes to the initial process flow.

The initial design featured 10 sets of parallel electrodes, which were kept as they were for the design used in this project. The electrodes, which were set on substrate previously, were

located on the top surface of trench structures for this project. In order to identify the most important geometric parameters of the design and to optimize the structure, electrostatic simulations using COMSOL Multiphysics were carried out. The simulated structure is shown in Figure 5, where the main geometric parameters, gate dielectric thickness (t_{ox}), trench depth (d_{trench}) and width (w_{trench}) are marked.

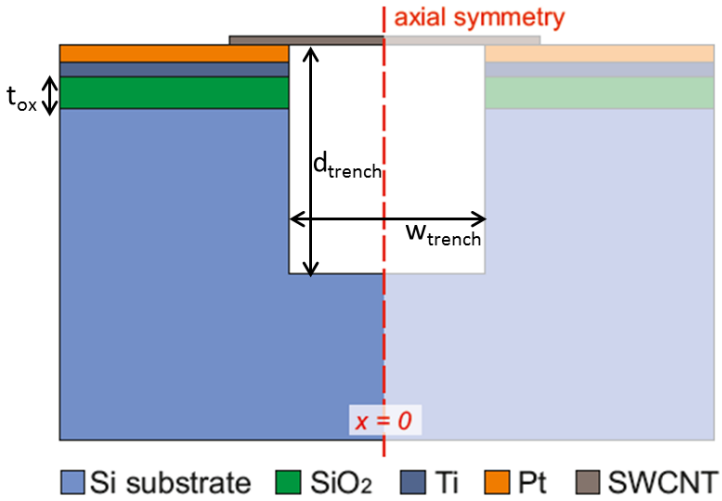

Figure 2: Trench structure as simulated. For reduced complexity, only half of the structure was simulated (to the left of the axis of symmetry). t_{ox} is the gate dielectric depth, d_{trench} is the depth of each trench and w_{trench} is the width of each trench.

The effect of each geometric parameter on the gate coupling ratio (applied voltage divided by the effective electric potential) at the center of the channel (x=0) was investigated. Figure 6 summarizes the simulation results with the blue curves showing the calculated gate coupling ratio, Γ, at x=0 and the red curves depicting the average over the whole channel. Figure 6(a) shows that the trench depth is only relevant for very shallow trenches, and becomes highly pronounced for values under 0.3µm. This insensitivity comes partially from the fact that the gate material (highly doped Si) extends to immediately below the gate dielectric underneath the contacts. Gating is therefore not limited to the silicon at the bottom of the trench. In order to have a design as immune to process variations as possible, we chose the trench depth to be 2µm. Figure 6(b) shows the effect of the trench width, where we see a weak dependence on this parameter. In order to be least affected by process variations, and to maximize the probability that a single nanotube will grow across each trench, this parameter was fixed at 2µm, as well. The detailed calculations of the bridging probabilities were carried out by Kiran

Chikkadi as part of his doctoral work. Finally, Figure 6(c) shows the dependence of the gate coupling ratio on the gate dielectric thickness. Thinner gate dielectrics, as expected, lead to more effective gate coupling. In order to balance the need for good gate coupling with excellent insulation, the gate dialect (SiO_2) thickness was chosen to be 200nm.

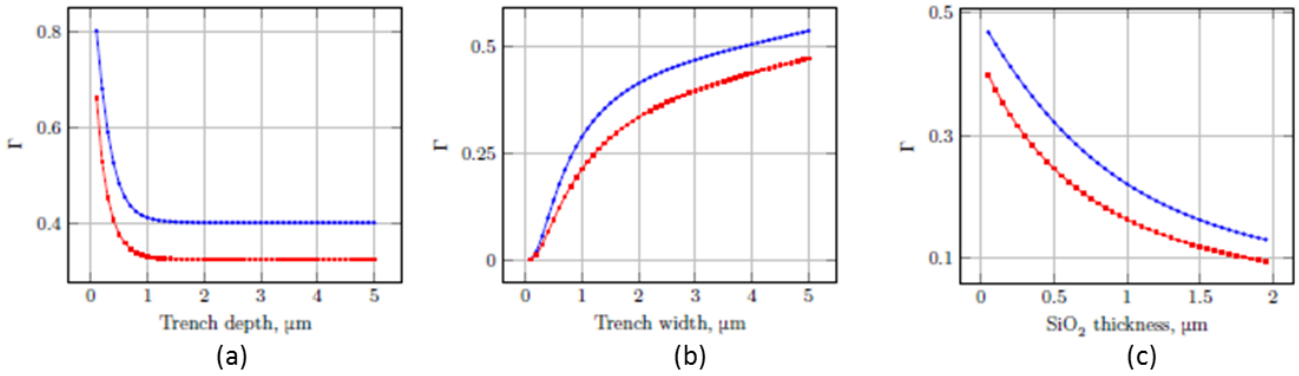

Figure 3: Simulation results on the effects of (a) trench depth, (b) trench width, and (c) gate dielectric thickness on the gate coupling ratio

Once the geometry of the transistor structures was determined through simulations, the exact fabrication steps to create the structures in the laboratory were developed. The process flow is summarized in Figure 4. The main features of the process flow are the dry etching steps for creating the trenches, and the metal evaporation for self-aligned contacts. The dry etching steps were carried out using reactive ion etching (RIE) for the gate dielectric layer and inductively coupled plasma (ICP) etching of the silicon layer.

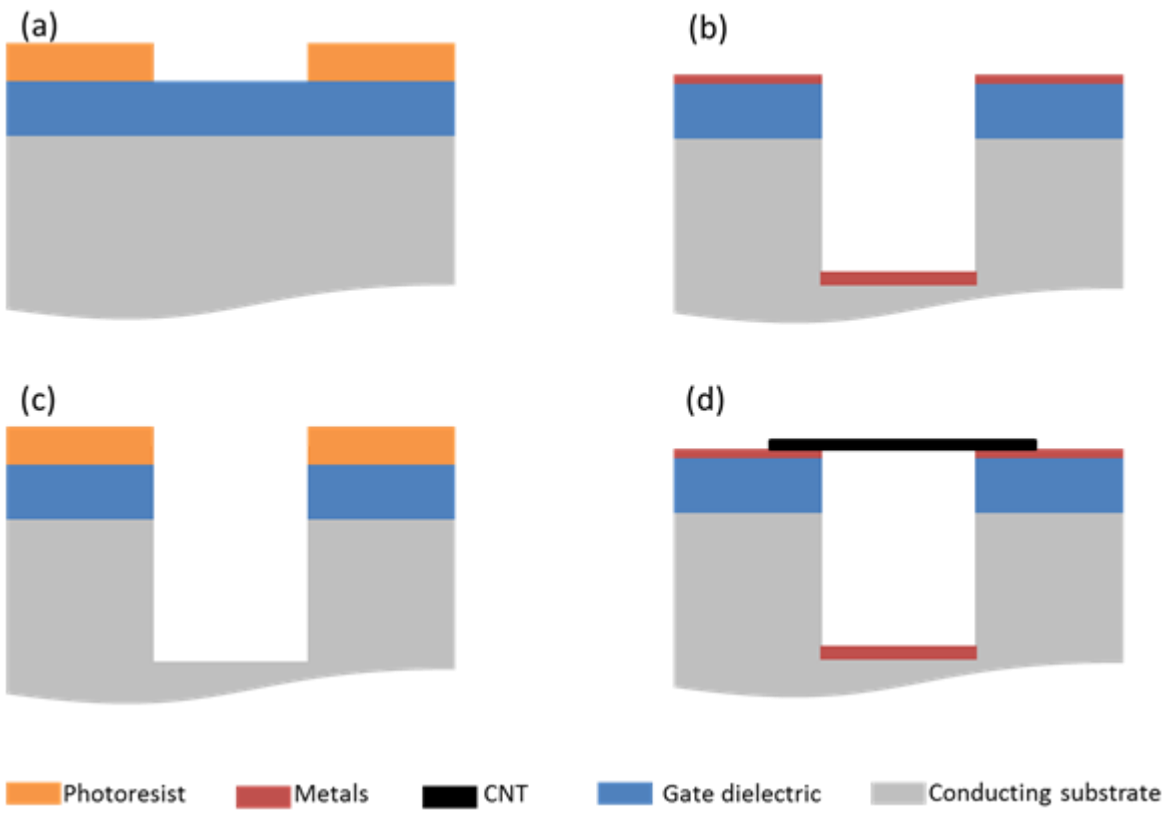

Figure 4: Summary of the process flow. (a) Patterning photoresist using deep-UV illumination, (b) two-step dry etching for trench creation, (c) metal evaporation for self-aligned contacts, (d) CNT growth.

The metals for source and drain contacts were deposited using directional evaporation using an electron beam evaporator. Materials and thicknesses of the layers in the metal stack were chosen after a systematic study to resolve issues related to the thermal robustness of the contacts. Very stable contact materials are necessary in order for the metal stack to survive the growth conditions for CNTs; 850 °C for approximately 15 minutes. Metals that are not highly reactive are desirable for such conditions; however, such metals have low adhesion to insulating surfaces such as SiO2. Therefore, an adhesion layer is necessary, and this layer must also be able to withstand the CNT growth step. After evaluating combinations of Pt and Pd as contact materials with Ti, W and Al as adhesion layers, the most stable combination was found to be Ti/Pt. Thicknesses of the layers were optimized as summarized in Figure 5. The figure shows scanning electron microscope (SEM) images of the metal stacks after they were annealed at 850 °C for 15 minutes. The optimal thicknesses are 10/200nm Ti/Pt. While morphological observations on the electrodes gave the first indications on their stability, leakage current measurements from the source and drain electrodes to the back gate revealed that the 10/200nm Ti/Pt electrodes had no measurable leakage current after annealing. In contrast, short circuits between the source and the gate electrodes were observed with

insufficient metal thickness. Increasing the Pt thickness beyond 200nm did not show additional benefits, and therefore, the final thickness was fixed at 200nm.

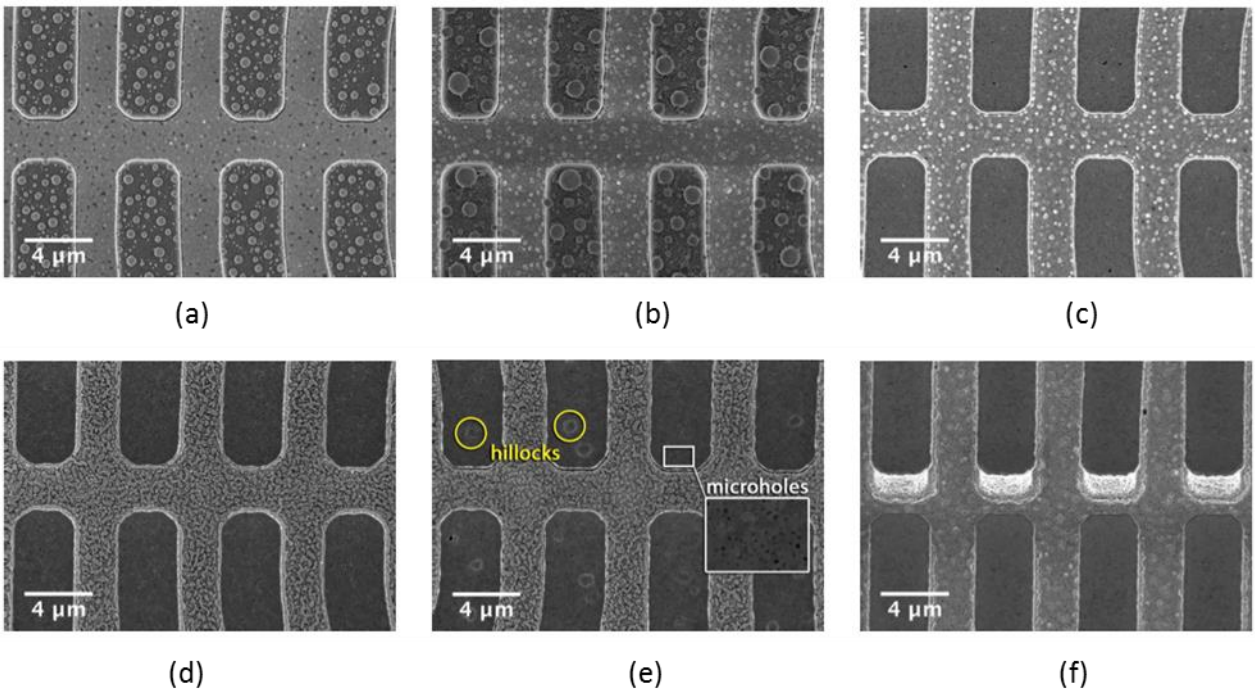

Figure 5: SEM images summarizing the metal stack optimization study. The thicknesses of the Ti/Pt stack are (a) 10/100nm, (b) 10/150nm, (c) 10/200nm, (d) 10/250nm, (e) 5/200nm, and (f) 10/200nm (tilted view).

As a result of the process development effort, a platform where contact resistances and the effects of gate dielectrics can be evaluated was achieved. The platform features three sets of 20 electrodes per chip, with suspended CNTs bridging the electrodes to form transistor structures. Due to a yet unresolved problem with CNT growth, electrical measurements are incomplete at the time of writing this report. The growth issue is related to equipment and materials combinations inside the catalytic chemical vapour deposition chamber, where the hypothesis is that the catalysts are unstable on the host surfaces on top of the electrodes. The main approach to solving the problem is densification of the host surface, which is expected to help catalyst nanoparticles remain at the spot where they are first adsorbed onto the electrode surface.

The platform achieved thus far is conducive to growing nanotubes without the electrode metals, thereby enabling structural characterization of many nanotubes at once. Raman spectroscopy and scanning electron microscopy were used to collect data (continuity, density, diameter) on approximately 300 nanotubes, in order to establish a procedure for evaluating

the effects of processing steps on the health of the nanotubes. The procedure starts by Raman spectroscopy immediately after growth to gather baseline information, and then an arbitrary processing step can be applied (e.g.: metal evaporation, soaking in solvents, ozone cleaning). The processing step is followed by a repeated Raman spectroscopy scan; therefore, comparative data on the location and half-width-at-full-maxima of relevant resonant peaks on the spectra can be collected. An SEM image is taken as the last step in order to put the data in context of whether it refers to a single CNT or a bundle of CNTs. An examples of the comparison carried out in this way is depicted in Figure 6.

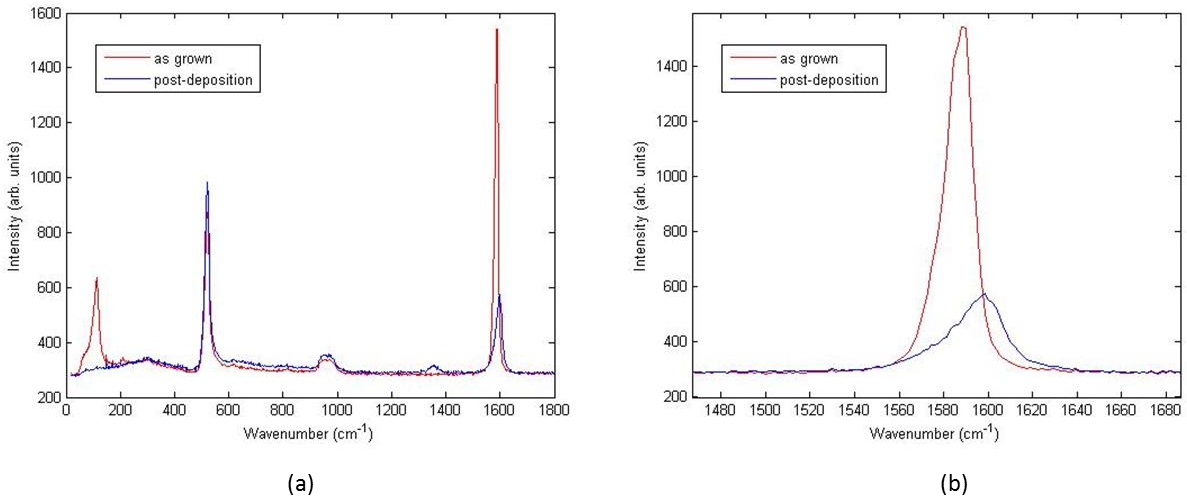

Figure 6: Raman spectrum of an example nanotube before and after insulator deposition. (a) shows the full spectrum, (b) zooms in on the G-peak shift and broadening.

Project management during the period

The management of the project was kept as flexible as possible (while allowing for structured experiment design and implementation). This flexibility is necessary in a fast moving field such as carbon nanotubes research. An example of this management approach is the addition of the objective of optimizing interfaces of CNTs with insulators, as such interfaces proved to be crucial to the performance of any CNT-based device. Another example is the relaxing of the requirement that the contacts to CNTs be made out of doped semiconductors, as was written in the initial project description. After doped semiconductors were shown to be a weak choice, a project management decision to look for an alternative was made.

The status of the project, from a management point of view, is that there is significant progress towards the objectives; however, many additional challenges prevented a full realization of the milestones and deliverables. Fabrication of prototypes is very heavily dependent on equipment availability, which became difficult to predict during the mid-phase of the project. In order to make progress in furthering our knowledge of the field, even without the specific milestones being met, the project was managed in an agile way. For example, as detailed in the "work progress and achievements" section, structural characterization of CNTs using Raman spectroscopy was employed whenever electrical characterization of transistor structures was not an option.

Milestone	Description	Status	Comments
M1	High conductivity ZnO	Proved unfeasible	Practical limits on conductivity of ZnO led to re-evaluation of all following milestones
M2	ZnO crystallinity study	Dropped	Not necessary after M1 changed
M3	Optimized contact process	Dropped	Not necessary after M1 changed
M4	Insulator effects study	Achieved (M16)	Added after project begin
M5	Suspended FET process	Achieved (M24)	Added after project begin
M6	Direct insulator deposition	Achieved (M24)	Added after project begin
M7	Optimized gate process	Partially achieved	Gate insulator achieved, gate metal pending at M24.

Table 2: Status of milestones

Table 2 summarizes the standings of the milestones from Annex I and those added after the first month of the project. It must further be noted that progress on milestones is highly dependent on the availability and health of laboratory equipment. While project management was done to eliminate any idle time (for example, reporting work, analysis, training and outreach activities are done during equipment downtime), delays due to critical break-downs were unavoidable. The most important case was being unable to grow carbon nanotubes for long stretches of time due to catalyst nanoparticle degradation.

Potential Impact

The potential impact of the project is best demonstrated by the continuation of the efforts in the same direction within the Micro and Nanosystems group, as well as the field in general. The results contribute to progress towards batch processed CNFETs, which can be commercially viable with only a few more steps of optimization. Specifically, the presented transistor fabrication and evaluation platform can serve as a test bench for determining the effects of specific process steps and altering these steps. Therefore, there is a wide range of uses for which the results should be made available. Dissemination activities summarized below were aimed at making sure the results reach as many researchers as possible.

Dissemination activities

1. Regular public seminars held at ETH Zurich where progress and results achieved during the project were presented. The fellow held seminars on 01.06.2012 and 18.10.2013,

2. K. Chikkadi, M. Politou, E. Cagin, O. Kurapova, D. M., and C. Hierold, "Investigations on passivation layers for carbon nanotubes transistors for sensor applications," NEMS Tokyo, Japan, 2012.

3. Manuscript in preparation: Effects of surface treatments on SWNTs as evaluated by Raman spectroscopy

An additional impact of the fellowship was the full integration of the fellow into the Swiss research community, and the opportunities for networking and establishing her career that she received. The fellow was able to develop additional skills and to get to know the Swiss research landscape closely. Her next career step will be to join the Interstate University of Applied Sciences (NTB, Buchs) as a senior scientist. In her new role, she will be expected to acquire and lead projects with funding mainly from industry.

4.1.4 Address of the Project Website

Not applicable.