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PROJECT FINAL REPORT

Grant Agreement number: 285275

Project acronym: GRAFOL

Project title: GRAPHENE CHEMICAL VAPOUR DEPOSITION: ROLL TO ROLL TECHNOLOGY

Funding Scheme: FP7-2011-NMP-ICT-FoF

Date of latest version of Annex I against which the assessment will be made:

Final report: **1st ☐ 2nd ☐ 3rd ☐ X 4th ☐**

Final covered: **from 1 Oct 2011 to 30 Sept 2015**

Name, title and organisation of the scientific representative of the project's coordinator[1]:

Prof John Robertson,

Engineering Dept, Cambridge University, Cambridge CB2 1PZ, UK

Tel: 44 1223 748331

Fax: 44 1223 748348

E-mail: jr@eng.cam.ac.uk

Project website[2] address: Grafol.eu

[1] Usually the contact person of the coordinator as specified in Art. 8.1. of the Grant Agreement.

[2] The home page of the website should contain the generic European flag and the FP7 logo which are available in electronic format at the Europa website (logo of the European flag: http://europa.eu/abc/symbols/emblem/index_en.htm logo of the 7th FP: http://ec.europa.eu/research/fp7/index_en.cfm?pg=logos). The area of activity of the project should also be mentioned.

Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project (tick as appropriate) [3]:

  X has fully achieved its objectives and technical goals for the period;

  ☐ has achieved most of its objectives and technical goals for the period with relatively minor deviations.

  ☐ has failed to achieve critical objectives and/or is not at all on schedule.

- The public website, if applicable

  X is up to date

  ☐ is not up to date

- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project (section 3.4) and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 3.2.3 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of scientific representative of the Coordinator: .....John Robertson.....

Date: .....7..../ ..10...../ . 2015.....

For most of the projects, the signature of this declaration could be done directly via the IT reporting tool through an adapted IT mechanism and in that case, no signed paper form needs to be sent

[3] If either of these boxes below is ticked, the report should reflect these and any remedial actions taken.

4.1 Final Publishable Summary Report

Executive Summary

The unique properties of graphene have led to much research work in this area. However, its take up by industry for commercial products is being limited by high production costs. There are two possible low cost means of production, liquid exfoliation and chemical vapour deposition (CVD). CVD is generally aimed at high-quality electronic grade graphene, whereas liquid exfoliation is aimed at low mobility, low cost products.

In GRAFOL, we aimed to develop two large scale CVD production tools, a wafer scale tool, and a roll to roll (R2R) tool. The key goal here was reliable graphene production, and cost reduction. GRAFOL achieved its target on cost reduction for graphene CVD, by achieving a satisfactory throughput.

GRAFOL contains the full chain of partners, from tool manufacturers, to process developers, to graphene users. The process developers (UCAM, FHI, TCD, DTU, GRA) then developed optimised process conditions under etch to go the graphene samples, based both on optimisation, but also on a deeper fundamental understanding of the growth process based on in-situ photoemission and electron microscopy of the growing films.

Then other GRAFOL partners then developed applications for graphene in the electronic and photonic areas. A key point was that a number of partners (UCAM, TRT, GRA, DTU) possessed their own 4" wafer CVD tools for sample supply, while UCAM and TCD possess various quartz furnaces for sample supply. This diverse sample supply base meant that there was never any backlog of sample supply for the various application oriented partners.

For optoelectronics, Philips developed doped graphene films as transparent, conductive graphene films for electrodes in OLEDs (organic light emitting diodes) that could replace the standard electrode materials, ITO, and was flexible. AMO and TRT developed photonic devices. AMO developed photo-modulators and photodetectors based on graphene on a silicon photonic platform. TRT developed electro-absorption modulators working at up to 30GHz. TRT and CNRS also developed high frequency field effect transistors for RF an analogue applications. CNRS and TRT were able to use the low spin orbit coupling of graphene to build spintronics devices with high output signal at least one order of magnitude higher than the state of the art ($\Delta R > 10^4 \Omega$). In a separate section, CCS developed graphene as the active sensing layer for low power sensors of gases such as NOx based on a low power CMOS platform of micro-hotplates. EPFL developed graphene layers for RF NEMS, based on the high modulus to density ratio of graphene. The NEMS switch is based on a capacitive switch. Each of these applications was successful, and reached their specifications.

In the final application, there was a comprehensive development of the all-carbon interconnect technology for VLSI, based of graphene based horizontal interconnects, and carbon nanotube vertical interconnects (Vias), plus some flipped down CNT horizontal interconnects. This WP achieved CNT via resistances of 490 Ω for a 300 nm diameter via, equivalent to a via resistivity of 7 mΩ.cm. This resistivity is comparable to the international state of the art, set by IMEC, Fujitsu, Samsung and TU Delft. The work also achieved a world record CNT area density, as needed for achieving the low via resistivity.

Context and objectives

The Grafol project arose because graphene has a set of very unique and extreme properties, but its application is constrained by the costs of its production. CVD is generally regarded as the preferred production route in the long term, particularly for electronic applications, but it will required a considerable improvement in the detailed production path, in for example lowering the growth temperature and developing more industrially compatible growth and transfer processes.

The project itself aims to achieve some of these, and then to implement them for a range of electronic applications, within a consortium which contains the full value chain of manufacturing, from growth to devices.

Objectives

- To develop a low-cost roll-based CVD system of 300 mm strip-width for graphene on flexible foil.
- Develop process conditions for an existing wafer scale CVD deposition system used for carbon nanotubes for the low-cost growth of graphene (and few layer graphene) for various electronic applications
- Define CVD process specifications and develop recipes for few-layer graphene growth onto metal surfaces, in terms of temperature, gas content, pressure, and using alloying to control the number of graphene layers.
- To use in-situ diagnostics (X-ray photoemission spectroscopy and high resolution transmission electron microscopy) to define optimum process conditions for graphene CVD on metal surfaces
- To define process conditions to maximise the graphene grain size at over 50 μm.
- Develop the basic building blocks of an all-carbon 3D carbon interconnect technology (combining multi-level graphene horizontal lines with vertical CNT interconnects) for next generation nanoelectronics, on industrially relevant 200 mm compatible tools
- Develop spintronics devices with high output signal at least one order of magnitude higher than the state of the art ($\Delta R > 10^4 \Omega$).
- Develop high frequency optoelectronic devices: 40 GHz photoconductors/ photodetectors and 1 GHz bandwidth photo transistor operating at 40 GHz.
- Demonstration of photo-mixing generic function.
- Develop doped few-layer graphene as transparent electrodes for organic light emitting diodes (OLEDs), as a replacement for Indium Tin Oxide (ITO) layers, with sheet resistivity of under 5.10^{-4} ohm.cm.
- Develop graphene-based electro absorption modulator with modulation >5db working at frequencies > 40GHz.
- Integrate graphene based absorption modulator and photodetectors into a silicon photonic platform
- Develop horizontal RF NEMs switch based on graphene technology with C_{on}/C_{off} >100 in the frequency range 2-5 GHz.
- Develop graphene-based gas micro-sensors using a Silicon on Insulator CMOS platform with embedded membranes.

List of partners

Participant no.	Participant organization name	short name	Country
1 (Coordinator)	University of Cambridge	UCAM	UK
2	AIXTRON	AIX	D
3	Philips	PHIL	D
4	AMO	AMO	D
5	Thales RT	TRT	F
6	Intel Performance Learning Solutions	Intel	IRL
7	CEA	CEA	F
8	TU Denmark	DTU	DK
9	Fritz Haber Institut (Max Planck)	FHI	D
10	Ecole Polytechnique Federale Lauysanne	EPFL	CH
11	Cambridge CMOS sensors	CCS	UK
12	CNRS	CNRS	F
13	Graphenea	Gra	ES
14	Trinity College Dublin	TCD	IRL

Main Science and Technology results

WP1 Develop CVD tools (AIX, UCAM, TCD, GRA)

Objectives

- Develop a roll-based system for deposition of graphene onto foil, covering the design, engineering, control systems, evaluate maintenance, reliability, life cycle cost and lift off transfer to polymer foils or glass.
- Adapt an existing 300mm CVD system in order to deposit graphene onto silicon wafers, covering the design, engineering, control systems, evaluate maintenance, reliability and life cycle cost.

Deliverables

number	title	who	month	Done?
1.1	Prioritised list of process parameters	AIX	12	Y
1.2	Finalised specification and concept for roll-based growth system	AIX	18	Y
1.3	12" wafer-scale growth of graphene	AIX	24	Y
1.4	Customized new graphene growth recipe with Raman I(2D)/I(G)>2.	GRA	24	Y
1.5	Provided graphene samples to end users	GRA	36	Y
6.2	Lifetime costings for rolled based and wafer based growth systems (related)	AIX	36	Y
6.1	Construction of R2R machine	AIX	36	Y (m48)

Task 1.1 derived a list of process parameters based on user requirements for each application.

Task 1.3. This developed the 300 mm wafer-scale tool previously made to provide wafer scale carbon nanotubes (CNTs) to produce graphene under different process conditions. The tool is shown below.

Figure 1.1: Photo of the 300mm wafer scale graphene tool

Here, the CNTs were typically grown at 600 - 750C using very thin Fe or Al_2O_3 as catalyst. For graphene, special Cu on SiO_2 on Si wafers were specified, and obtained from a specialist supplier. The tool was modified for a high process temperature of up to 1050 C. An important feature of the design is a three-zone heater, which allows a highly uniform radial temperature distribution, with rotating wafer, all of which assures a good graphene sample uniformity in the resulting product. Various monitoring instruments are used, including three infra-red surface temperature monitors, to achieve +/- 1.5 C over the wafer. The whole reactor was also modelled in terms of its temperature response and thermal expansion effects.

Samples are loaded into the growth chamber, preheated from a wafer loader robot on the right through a load-lock. The samples are then further heated to reaction temperature. The wafers are subject to a pregrowth anneal step in hydrogen or diluted hydrogen to condition the Cu catalyst. Then a hydrocarbon growth gas is introduced for the growth step. After growth, the wafer is cooled down, then transferred to the wafer loader robot, at temperature, and further cooled down. This whole cycle in the growth/anneal chamber takes under 30 minutes in the fully developed system, allowing the high throughput to be achieved. The cool down time in the wafer handler is extra to this.

The resulting samples are characterised by Raman mapping at AIXTRON. Additional, detailed characterisations were carried out by other partners, For example, DTU developed a microwave mobility tester system.

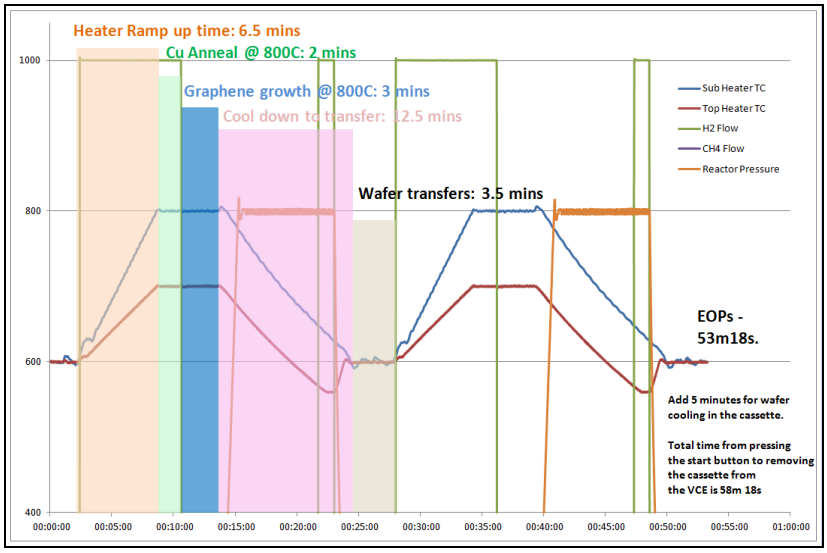


Figure 1.2: Timeline of the processing of two wafers per hour from ambient to delivery to the VCE Loadlock

Costings. The costings for graphene on wafers worked out similar to that of nanotubes on wafer, of order \$1 per in^2, based on this throughput.

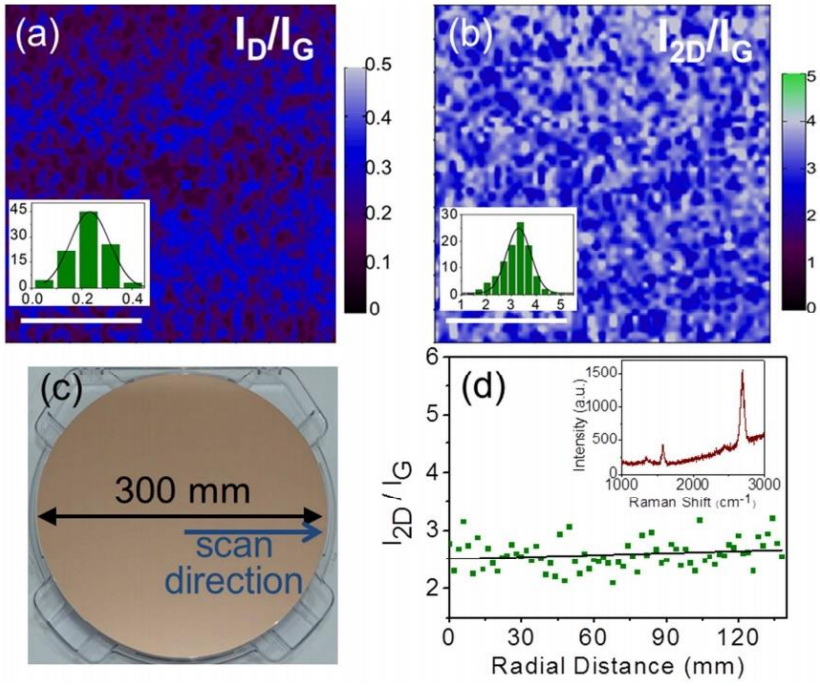


Figure 1.3: Raman spectroscopy over 300mm wafer to confirm monolayer graphene growth and uniformity

Task 1.2 was to develop the design concept for a R2R machine.

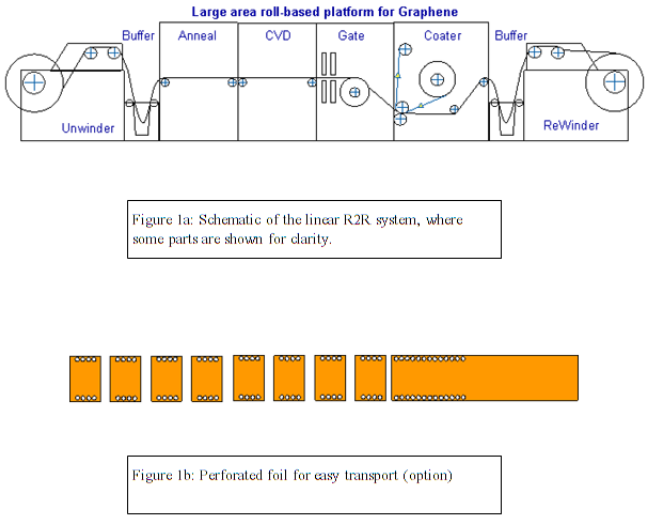


Fig. 1.4. Standard in-line R2R system concept.

Fig 4 above shows a traditional in-line R2R concept. This has some disadvanatages in terms of large footprint, large energy use, and difficulty of tensioning the Cu foil which is used. Cu is likely to be the preferred catalyst material for the CVD.
A number of unusual design concepts were developed and patented, including a 'barrel' chamber, as shown in fig 5, which aimed to reduce the footprint size, while cleverly tensioning the foil around the barrel shape.

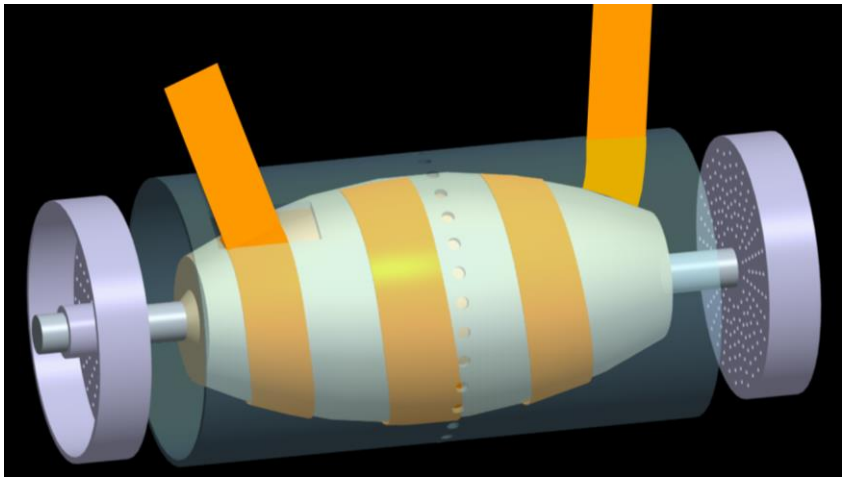


Figure 1.5: 3D barrel concept

Task 6.1 R2R construction.

There are four published R2R machine designs in the literature, an enclosed design from Sony, an infra-red heated foil design by Samsung Techwin, a high power microwave plasma design from AIST for lower temperature growth, and a bench top design from Michigan State University, Fig 6.

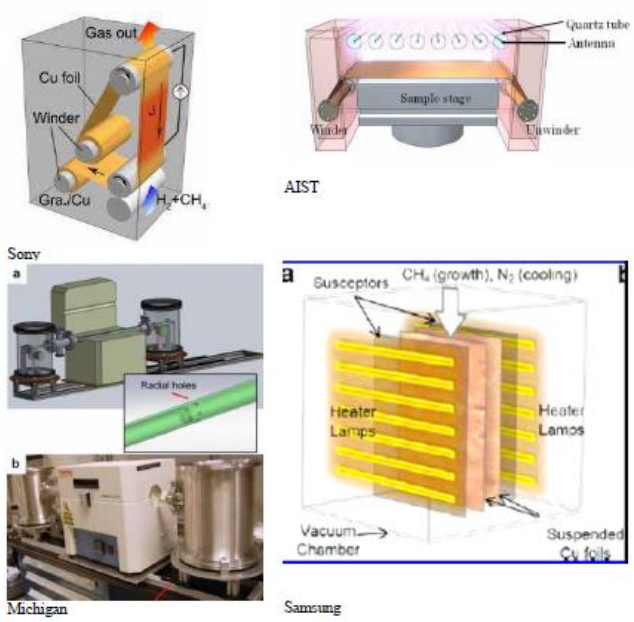


Fig. 1.6. Various R2R systems in the literature.

The final design that AIXTRON used is a return to the in-line R2R system of Fig .4, with atmospheric pressure processing, and a slowly moving foil. The foil transport mechanism is specially designed to carry the foil without ripping or stressing it.

The resulting system is shown in Fig 7. The specifications of the machine are as follows; stand-alone or inline integrated system, small footprint (4.5 m by 1.6 m), temperatures up to

1000C for CVD, 100 um thick Cu foil 300 mm wide, speeds up to 8 m/hr, and diverse gas supplies. The development of the operating conditions is described shortly.

Fig. 1.7. Black Magic 'Spider' R2R machine, after construction.

Task 1.4 Lift-off and Transfer of graphene films (TCD)

The graphene is grown on a metal foil, either Cu or Ni. After this, it must be transferred to another substrate such as SiO_2 on Si by a transfer process. This involves spinning-on a polymer (PMMA, or PDMS) film onto the top of the graphene film, dissolving the underlying catalyst layer by say $FeCl_3$ (in case of Cu) or ammonium persulfate, floating off the graphene, then catching it on the new substrate. Transfer is one of the rate limiting steps in graphene CVD production. It also tends to leave a polymer residual on the graphene which is not easily removed. In the case of a Si system, the polymer could be removed by a O_2 plasma, but in the case of graphene, this would etch off the graphene as well. TCD has optimized a Lift-off process via modification of a Polymer Assisted Transfer process (PAT). TCD developed several alternative transfer polymers such as cellulose polymer. This resulted in lower residuals. Fig. 8 shows the schematic and the test platform.

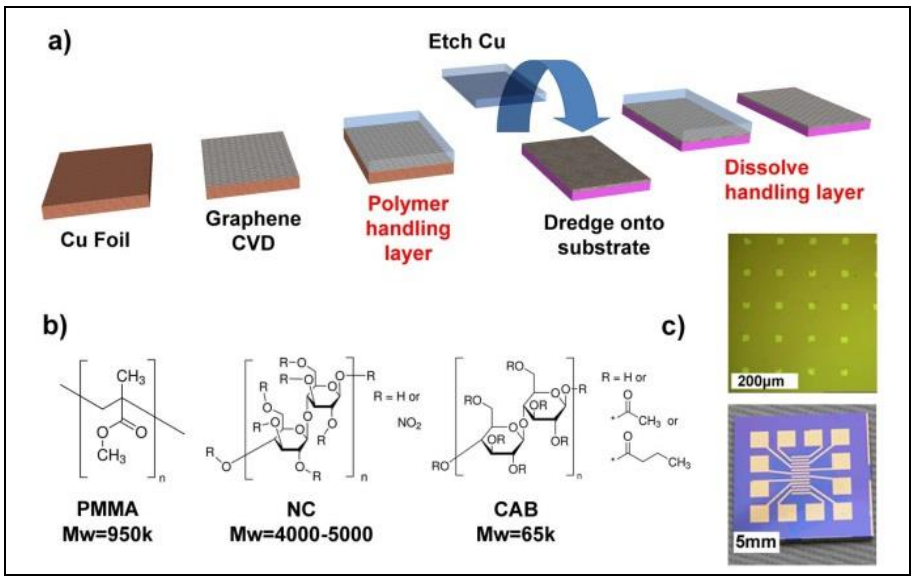


Figure 1.8: a) Process flow for graphene PAT b) Repeat units of polymers investigated c) Device platform for comparison of electrical performance of graphene after PAT

WP2 Process Development

T2.1. Fundamental Unerstanding (FHI, UCAM, DTU)

The standard model of graphene CVD using Cu or Ni as catalysts proposed that, after dissociation of the hydrocarbon moledcule on the metal surface, that in the case of Ni, C atoms diffuse into the surface, and then they precipitate out on the surface when the Ni is cooled down. In contrast, on Cu it is purely a surface process, so that the Cu produces monolayer graphene whereas Ni produces varied thicklnesses.

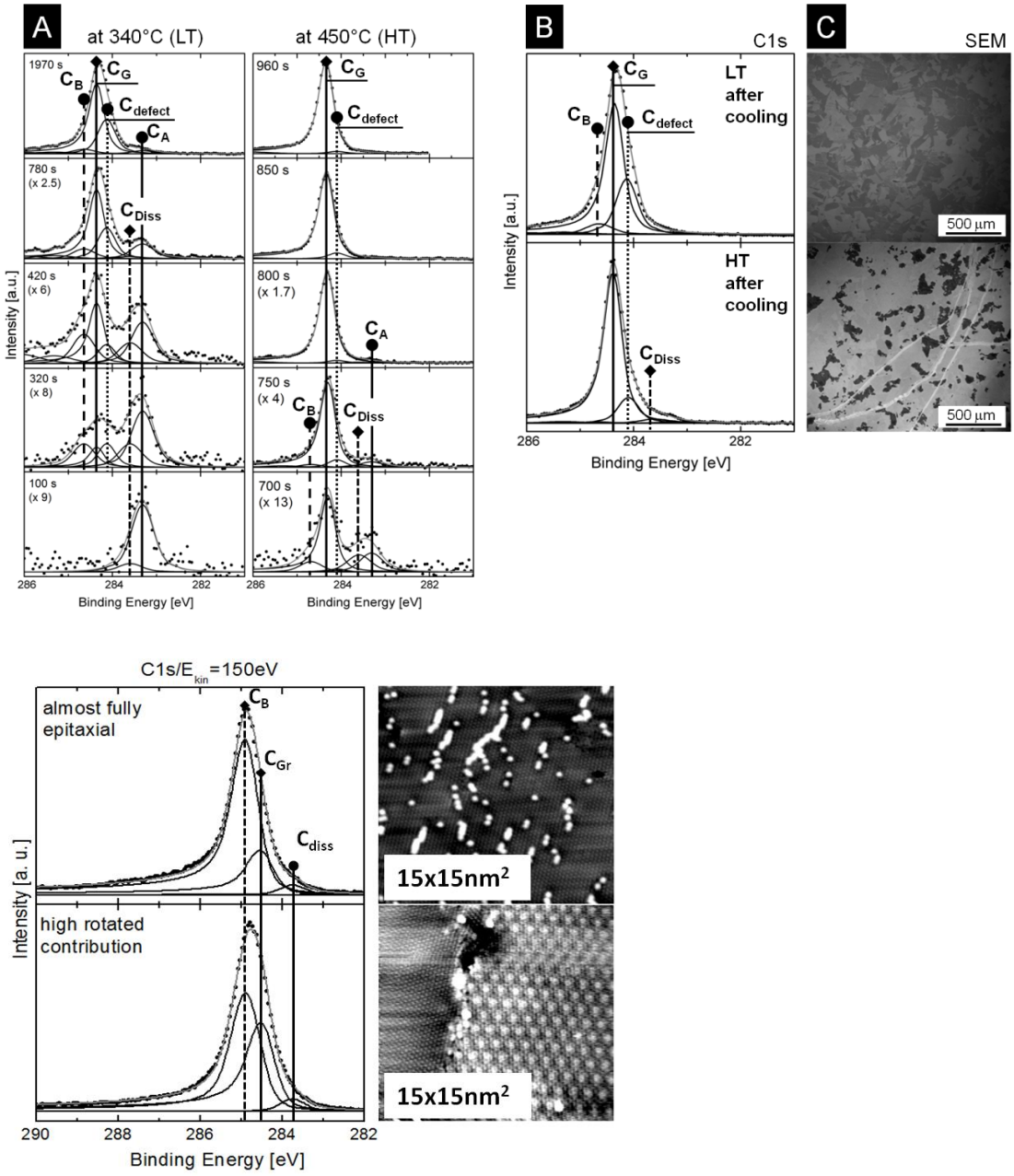


Fig 2.1. C 1s core level assignments

A systematic study of the reaction of methane on Ni or Cu by in-situ XPS was carried out by FHI. A key part was to obtain the correct assignment of the various components of the C 1s core level spectra in fig 1, particularly that due to subsurface bonded C, and of the Ni or Cu

core level spectra. It was confirmed that Cu is indeed a surface process, because the C solubility in Cu is only 0.03% at 1000C.

But the process on Ni is different. It is mostly isothermal. C atoms are released at the surface. At this stage, the C can diffuse into the Ni interior, controlled by its diffusion coefficient and the overall thickness of the Ni film acting as a reservoir, Fig 2(a). The C that does not go in, precipiates on the surface as graphene, at the growth time. Additional C can precipitate on cool down, but this depends on the diffusion coefficient, at that temperature. Thus, with Ni, the key paramerters are the foil (reservoir) thickness, and the reaction temperture.

T2.2 Growth on Ni (UCAM)

With this understanding, it is possible to design the use of Ni as a catalyst, for arbitrary numbers of layers, and reduced grwoth temperature. First a dilute alloy of Ni with Au is made. The role of Au is to saturate nucleation sites on the Ni surface, Fig 2(b). Grain size is inversrely proportional to nulceation density, so that it is useful to saturate nucleation sites, to increase the grain sizes.

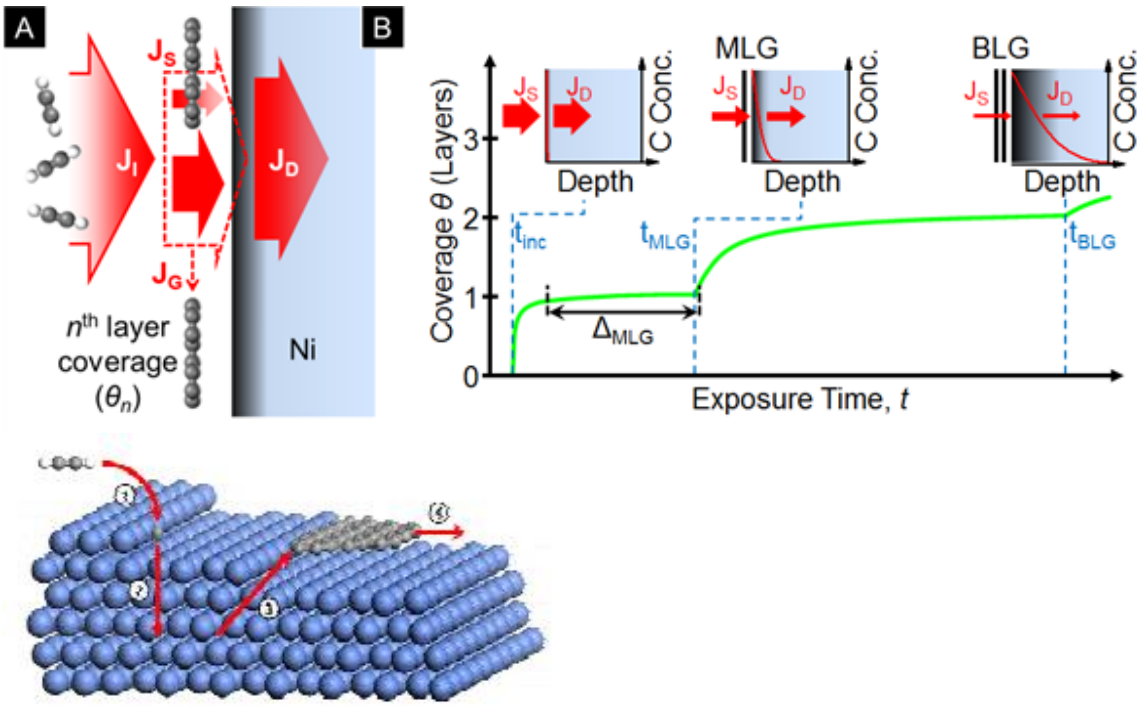


Fig. 2.2. (a) Generalised model for graphene growth on Ni. (b) Role of Au in saturating surface nucleation sites.

T2.3 Growth on Cu, large grain sizes

A reasonable quality graphene with grain sizes above 100 um was achieved by suitable annaling of the Cu foil, keeping the growth temperature low and dilution with H2.

T2.4 Solid state converison process

It was realised by others that graphene could be prepared by an all-solid state process, by the diffusion of C atoms through a Ni catalyst to emerge as graphene. Tetrahedral amorphous

carbon (ta-C) is a useful source of carbon, because it has a high free energy (less stable). Although previous groups claimed the process resulted in good samples, we did not verify this, but to diffusion of C along the grain boundaries of the Ni. Thus, we introduced a Al2O3 diffusion barrier layer to homogenise the diffusion rates across the sample (Fig 3). This resulted in good graphene, at 450C.

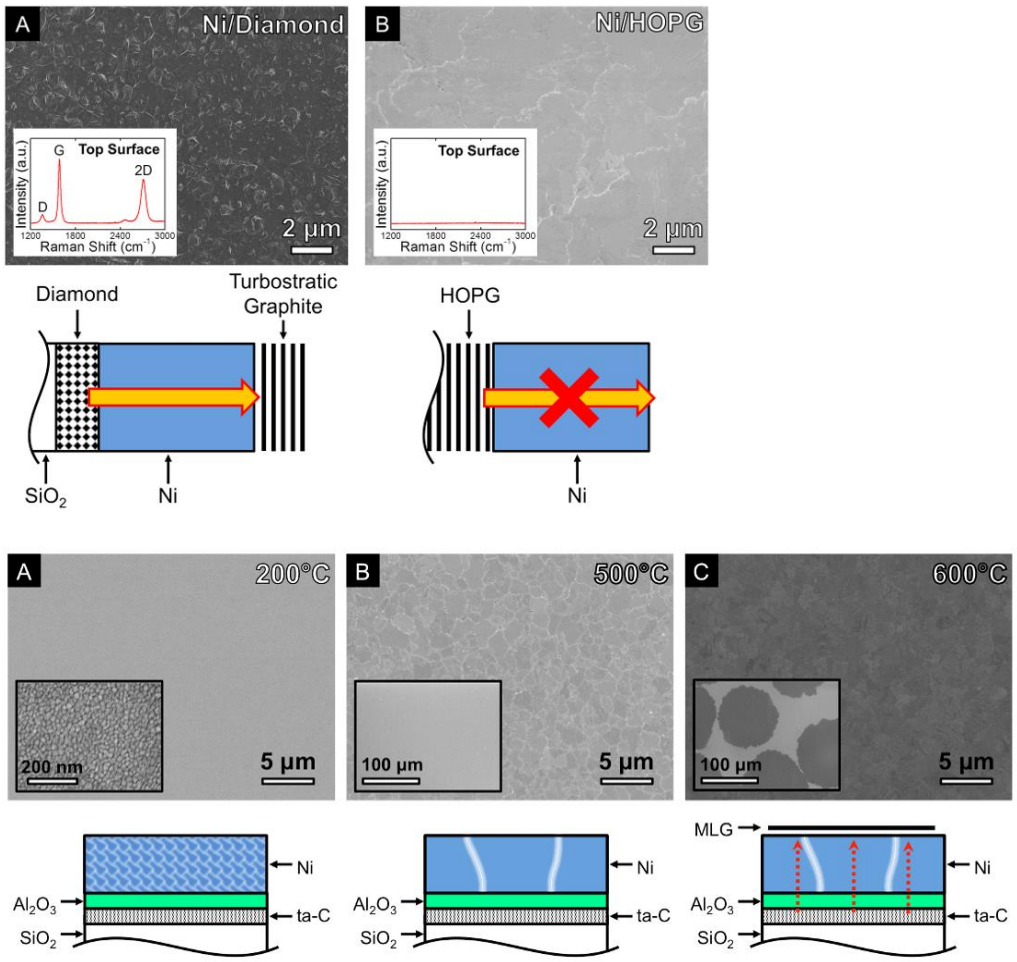


Fig. 2.3. Need to cut out short circuit diffusion paths. (b) illustration of samples, and schematic of use of diffusion barriers.

T2.5 Lower Temperature Growth on Cu

While Cu is advantageous for producing monolayer graphene without complications, the evaporation of Cu at high temperatures is inconvenient when CVD is operated at a low pressure. The alternative is to use a high pressure, which suppresses the evaporation. The other way is to redeuce the growth temperature. This can be achieved without compromising the graphene quality by changing the precursor gas from methane to a complex hydrocarbon like ethene, benzene or xylene. Benzene is not allowed in most labs because it is carceneogenic, so ethene or xylene are prefered choices. It is possible to reduce the growth temperature from 1000C to 850C using this method, based on the Raman spectra.

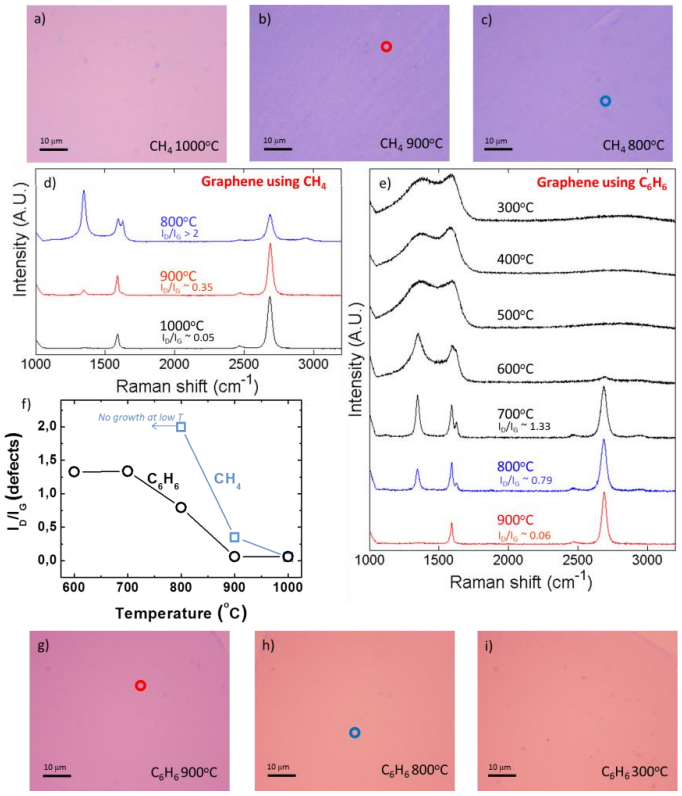


Fig 2.4. Reduced temperature growth of graphene on Cu, by using different precursor gases.

Task 2.6. Optimum process parameters for atmospheric pressure R2R growth

AIXTRON decided to use an atmospheric pressure, in-line R2R scheme, as shown in Fig. 1.1. This uses atmospheric pressure conditions, and a gas blanket to separate the air from the growth or annealing gas ambient. This requires the development of intrinsically safe growth conditions, by diluting hydrogen annealant and methasne below their respective uper flammability limits (4% for both). Thus hydrogen is diluted to 2% by nitrogen as in forming gas. AIXTRON constructed an atmospheric pressure test rig with multiple gas sensors which was then operated in the UCAMcleanroom.

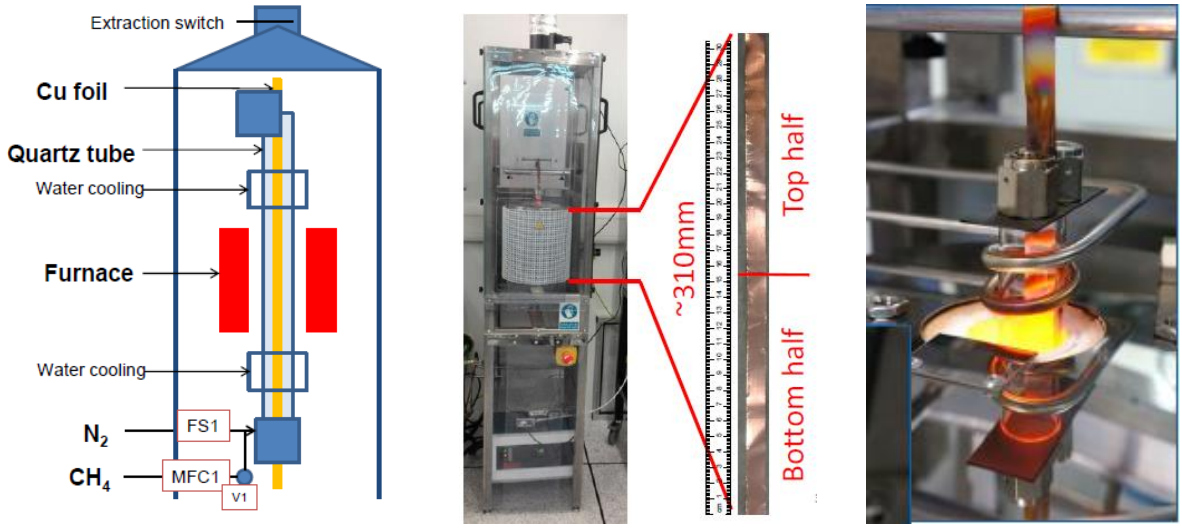


Fig 2.5. Concept of the test rig, overall image, and close up of heated and cooled sections under operation.

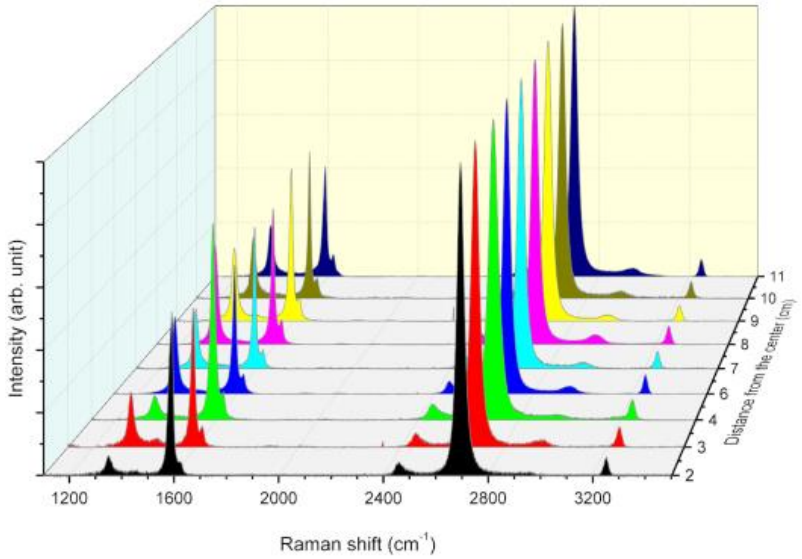


Fig 2.6. Raman spectrum of monolayer graphene under R2R conditions, scanned across the sample.

The foils are fed in through slits, drawn vertically downwards through the reaction chamber, and out of a lower slit, onto a receiving roller. The optimisation requires control of slit width, so that oxygen ingress does not etch the growing graphene, and control of the gas mixture to anneal the Cu foil, and give good growth. A Raman spectrum of the resulting graphene films is shown above in fig 2.6.

WP3 Opto-electronic devices (PHIL, AMO, Thales, CNRS, DTU)

Objectives

- Develop doped few-layer graphene as transparent electrode for organic LED (OLED)
- Develop few layer graphene for transparent electrodes for GaN LEDs
- Realize graphene based electro-absorption modulators.
- Integrate graphene based modulators and photo-detector in silicon photonic platform.
- Fabrication of a hybrid silicon / graphene photonic devices.
- Demonstrate spintronics devices with high output signal at least 1 order of magnitude higher than state of art ($\Delta R > 10^4 \Omega$)
- > 40 GHz photoconductors/detectors
- 40 GHz photo-mixing demonstration and "plasma wave" like operation

Deliverables

	title	who	month	Done?
3.1	Evaporated small molecule white OLED	Phil	24	Y
3.2	Report, Comparison: Graphene – state of the art TCOs for OLEDs	Phil	48	Y
3.3	Report, Comparison: Graphene – state of the art TCOs for GaN LEDs	Phil	44	Y
3.4	Realize a graphene based electro-absorption modulator with a modulation	AMO	24	Y
3.5	Comparison of electro-absorption modulation in CVD grown and exfoliated graphene	AMO	30	Y
3.6	Report on silicon photonic chip with graphene-based modulator working at frequencies > 40 GHz	AMO	48	Y
3.7	Fabrication of single gate and dual gate graphene transistors	TRT	18	Y
3.8	Determination of physical parameters of Aixtron CVD graphene devices based on device performances	TRT	24	Y
3.9	Fabrication of spintronics devices based on Aixtron graphene	CNRS	24	Y
3.10	Fabrication of 40GHz photoconductor /detector devices based on Aixtron graphene	TRT	24	Y
3.11	Demonstration of high output signal ($\Delta R > 10^4 \Omega$) in spintronics devices	CNRS	36	Y
6.3	Demonstrate 1GHz bandwidth phototransistors operating at 40 GHz	TRT	36	Y
6.4	Report on performances of spintronics devices and high frequency opto-electronic devices based on Aixtron graphene	CNRS	48	Y
3.14	Sub 25 nm periodic lattice defined in graphene, structural and electrical characterisation	DTU	18	Y
3.15	Nanopatterned graphene transistor, feature size 10 nm	DTU	36	Y

Task 3.1 Graphene for OLEDs (Philips)

The replacement of ITO electrodes by flexible graphene electrodes is one of the most discussed applications of graphene. Few layer graphene can be transparent, but it must be doped to achieve an adequate conductivity, due to its low carrier density, if it is to approach the performance figures of ITO. Doping of graphene is not achieved by substitutional doping or by molecules, it is achieved by transfer doping by high or low work function layers. This technology is transferred from OLED experience. Here we use evaporated MoO_3, with a function of 6.6 eV. MoO_3 is transparent, and environmentally stable, as well as having this high work function. Its high work function also provides an excellent hole injection layer into

the organic light emitter layer. The OLED device structure is shown in Fig 3.1(a). The energy alignment from XPS is shown in Fig 3.1(b).

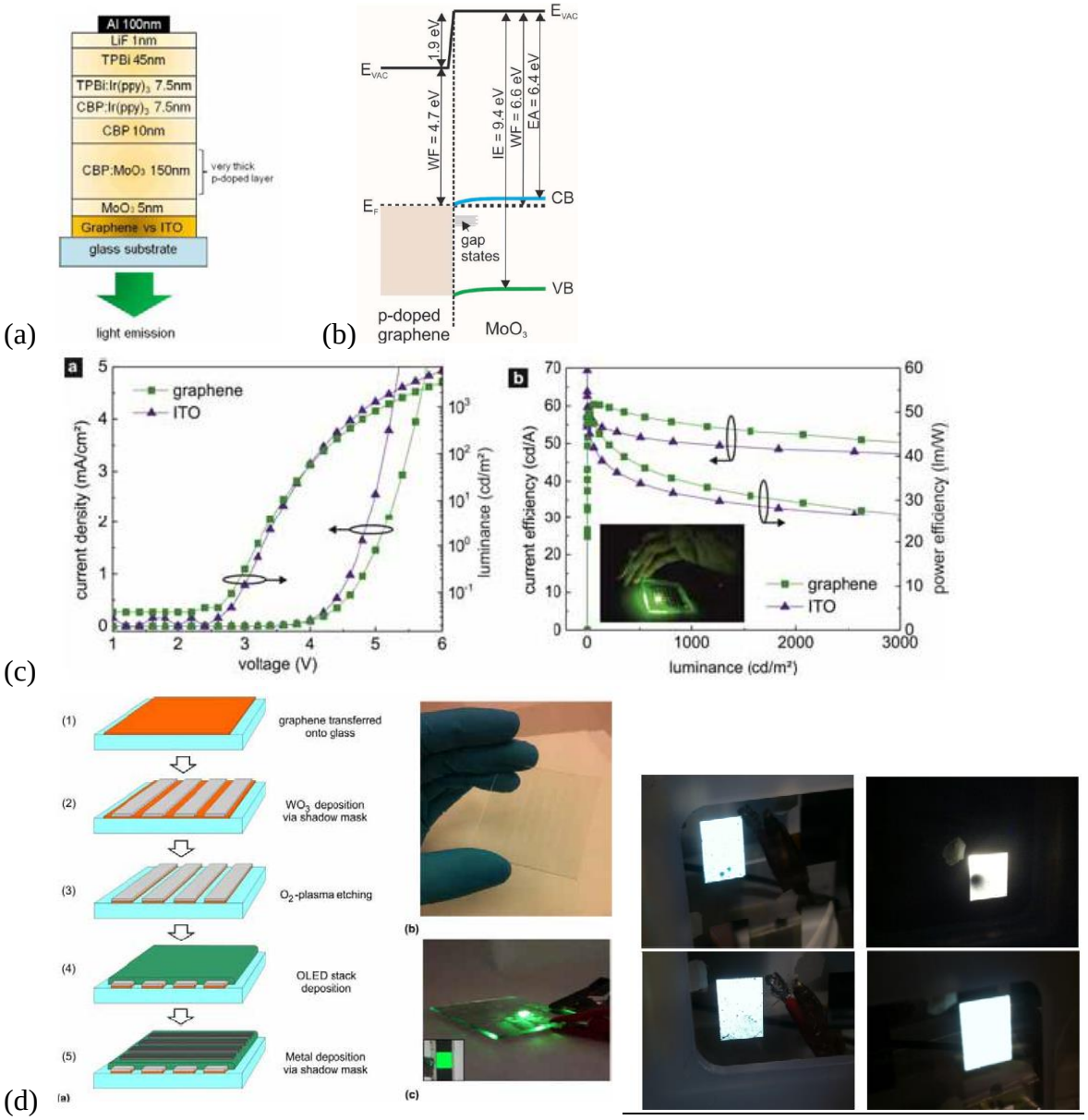


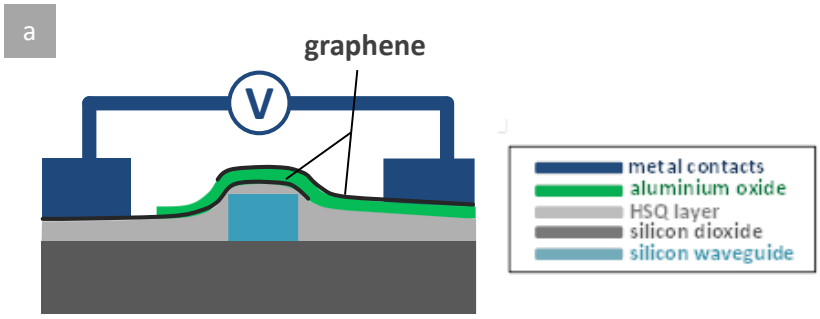
Fig 3.1(a). OLED structure, (b) band line-ups in device, (c) Current density, luminance vs applied voltage. (c) process steps and resulting devices.

Fig 3.1 (c) compares the operating current density vs applied voltage for ITO and the doped graphene devices. It is seen that the graphene device has comparable optical and electrical performance to the ITO device because the graphene is not thick but conductive enough. Fig 3.1(c) shows that green emitting devices result. Larger, white emitting devices were also constructed. The results show that graphene based OLEDs can perform as well as conventional OLEDS. However, the devices would need to be encapsulated and their lifetimes to be tested. Also, costs should be comparable to devices using ITO to be useful.

Graphene was also compare for inorganic (GaN) LEDs. In this case, the graphene could be a useful heat spreader layer. However, it was found that graphene gave no useful performance advantage.

Tasks 3.5 and 3.6, Optical modulators (AMO).

Graphene could make an interesting photo-modulator because of its unique linear-dispersion band structure, whiuch means the same device could operate at a range of frequencies. First though, graphene must be transferd to a Si optical platform to make the device. Fig 3.2 shows the device layout, while Table 3.1 compares the performance of different modulator designs.



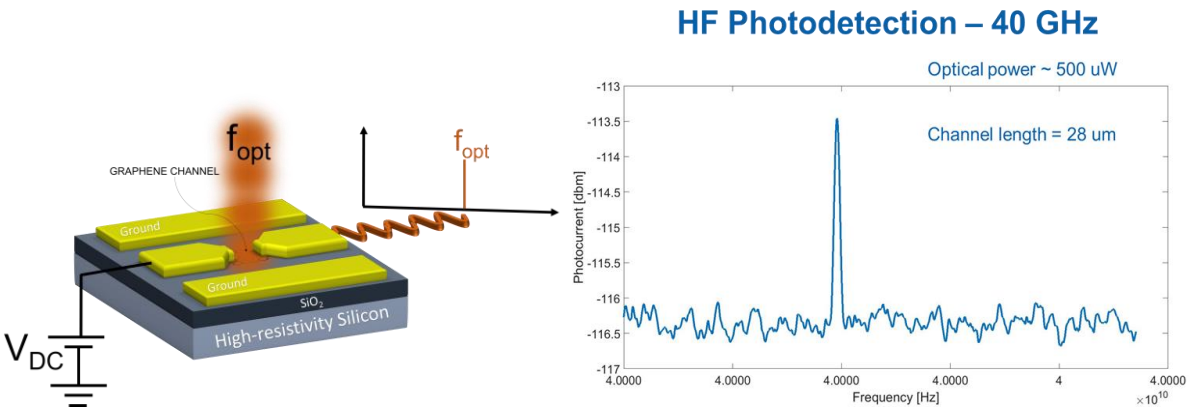
Value	Graphene actual	Graphene expected 2015	GeSi absorption modulator	Si Mach-Zehnder Modulator
Modulation depth (Mod)	16 dB	16 dB	6 dB	5.5 dB
Insertion loss on chip (IL)	3.3 dB	3.3 dB	5 dB	4.2 dB
Ratio Mod/IL	5	5	1.2	1.3
-3dB bandwidth	3.4 GHz	25..50 GHz	40 GHz	26.5 V
Max data rate	6 GBit/S	50 GBit/s	---	50 GBit/s
Drive voltage	7 V	7 V	1.9 V	7 V

Table 3.6.1 : Key parameters for the graphene based electro-absoprtion modulator developed in Grafol compared to competing technologies. Data for GeSi are from D. Feng et al. Optics Express. 20, 2224 (2013), data for Si MZI are from X. Tu et al. Optics Express 21, 12776 (2013).

As can be seen the modulator already now outperforms all competing technologies in the static parameters. The static transmission of the modulator shows a modulation depth of 28 dB for a 400 µm long modulator. The on-chip insertion loss of the modulator is estimated to be ~5 dB. For the maximum speed, the main limitation are still parasitic resistances and capacitance. Therefore graphene can be considered at the moment as the most promising approach to realize an absorption modulator on silicon waveguides.

Tasks 3.10 and 6.3, Thales

Thales achieved photodetection devices that operated at 40 GHz.



Tasks 3.7 (CNRS)

Graphene has particular advantages in spintronics. Graphene has a long spin coherence length for injected electrons or holes, because carbon has small spin-orbit coupling due to its low atomic number. This allows for the fabrication of magneto-resistive devices with a large magneto-resistance. Eventually, it was possible to fabricate a device with a 10% magneto-resistance. Generally, it is necessary to inject carriers from a high impedance into the graphene transport layer, in order to develop a large magneto-resistance. Typically this is done by using an Al2O3 tunnel barrier injection layer. In the case of graphene, this is non-trivial. An ultra-thin (1 nm), pin hole free layer of Al2O3 must be grown on graphene. Generally, it is very difficult to grow any oxide layer on graphene because of its low surface energy. Often, an initiation layer is used to increase the nucleation density of the Al2O3. Sputtered layers have been used. Eventually, we succeeded in growth 1 nm thick Al2O3 by atomic layer deposition (ALD), which was pin-hole free and a functioning tunnel barrier. This gave the 10% resistance ratio shown in fig 3.4.

It was also discovered that graphene films could give an excellent corrosion barrier over Co or Ni, which would be an extremely useful practical gain from us of graphene films in these devices.

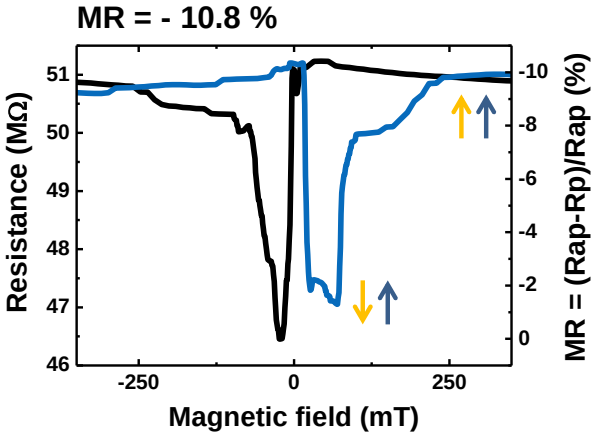


Fig 3.4. Measured spin signal for a graphene-passivated nickel electrode contacted by a Al_2O_3/Co spin analyser

WP4 Carbon Interconnects (UCAM, CEA, Intel)

Objectives

The objective of WP4 is to develop the basic building blocks of 3D carbon interconnects combining graphene horizontal lines with vertical CNT interconnects on industrial relevant 200 mm compatible tools.

The specific objectives of WP4 are:

- Demonstrate CVD graphene lines technology
- Demonstrate growth of localized dense bundles of CNTs on graphene
- Develop the best contact structures between graphene horizontal graphene lines and vertical CNT growth
- Develop a low temperature graphene manufacturing process

	title	who	month	Done?
4.1	High density process 10^{13} cm^{-2} CNT in via with SOA electrical contact. Electrical test with metal top contact for perpendicular contact technology	CEA	18	Y
4.2	Feasibility of CNT forest growth on graphene	CEA	18	Y
4.3	Theoretical comparison with different situation of C-C contact	UCAM	24	Y
4.4	Comparison of electrical data for different contact configuration with additional graphene layer	Intel	36	Y
4.5	Low temperature process for CNT growth and graphene at 400°C	UCAM	36	Y
6.5	Final best high density >10^{13} cm^{-2} CNT in via with State of Art contacts	CEA	48	Y

The continued scaling of CMOS devices means that the current density carried by Cu based interconnects will soon exceed the maximum that Cu can carry (10^6 A/cm^2). The only material able to carry higher current densities is carbon, in the form of carbon nanotubes (CNT) or graphene (~10^9 A/cm^2) due to its strong covalent bonds. However, serious material integration issues must be solved to allow either of these materials into CMOS. Electrically, very high area densities of CNTs are needed to reduce the electrical resistivity of the overall via (vertical interconnect). For a fully carbon system, as shown schematically in Fig. 4.1(a), there is the problem of nucleating CNT growth on the low surface energy graphene.

CNT growth and doping (UCAM)

A design of the catalyst /support layer combination using ultra-thin Fe on plasma treated Al_2O_3 allowed the highest areal density of CNTs at 2x10^{13} cm^{-2} to be produced by UCAM, a world record. The CNTs were separated by only 2 nm between centres. This density is a factor of 1000 higher than achieved previously. However, Al_2O_3 is an insulating suport layer and ultimately cannot be used as a support. Growing high density CNT forests or bundles on a metal layer is more difficult, because the high surface energy of the metal inhibits the de-wetting of the catalyst into nanoparticles. After previous work by UCAM on $CoSi_2$ and TiN metallic support layers improved the situation slightly, the ideal metallic support layer was discovered to be amorphous TiSiN. This is a strong diffusion barrier with no grain boundaries, a low surface energy, and is unreactive towards C or O. UCAM was able to make CNTs with an areal density of 5x10^{12} cm^{-2} on TiSiN. The areal densities are summarised in Fig 4.1(b).

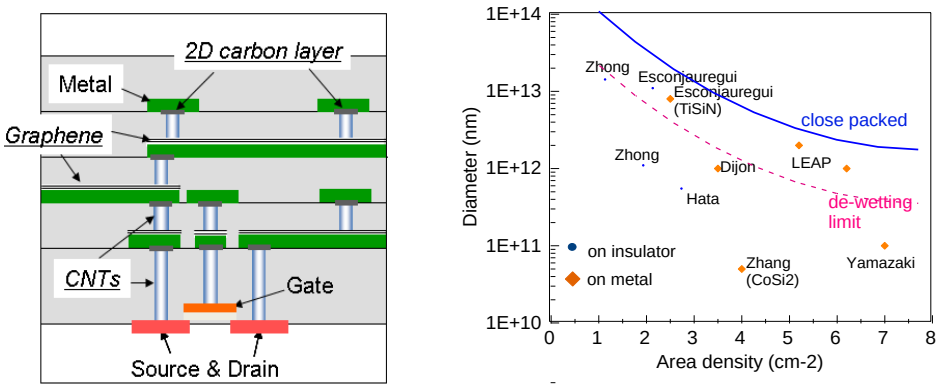


Fig 4.l. (a) Schematic of Carbon Interconnects, (b)Area density vs CNT diameter for forests.

A second factor for CNT vias is maximising the fraction of metallic tubes. There are various means of designing a catalyst or process to maximise the fraction of *semiconducting* tubes, but there few equivalent processes to maximise *metallic* tubes, except a difficult design of the catalyst. However, this would interfere with the maximisation of areal density. Therefore, we chose instead to dope the whole CNT forrest, and so turn all tubes into metallic. This is achieved by transfer doping using MoO_3, as used for graphene in OLEDs. This has allowed a 200 fold increase in the forrest's electrical conductivity.

Process Integration and Electrical Measurements (CEA/Intel); extension of D6.5.

The overall process flow to make the vias is shown in Fig 4.2(a). In a previous EC/FET project on interconnects (Viacarbon), also involving UCAM, CEA and Intel, the integration failed at the last stage, with a high overall resistivity between the top and bottom contacts.

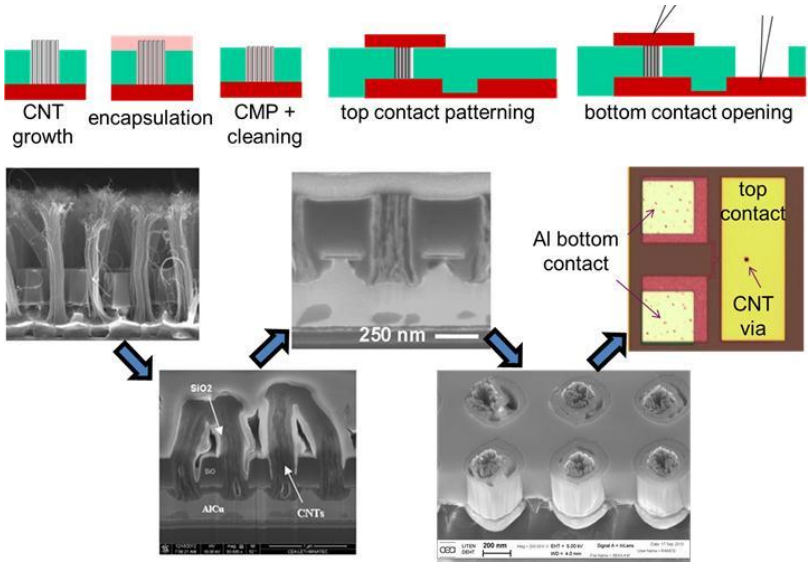


Fig. 4.2. Process flow.

There were three possible reasons for the problem; oxidation of the bottom contact which contained Al, poor wetting of the top contact to the CNTs, or pull out of the CNTs during the Chemical Mechanical Polishing (CMP) step. CEA used the flip down technique to lie down CNT bundles horizontally, added some on-top electrodes to this and measured the resistance. This showed that the top or bottom contact was not a problem; it was the CMP step.

At step 3 in Fig. 4.2, the CNTs are anchored into the via holes prior to CMP by an encapsulation layer, of which SiN_x, SiO_2 (from TEOS) or various polymers were tried. Eventually, a short chain polyethylene $(CH_2)_n$ was found to be a good encapsulation layer. The electrical properties of the resulting vias were measured by Intel, and were found to have a good cumulative resistance distribution (Fig 4.3). Fig 4.3(b) shows a FIB-SEM cross-sectional image.

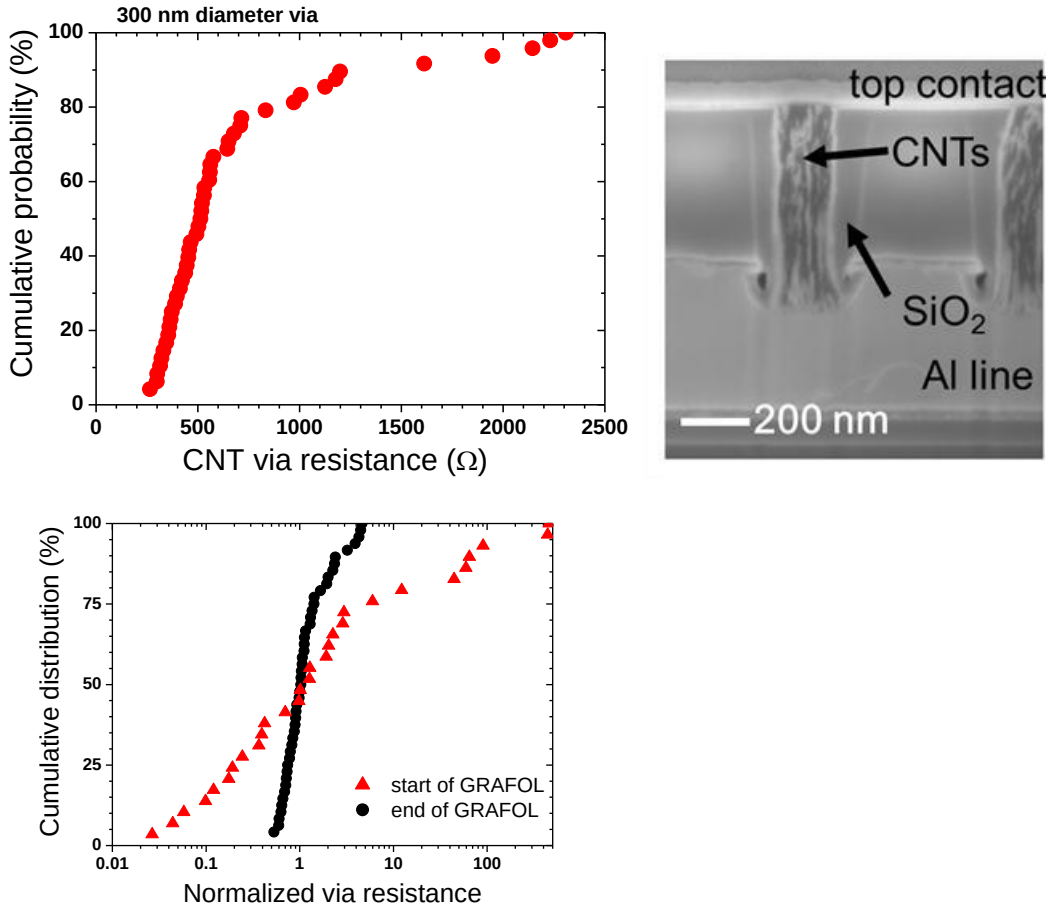


Figure 4.3. (left) cumulative probability distribution of 300 nm diameter CNT via resistance with Pd top contact; (right) FIB-SEM cross section of a CNT via. (bottom)improvement through project.

The best electrical results were obtained with a Pd top contact patterned by lift-off and the cumulative distribution of 300 nm diameter via resistances measured by a 2-point-probe configuration is plotted in Figure 4.3(left). It shows the median CNT via resistance is ~490 Ω, which corresponds to an equivalent via resistivity ~7 mΩ.cm (including contacts and "empty" space in the via). This is comparable to the international state-of-the-art. Since the resistivity of the *same* CNTs alone is ~1 mΩ.cm (Fig. 4.4), and since we checked that encapsulation does not degrade this resistivity (see M36 report), one can thus conclude that:

- contacts are the main contributor to the measured via resistance, although the estimated median value of the CNT/metal specific contact resistance is rather low, i.e. ~10^{-7} Ω.cm^2 ;
- the *dispersion* of resistance in Fig. 4.3(a) originates mostly from the *bottom* contact (low dispersion on the resistance of CNT bundles alone and the CNT/Pd contact resistance.

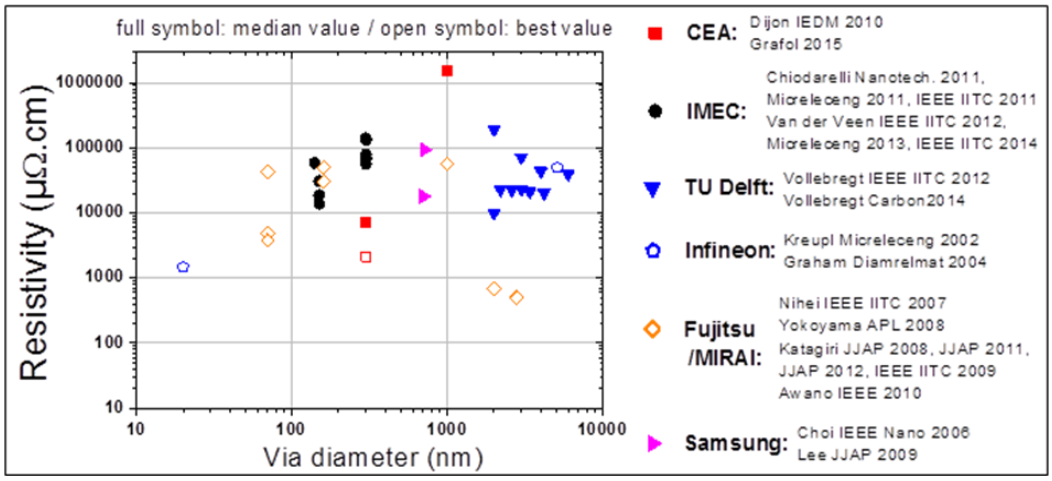


Fig. 4.4 comparison with other groups.

The comparison with other international groups in Fig. 4.4 above is impressive. The Fujitsu work was the leading work for many years. The most recent work is by IMEC reported in the IITC conferences. The original 'Viacarbon' CEA value is the red square at the top The 'Grafol' CEA values are at 1000-10,000 μΩ.cm, in red; filled symbol = median, open square = best value. These Grafol values are below all others except the Fujitsu values (open diamonds), but there a possibility exists that the encapsulant did not complete fill the via, so the top contact metal shorted the via.

Graphene Aspects

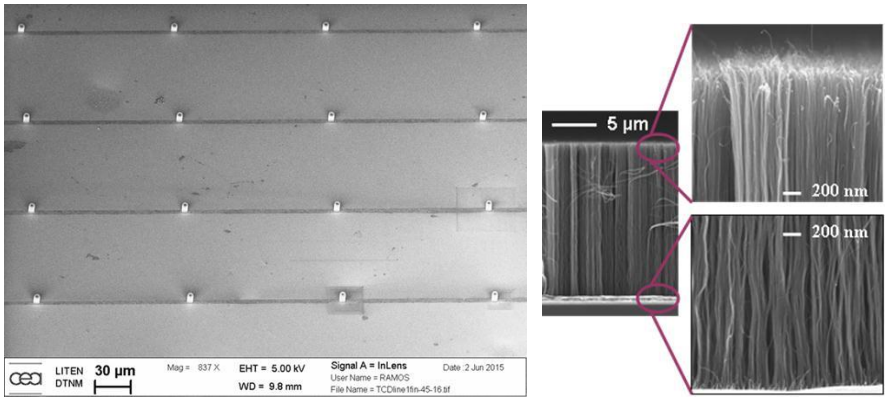


Fig. 4.5. Patterned growth of CNT forests on graphene lines.

Graphene lines for use as horizontal interconnects were supplied from WP2. CEA developed two processes to grow CNTs onto graphene surfaces, to complete fully carbon interconnects. The problem is the low nucleation density due to the low surface energy of graphene. The preferred process involves depositing a thin Ti layer onto the graphene, onto which catalyst layers can be deposited, and then carrying out the growth. A CNT density of $5x10^{12}$ cm^{-2} was achieved, with specific contact resistance of under 10^{-5} ohm.cm^2 between the graphene and a top Pd contact.

WP5 RF MEMS and Sensors (CCS, EPFL)

Objectives. NEMs:

- To fabricate NEM capacitive switch with C_{on}/C_{off} >100 in frequency range 2-5 GHz based on MWNT technology
- Design and fabrication of electrostatically actuated RF NEM switches with specifications for reconfigurable interconnects and power supply gating switch
- Develop electromechanical and HF analytical and lump (circuit model) for RF NEM switches: capacitive and in-series power supply gating switch
- Comparison and benchmarking of key figures of merit of CNT NEM switches against state-of-the art membrane MEMS switches

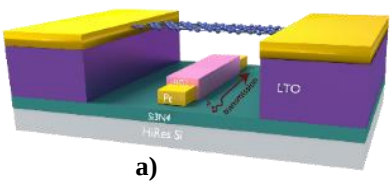
Sensors

- To grow/deposit graphene on CMOS micro-hotplates
- To develop and characterize low power CMOS based gas sensors based on graphene

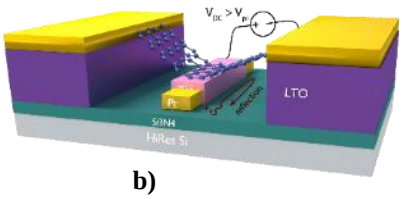
	title	**Who**	**month**	**Done?**
5.1	Specifications and design of horizontal nanotube mat arrays for a NEM device	**EPFL**	**6**	**Y**
5.2	1st fabrication run for multi-layer graphene NEM switches	**EPFL**	**18**	**Y**
5.3	2nd fabrication run for optimised multi-layer graphene NEM switches (operating at f>2GHz and contact resistance <0.1 Ohm	**EPFL**	**36**	**Y**
5.4	DC and HF models for optimised multi-layer graphene RF NEM switches	**EPFL**	**42**	**Y**
5.5	Demonstration of deposition of graphene on CMOS micro-hotplates	**CCS**	**12**	**Y**
5.6	Design and simulation of micro-hotplates with pulsed power consumption of 0.1mW per unit for 200 °C and thermal time constants below 30ms	**CCS**	**18**	**Y**
6.6	Fabrication, characterization and reliability tests of micro-hot plate chips and CMOS drive	**CCS**	**36**	**Y**

NEMS

The high modulus/weight ratio and good conductivity make graphene a favoured candidate for use in RF MEMs switches. Fig 5.1 shows the switch in the on and off (up and down) conditions. It operates as a shunt capacitive switch, with input shorted to ground in the off state (b). Table 1 is a Comparison of technologies for RF capacitive switches.



a)



b)

	PIN diodes	RF MEMS	Graphene NEMS (SLG) [1]	Graphene NEMS (MLG) [1]	Graphene NEMS (meas. flakes)	Graphene NEMS (meas. CVD)
Actuation voltage	3-5 V	10-100 V	0.3 V	1.4 V	<3 V	< 5 V
Capacitance Ratio	~ 10	40-500	269.2	282.6	**50**	**79**
Capacitance	OFF: 40-80 fF	UP:1-10 fF	16 fF	16 fF	50 fF	10 fF
Resistance	ON:2-4 Ω	DOWN: 0.5-2 Ω	8.57 Ω	2.16 Ω	300 Ω	70 Ω
Switching time	1-100 ns	1-300 µs	0.43 µs	0.24 µs	<1 µs	<1 µs

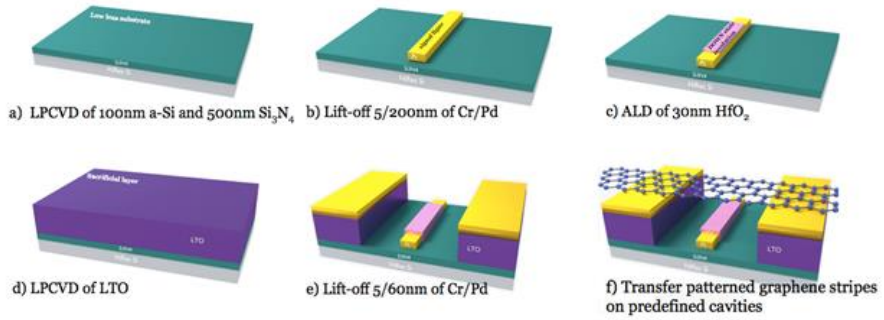
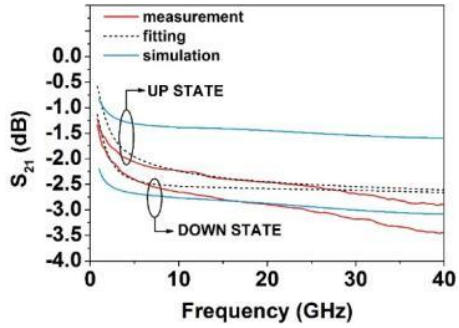


Fig 5.2. Process flow of graphene MEMs switch.



Width suspended graphene	25 µm
Length suspended graphene	5 µm
CPW signal	3 µm
CPW spacing	1 µm

NEMS equivalent parameters	
Measured	
C_{up} = 50 fF	R_{up}= 300 Ω
C_{down} = 2.5 pF	R_{down}= 300Ω
Simulated	
C_{up} = 25 fF	R_{up}= 1.4 kΩ
C_{down} = 2.5 pF	R_{down}= 252 Ω

Figure 5.3 left: Simulation and experimental RF characterization of a switch in 'on' (up) and 'off' (down) states; right: geometry of the measured device and extracted parameters using the model in T5.4

Two fabrication runs were carried out, with the design modified after run 1 to take account of improvements. Fig 5.3 shows the final results of the analysis of the completed devices. We obtain a high C_{down}/C_{up} capacitance ratio of 50. The impedance analyzer measurements show a pull-in voltage at a low actuation voltage V_{pi} = 2.9 V.

Sensors

The sensor devices made by CCS are based on their CMOS micro-hot plate design. The hot plates can be used to deposit multi-layer graphene or CNTs. The hot plate is used in operation to refresh the sensor surface by desorbing the molecule being sensed. The sensor is operated in pulsed mode to minimise operation power. The design is optimised to maximum sensitivity and minimum power. Sensed species include NOx and CO2.

Parameters	Conditions	Typical Value	Units
Operating Temperature		600	°C
Thermal Rise Time (t_{90})		15 ± 5	ms
Thermal Fall Time (t_{10})		30 ± 5	ms
Power Consumption (P_H)[1]	DC @ 600 °C	65 ± 5	mW
Heater Voltage (V_H)[1]		2.2 ± 0.3	V
Heater Current (I_H)[1]		30 ± 4	mA
Heater Resistance (R_0)		80 ± 20	Ω
Ambient Resistance (R)		40 ± 10	Ω
Sensing Area		0.05	mm^2

Table 5.2 Specifications of CCS hot plate design.

Parameter	Graphene	MOX	Comment
Operating temp (°C)	180	300	RGO much lower
Power consumption at operating temperature	8 mW	25 mW	RGO <1 mW when pulsed
Sensitive to 50 ppb NO2	Yes (CCS) Very high (DTU)	Yes (UW)	5 ppb resolution for MOX 1 ppb by DTU on nanopatterned graphene
Response time at power	180 s	< 15 s	Recovery slower for MOX
Stability	Poor	Good	RGO poor
Cross-sensitivity	Yes	Low except H_2S	Humidity issue?

Table 3. Feature comparison of graphene and metal oxide (MOx) based sensors

Compared to the established MOx sensor technology, graphene sensors can both sense 50 ppb of NOx, their baseline stability is poorer, and they are able to operate at much lower temperatures. MOx has better reproducibility and faster response, but is less sensitive.

4.2 Use and Dissemination of Foreground

Exploitation and Dissemination is covered in more detail in Deliverable D7.2.

A1. Public
The project resulted in 122 publications.

A2. There was also one large scale public dissemination exercise, the open workshop at the Carbonhagen meeting in Aug 2015.

B1 List of Applications for patents

LIST OF APPLICATIONS FOR PATENTS			
Type of IP Rights: Patents, Trademarks, Registered designs, Utility models, etc.	Application reference(s) (e.g. EP123456)	Subject or title of application	Applicant (s) (as on the application)
French patent being extended WO	Reference #FR1354795 filed 28-05-2013	Substrat conducteur électrique sur au moins une de ses faces muni d'un empilement de couches minces pour la croissance de nanotubes de carbone (NTC)	R. Ramos, H. Okuno, J. Dijon
Patent application	28036DE (Nov 2012)	Roll to roll	Aixtron
Patent application	28907DE (Jun 2015)	Roll to roll with beams	Aixtron

B2. As a result of the exploitation seminar, the following results were identified for exploitation.

OVERVIEW TABLE WITH EXPLOITABLE FOREGROUND					
Exploitable Foreground (description)	**Exploitable product(s) or measure(s)**	**Sector(s) of application**	**Timetable, commercial use**	**Patents or other IPR exploitation (licences)**	**Owner & Other Beneficiary(s) involved**
Growth on Metals	Wafer scale system for graphene	Electronics, sensors	5 years	IP	AIXTRON
Growth on Metal foil	R2R system	Coatings, lightning (OLED)	3 years	IP	AIXTRON
CVD Graphene films for optoelectronic applications	Large scale and high homogenity graphene films for opto electronics applications	Electronics, sensors, OLEDs lighting	> 7 years		GRAPHENEA
Graphene transparent electrode in OLEDs	Transparent flexible electrode based on Graphene	OLED Lighting	> 10 years		Philips
Graphene integrated photodetector	Integrated photodetector	Data communication	> 5 years		AMO
Graphene integrated modulator	Integrated absorption modulator	Data communication	> 5 years		AMO
Graphene integrated modulator	Integrated phase modulator	Data communication	> 5 years		AMO
Graphene integrated heater	Integrated heater	Data communication /integrated communication systems	> 5 years		AMO
Photomixing demonstration	Photomixing device	Telecommunication radars	2022		Thales/AMO/ Graphenea
Photosampling concept	Photosampling device	Telecommunic	2025		Thales/AMO/

		ation radars			Graphenea
GRAPHENE BASED CHANNEL	HIGH EFFICIENCY GRAPHENE BASED SPINTRONICS DEVICES	ELECTRONICS/ SPINTRONICS	AT LEAST 10 YEARS		CNRS, THALES
GRAPHENE BASED ELECTRODES	GRAPHENE BASED MAGNETIC TUNNEL JUNCTIONS	SPINTRONICS/ MEMORIES	At least 5 years		CNRS, THALES
Graphene based gas sensor on SOI	SOI micro-hotplate CCS3oI	Industrial	2015		CCS
Full CMOS integrated gold wafer process	Resisting gas sensors	Wearable / Industrial	2014		CCS
Graphene in IR gas sensors	IR detector with graphene / CNTS	Industrial	2016		CCS
Graphene in IR gas sensors	IR source with graphene / CNTS	industrial	2016		CCS
Graphene based process for RF passives and specific optimized design	Graphene tunable quantum capacitor	Radio-Frequency filters and reconfigurable RF front-ends	> 3 years	On-going search for patentatble solutions	EPFL
Technological process for graphene based MEMS switch	Suspended graphene membranes for RF MEMS switches based on graphene	Radio Frequency switches and sensor applications	> 5 years		EPFL, Graphenea
Ni based growth process	Industrial graphene processing	Materials	Link to industrial application		UCAM/Aixtron/ Graphenea/ Philips/Thales
Solid state Ni graphene growth	Industrial graphene processing	Materials	Link to industrial application		UCAM/Aixtron/ Graphenea/ Philips/Thales
Low Temperature Cu growth	Industrial graphene processing	Materials	Link to industrial		UCAM/Aixtron/ Graphenea/
High sensitive gas sensor based on graphene	NH_3 sensor for continuous monitoring in animal production	Animal production, environmental monitoring	4-5 years		DTU
CNT growth process	Ultra high density CNT shunt	Interconnects/ Integrated circuits	> 3 years		UCAM
CNT growth on graphene	3D carbon interconnects, battery electrodes	Energy / electronics	> 10 years	1 patent	CEA
High density CNT via	Carbon interconnects	Microelectronics	> 10 years	1 patent	CEA/Intel
Carbon based Interconnects	Integrated Carbon interconnects	ICT	> 5 years	-	Intel
Ethene Low temperature graphene growth process	Industrial graphene processing	Materials	Link to industrial application	-	TCD