Project Report

Project: 301028 (Soft-COM: FP7-PEOPLE-2011-IEF)
Research Fellow: Shunpu Li Scientist in Charge: Daping Chu

The fellow and scientist in charge are very grateful for the support. The outcomes from the project are very fruitful. For instance we have demonstrated n-type polymer ferroelectric field effect transistor based memory device with world-record on/off current ratio large than 10^3 in air. We have successfully manipulated micro-liquid to form sophisticated patterns with submicron resolution and short channel transistors with excellent performances were fabricated by this technique. Several papers in peer-reviewed journals and one book chapter have been published (or in press), and more papers are under preparation. Undergraduate teaching, student supervision, project proposition and management etc. skills have greatly improved during the fellowship thanks to training opportunities offered by the university.

1. Work progress and achievements during the project

1.1 The project

In this project we propose a new type non-volatile memory devices based on organic semiconductors for application of printed electronics, like low-cost identification tags and switching devices for active matrix display. A new design of organic ferroelectrics thin film transistor (FTFT) based devices will be fabricated by low cost method with reasonably high resolution. In particular, a complementary design of memory device will be fabricated, and such devices are compatible with organic complementary circuit. The new complementary devices comprise both p- and n-channel organic FTFT to ensure a minimized current flow for reading. All components of the organic FTFTs including transistor channels, both p- and n-type of semiconductors, and gate will be patterned by “3D self-aligning process” without mask alignment. The most challenge part of the project is air stable n-type FTFT development as there is very limited number of n-type organic semiconductors available currently. In addition, high resolution patterning technology development for electrical device application is an important part of the project.

1.2 Summary of progress

The project implementation includes following steps
(I). P-type and n-type organic TFT development
(II). P-type and n-type organic FTFT development
(III). 3D imprinting and integration of p-type and n-type FTFT to complementary devices.
(IV)Short-channel TFT/FTFT development.
We have successfully completed steps (I), (II) and (IV). Majority of (III) is done and the final device integration is still in progress.

1.3 Description of project progress

(1) PQT-12 p-type semiconductor devices

Transistors with p-type PQT-12 [poly(3,3‴-didodecylquaterthiophene] semiconductor were fabricated. The geometries of transistors were top or bottom gated. The fabrication process of top gated transistors is (i) gold source-drain electrodes with various channel length were prepared on glass substrates by optical lithography and subsequent lift-off use thermally evaporated Au(100nm)/Ti(10nm) and then dissolve photo-resist in acetone. (ii) Next, 50nm thick PQT12-semiconductor was spin-coated from dichlorobenzene (10mg/ml) and annealed under 80°C (20min) and 140°C (20min). (iii)Then, 500nm thick poly(methyl methacrylate)(PMMA) film was spin-coated on semiconductor and (iv) finally 100nm thick aluminium gate was deposited by thermal evaporation through shadow mask or inkjet printing polymer conductor (PEDOT:PSS). A typical output curve of the fabricated transistors is shown in Fig.1. The typical charge mobility is $0.025cm^2/VS$ and current on/off ration is 10^4 when measured in air. Bottom gated PQT-12 have fabricated and measured. In this configuration, n+ doped silicon with thermal oxidation layer (300nm) were used as bottom gate and dielectrics. The Au electrodes and PQT-12 film deposition and thermal annealing remain the same as top gated devices.

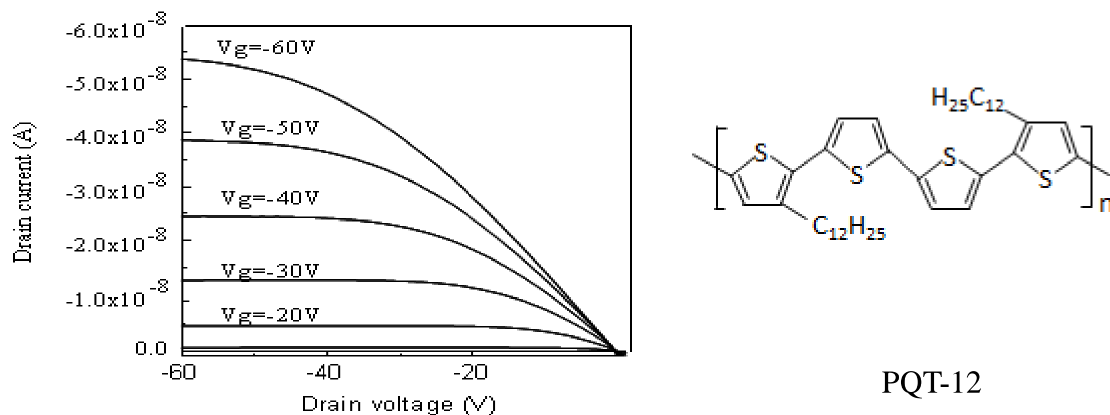


Fig.1 Typical output characteristic of TFT with PQT-12 semiconductor

(2) F8T2 p-type semiconductor devices

Transistors with p-type F8T2 [poly(9,9-dioctylfluorene-*co*-bithiophene)] semiconductor were fabricated. The geometries of transistors were top or bottom gated. The fabrication process of top gated transistors is (i) gold source-drain electrodes with various channel length were prepared on glass substrates by optical lithography and subsequent lift-off use thermally evaporated Au(100nm)/Ti(10nm) and then dissolve photo-resist in acetone. (ii) Next, 50nm thick F8T2-semiconductor was spin-coated from toluene (10mg/ml) and annealed under 80°C (20min) and 150°C (20min). (iii) Then, 500nm thick poly(methyl methacrylate)(PMMA) film was spin-coated on semiconductor and (iv) finally 100nm thick aluminium gate was deposited by thermal evaporation through shadow mask or inkjet printing polymer conductor. A typical output curve of the fabricated transistors is shown in Fig.2. The typical charge mobility is $5\times10^{-3}cm^2/VS$ and current on/off ration is 10^5 when measured in air. Bottom gated F8T2 have fabricated and measured. N+ doped silicon with thermal oxidation layer (300nm) were used as bottom gate and dielectrics. The Au electrodes and F8T2 film deposition and thermal annealing remain the same as top gated devices.

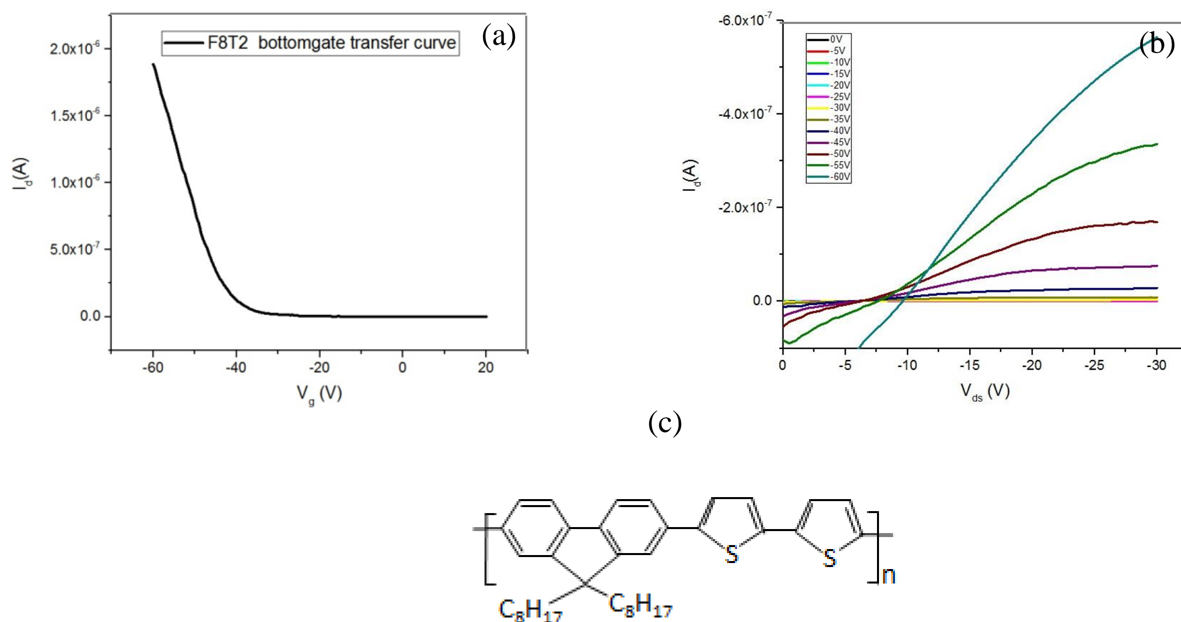


Fig.2 Performance of a bottom gated transistor with F8T2 as semiconductor where: (a) Transfer curve; (b) Out-put curve; (c) F8T2 molecule structure.

(3) P(NDI2OD-T2) n-type semiconductor devices

Transistors with n-type P(NDI2OD-T2) {poly{[N,N0-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bithiophene)}}semiconductor were fabricated. The geometries of transistors were top or bottom gated. The fabrication process of top gated transistors is (i) gold source-drain electrodes with various channel length were prepared on glass substrates by optical lithography and subsequent lift-off use thermally evaporated Au(100nm)/Ti(10nm) and then dissolve photo-resist in acetone. (ii) Next, 40nm thick P(NDI2OD-T2) (N2200 commercial name) -semiconductor was spin-coated from toluene (15mg/ml) and annealed under 80°C (10min) and 140°C (6h). (iii)Then, 500nm thick poly(methyl methacrylate)(PMMA) film was spin-coated on semiconductor and (iv) finally 100nm thick aluminium gate was deposited by thermal evaporation through shadow mask deposition or inkjet printing polymer semiconductor. A typical transfer curve of the fabricated transistors is shown in Fig.3. The typical charge mobility is 0.01cm^2/VS and current on/off ration is 10^3 when measured in air. Bottom gated transistors have also been fabricated and measured. N+ doped silicon with thermal oxidation layer (300nm) were used as bottom gate and dielectrics. The Au electrodes and P(NDI2OD-T2) film deposition and thermal annealing remain the same as top gated devices.

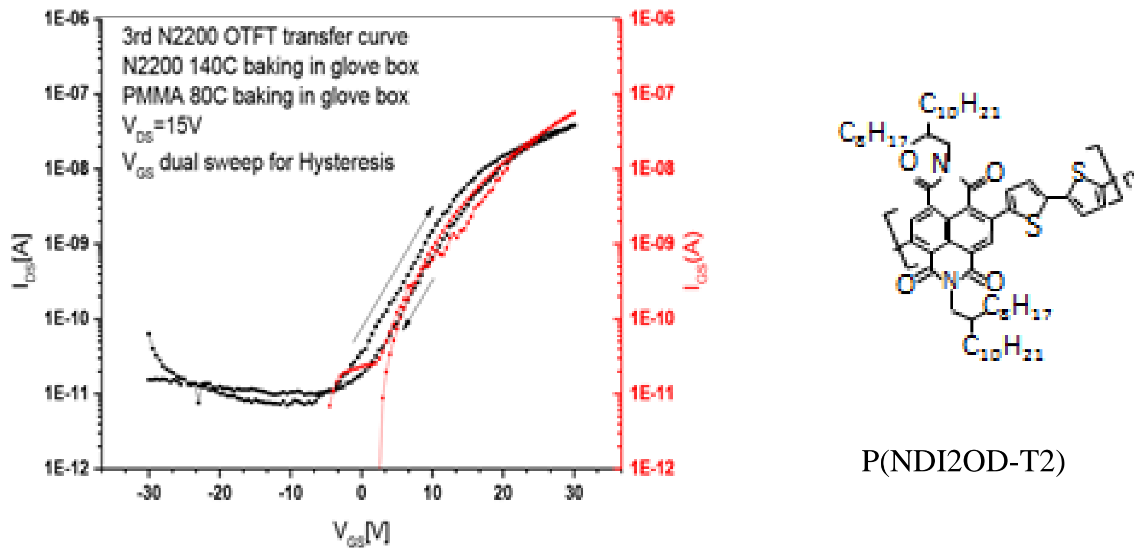


Fig.3 Transfer curve of a top gated transistor with P(NDI2OD-T2) n-type semiconductor, where red coloured curves shows leakage current between source and gate.

(4) Ferroelectric TFT memory

In this part of the project, the main focus was n-type of ferroelectric thin film transistor development as the p-type ferroelectric thin film transistor has been well developed. This is because there are a large number of p-type semiconductor materials are available. In contrast only very few benchmark n-type semiconductor materials available on market.

FTFTs with n-type P(NDI2OD-T2) {poly{[N,N0-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bithiophene)}} semiconductor and P(VDF-TrFE) (Polyvinylidene fluoride-trifluoroethylene) ferroelectric layer were fabricated. The geometries of transistors were top gated. The fabrication process is (i) gold source-drain electrodes with various channel length were prepared on glass substrates by optical lithography and subsequent lift-off use thermally evaporated Au(100nm)/Ti(10nm) and then dissolve photo-resist in acetone. (ii) Next, 40nm thick P(NDI2OD-T2) (N2200 commercial name) -semiconductor was spin-coated from toluene (15mg/ml) and annealed under 80°C (10min) and 140°C (6h) in N2 atmosphere. (iii) Then, 450nm thick P(VDF-TrFE) film was spin-coated on semiconductor from cyclohexanone and the sample was annealed under 140°C for 12h in N2. To improve wettability of P(VDF-TrFE) solution with P(NDI2OD-T2) film a layer of P(VDF-TrFE) from butyl-acetate fist spin-coated and subsequently P(VDF-TrFE) from cyclohexanone is coated again as the butyl-acetate solution has much better wettability with the P(NDI2OD-T2). The obtained P(VDF-TrFE)film from butyl-acetate solvent cannot be used to make device as the obtained film is too rough which lead very high leakage current. (iv) 100nm thick aluminium gate was deposited by thermal evaporation through shadow mask deposition or inkjet printing polymer conductor. A typical transfer curve of the fabricated FTFT is shown in Fig.4. The transfer curve shows a clear memory effect (the existing hysteresis loop between forward and backward scan) current on/off ration is 10^3 when measured in air.

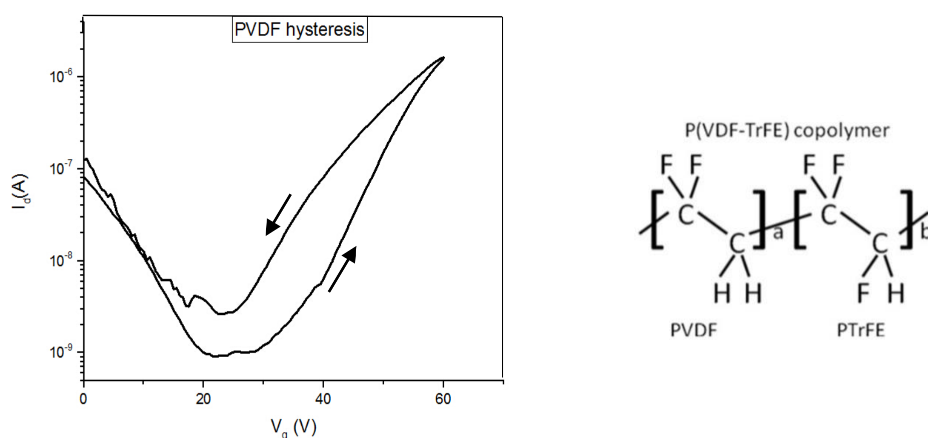


Fig.4 Transfer curve of a top gated transistor with P(NDI2OD-T2) n-type semiconductor and P(VDF-TrFE) as ferroelectrics

(5) Self-aligned 3D imprinting for fabrication of TFT electrodes

To realise a self-aligned fabrication a 3D stamp need to be fabricated. Fig.5 shows process of fabrication stamp with 2 layered structure. A layer photoresist (like AZ 5214E) was spin-coated on silicon-wafer and pattered by optical lithography (Fig.5a,b). Then a dry etching is applied by using SF6 to etching the Si down for 1μm thick (Fig.5c). After removing the photo-resist a new layer of photo-resist was spin-coated (Fig.5d) and patterned by optical lithography through another photomask(Fig.5e). Second dry etching was applied to etch the silicon down for 1μm again to define another layer of structure and residual resist was washed away by organic solvent like acetone. Similarly we can make stamp with 3 layers by adding additional lithography and etching.

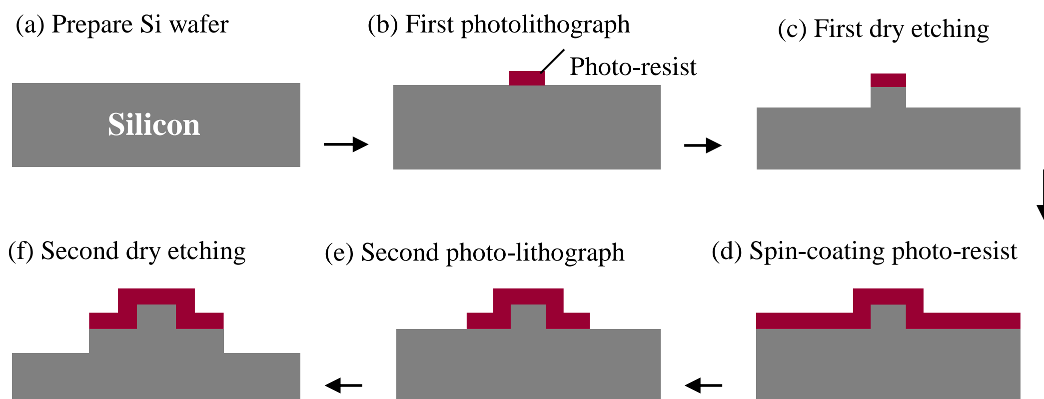
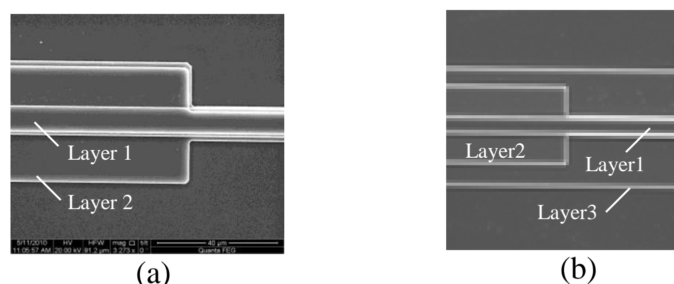


Fig.5 Fabrication process of 3D-stamp with two layers

The fabricated 3D-stamp requires anti-adhesion treatment to avoid the difficulty of stamp releasing from sample after imprinting. The anti-adhesion is done by O2 plasma treating silicon stamp and emerging the stamp subsequently into 0.01M octadecyltrichlorosilane (OTS) of tetradecane solution for 10 min and dry with N2 flow. This is achieved by chemical reaction between plasma generated –OH groups on silicon surface and octadecyltrichlorosilane. By eliminate a HCl molecule the OTS is chemically bonded with silicon-oxide. The OTS single molecule layer is highly hydrophobic. Fig.6 shows the fabricated stamps.



(a) (b)

Fig.6. Fabricated Si stamps with 2-layered (a) and 3-layered (b) structures

The imprinting is done by a process illustrated in Fig.7. A 300nm PMGI layer was spin-coated on substrate (like glass) with Au/Ti pre-deposited layers and baked at 200°C for 30min. Then a layer of PMMA[Poly(methyl methacrylate)] or polystyrene (PS) is spin-coated on to the PMGI film and baked at 100°C for 10min. Then a Si-stamp was brought to against the PMMA sample at 150°C by using a homemade imprinting device. After cooling the imprinting device to room temperature the sample was released for pattern transfer (Fig.7a). The pattern transfer is done by O2 (or mixture of O2 + CF4) plasma etching until the narrow trench is down to Au layer (Fig.7b) and a wet etching is carried out to etching Au/Ti (I2+KI in H2O for Au (50s), and 1% HF for Ti(10s)) to define source-drain channel (Fig.7c). Another plasma etching is applied to etch through the wider trench to partially expose the Au surface for deposit semiconductor (Fig.7d), Finally top PMMA (or PS) layer is removed and only PMGI stays as bank (Fig.7e). The Introduction of PMGI is because it highly stable for subsequent liquid process like inkjet printing, spin-coating.

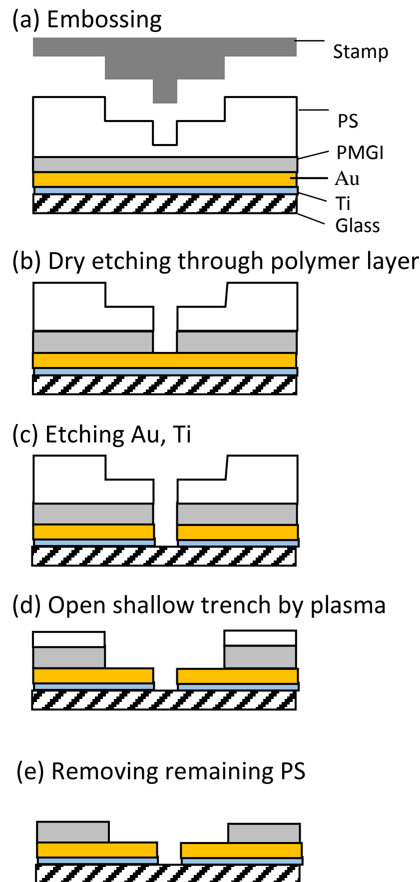


Fig.7 Schematic illustration of 3D printing process we have used

Fig.8 shows the embossed PMMA structure (Fig.8a) and fabricated Au electrode along with PMGI banks on glass substrate (Fig.8b).

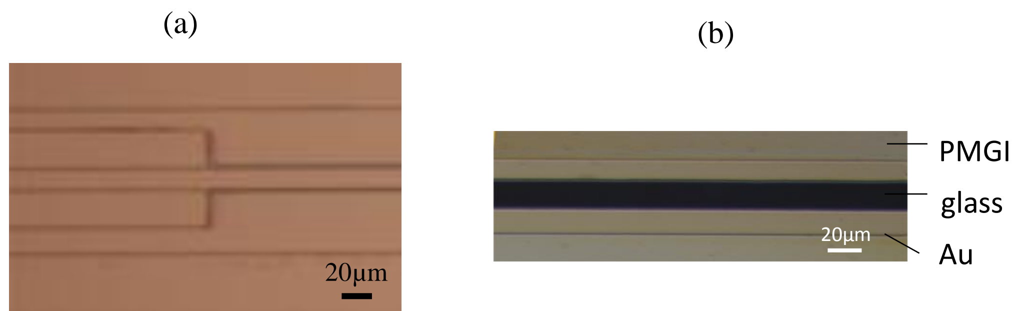


Fig.8 Optical images of embossed PMMA structure carried on substrate (a) and fabricated Au electrode along with PMGI banks on glass substrate (b).

(6) High resolution TFT channel fabrication

We have proposed high resolution sub micrometre sized TFT channel fabrication. Although we can easily make this by conventional e-beam lithography we have find that submicron channel can be made by control micro-liquid to use "coffee-stain" effect. After drying liquid droplet of solution a ring can be formed due to the capillary flow of drying liquid. Use this principle we can control the pattern formation by guiding the liquid drying with much large sized patterned stamp. The process we applied is shown in Fig.9.

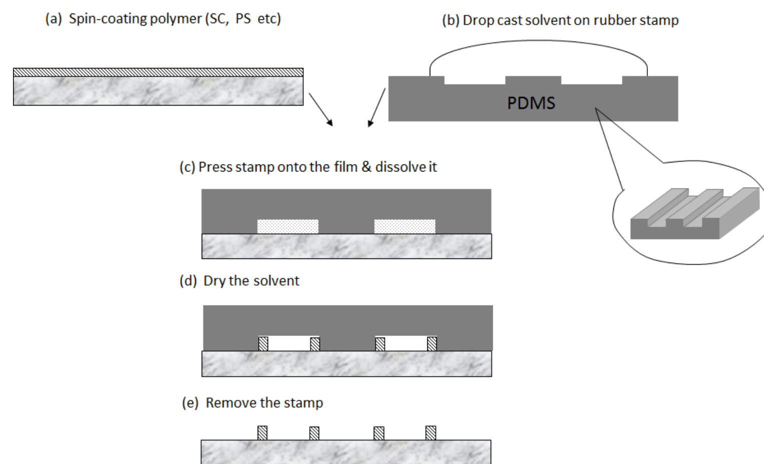


Fig.9 Process of controlled coffee-stain effect fabrication polymer lines with submicron resolution

A thin layer of polymer (like polystyrene) is spin-coated on substrate (Fig. 9a). A drop of solvent is casted onto PDMS structured stamp (with tens of micron-meter feature duplicated from photoresist pattern) (Fig. 9b) and the stamp is brought to press onto the coated film surface (Fig.9c). After drying the solvent the stamp is released from the substrate and very narrow lines are defined by the liquid flow during drying (Fig.9d,e). Fig.10 shows such a polystyrene line pattern with line width about 1 micron meter.

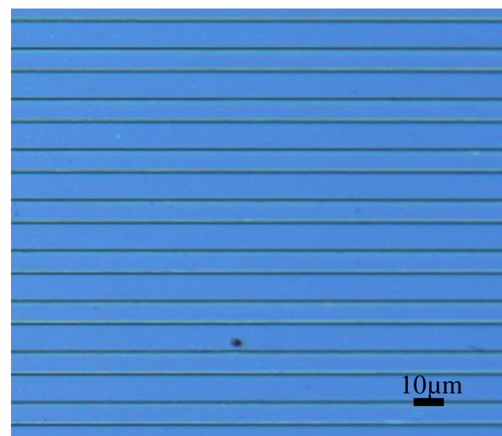


Fig. 10 Fabricated polystyrene line array on SiO2

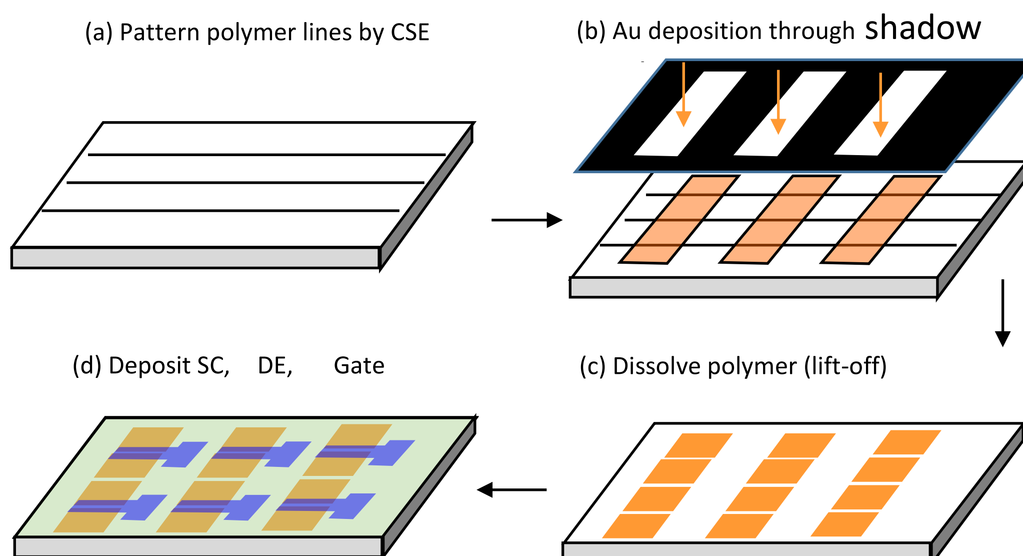


Fig.11 Short channel TFTs(FTFTs) with top gate configuration fabrication process

One can easily convert this line pattern into electrode array with short channels by lift-off process and make devices as shown in Fig. 11. We first fabricated polystyrene narrow line pattern by coffee stain effect with process as shown in Fig.9 (Fig.11a). Then 30nm Au (with 5nm Cr adhesion) electrode array is deposited through shadow mask (Fig.11b) and channels are opened by submerge samples in toluene to dissolve the polystyrene lines (Fig.11c). Then 50nm thick F8T2-semiconductor was spin-coated from toluene (10mg/ml) and annealed under 80°C (20min) and 150°C (20min). Then, 700nm thick poly(methyl methacrylate)(PMMA) film was spin-coated on the top of F8T2 and finally 100nm thick aluminium gate was deposited by thermal evaporation through shadow mask. A typical performance curves of the fabricated transistors is shown in Fig.12.

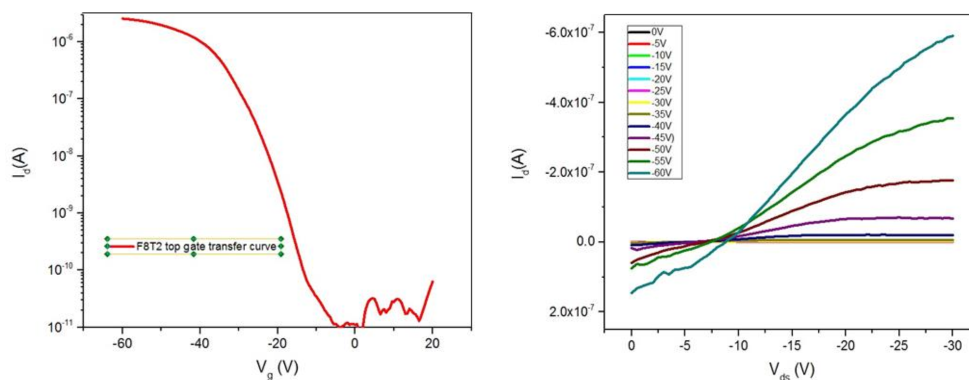


Fig.12 Performance of bottom-gated TFT with short channel defined by coffee-stain effect

1.4 Publications

(i)S. Li et al. Patterning submicrometer thick inorganic nanoparticle films by solution process and application for light trapping in solar cells, *IEEE Transaction on Nanotecnology* 13, *537 (2014)*
(ii)S. Li et al. Electrical/optical dual-function redox potential transistor, *Scientific Report.3, 3391; DOI:10.1038/srep03391 (2013).*
(iii) S. Li et al. Substrate controlled crystallization of solution processable tetrabenzoporphyrin films, Journal of Applied Physics (under review, 2014).
(iv)) S. Li et al. “Micro Photovoltaic Module Energy Harvesting” in book titled “ “*Micro-Energy Harvesting*” to be published by Wiley (2014)

1.5 Other research work involved

(1) Molecule-based opto-electronic devices were developed which include optical sensor, light trapping structure fabrication for solar cells, substrate-directed molecule aligning etc.
(2) XMCD investigation of magnetism of Fe_3O_4 films and Fe deposited on graphene.

2. Future work after project

Integrating p- and n-type FTFT to complementary memory device with 3D structure fabricated. Funding application from various funding agencies, like EPSRC, to apply the developed 3D imprinting technique into other field, for instance, bioelectronics. This technique is well suited for fabrication implantable electronic devices for in vivo electrophysiological recordings of neuronal circuits for diagnostic purposes and for brain-machine interfaces.

3. Training received

Various trainings have been carried out during the fellowship:

(1) Technique training.
Equipment usage: plasma etcher, electro-microscope, optical lithography, atomic force microscope, X-ray magnetic circular dichroism.

(2) Teaching training:
The department has arranged lecturing sharing with other academic staff for the fellow. The fellow was giving lecture on Nanotechnology for year 1 students, and on Advanced Storage Technology for year 3 students. While the fellow has attended a course organized by the University called PGCAP (Postgraduate Certificate in Academic Practice) where the fellow was trained on teaching method, assessment, and feedback techniques.

(3) Proposition training.
The fellow have prepared 4 proposals [Two proposals for EPSRC, and two proposals for synchrotron beam-time at Diamond Light Source] and one beam time proposal at Diamond Light Source was successful.

(4). Assist the scientist in charge to supervise PhD students (two PhD students are working in this project).

4. Project management

The major part of the project have been implemented as originally planned. Research has always been focusing on TFT and FTFT development. N-type FTFT with record on/off current ratio measured in air has been demonstrated. The method of short channel transistor fabrication has been modified as we found a new, interesting way to fabricate small structure. We have found that one can obtain uniform pattern with high resolution (less than 1 micron meter) through control liquid flow and drying which is very similar to coffee stain effect, but it resolution is much higher. This is a very impressive result and hopefully this can give the fellow a considerable positive career impact. With agreement from EC, the fellowship has been relocated from University of York to Cambridge University due to sabbatical of scientist in charge in York (prof. Xu). This has caused a slight delay of the progress of the project. The device integration is still in progress. Beside the proposed work in the project other relevant research in the scope of electronics have also be carried out, for example organic solar cells, crystallization of organic semiconducting materials, magnetic thin film etc. As a part of project outreach the fellow has presented organic electronic technology for undergraduate students in University of York. Paper preparation use the main result from the project is undergoing and papers with high impact factor are foreseen.

5. Career impact

The fellow has received job offer from University of Cambridge, Engineering Department as senior research associate. This will allow the fellow to generate more research results, apply more funding, and seek new career opportunity.