During the fellowship the main challenge outlined in the proposal: the design and test of a high bandwidth (1.5 GHz) and high resolution (183 kHz) single chip (mixed signal ASIC) digital spectrometer for space borne applications has been fulfilled. This ASIC has been fabricated using a CMOS 65 nm radiation tolerant process. The chip integrates both an analog to digital converter (ADC) and a digital spectrometer, the savings in terms of power compared to a system using a standalone ADC and a separate digital spectrometer are in the order of 10 W for a 30 W instrument. Normally several watts are required for line driver circuitry.

The ADC used in the chip implemented is a Successive Approximation Register (SAR) interleaved architecture previously developed in the Berkeley Wireless Research Center [(BWRC). This ADC has a bandwidth of 3GS/s and a resolution of 11 bits. One of the chief goals of the spectrometer was to combine this ADC with a digital spectrometer in the same die. This ADC was fabricated using a ST 65 nm process so part of the layout was reused, Figure 1.

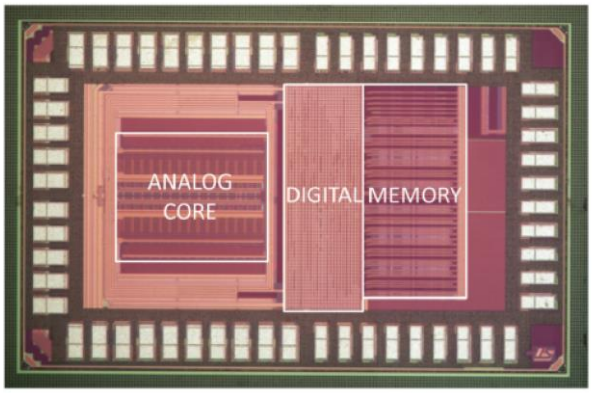

Figure 1. Die photo of the Analog to Digital Converter.

The digital spectrometer was designed using a mixed flow, the high level description was developed using Simulink and system generator for DSP taking advantage of the Digital Signal Processing (DSP) libraries previously developed by the CASPER (Collaboration for Astronomy Signal Processing and Electronics Research) group at the University of California at Berkeley. The digital backend of the chip integrated a Polyphase Filter Bank (PFB) a Fast Fourier Transform (FFT) and a digital transmitter that serializes the data and transmits it to an onboard computer. The digital architecture is shown on Figure 2.

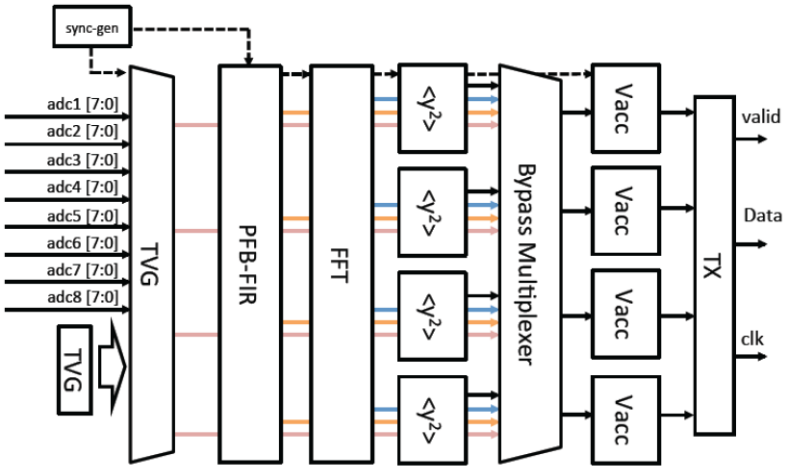

Figure 2. Digital Architecture.

This design was then tested in an FPGA using ROACH 2 board to verify the behavior of the algorithms, in particular: the desired bin shape, the power in- power out curve and the scalloping. External ADCs were used to digitize the signals.

After the algorithms have been tested in the FPGA, the next step and one of the more challenging ones is the transition between FPGA oriented Verilog to ASIC specific one. This step is done at first by an in house tool developed at BWRC called insecta, that translates the FPGA verilog into plain verilog. However, FPGAs implement double port memories and the technology used to build the ASIC only single port ones. Therefore, specific architectures containing single port memories have been designed to replace those containing double port ones. During this process it must be ensured that the new architectures have exactly the same behavior. Thus the system with the new architectures has been simulated in Modelsim against the design with dual-port memories, in order to check that the behavior is bit and cycle-accurate. After verifying that the behavior is correct the results can be passed into the place and route tools. The digital part of the chip was designed using Design compiler and IC compiler. The integration with the ADC was also performed using these tools and the final verification of the whole chip with cadence virtuoso.

As above mentioned the chip was fabricated using a ST Microelectronics 65 nm process it was taped out in July 2014 and arrived in Berkeley in October 2014 a picture of the chip can be seen on Figure 3. The chip was tested during 2015 using an Opal Kelly board.

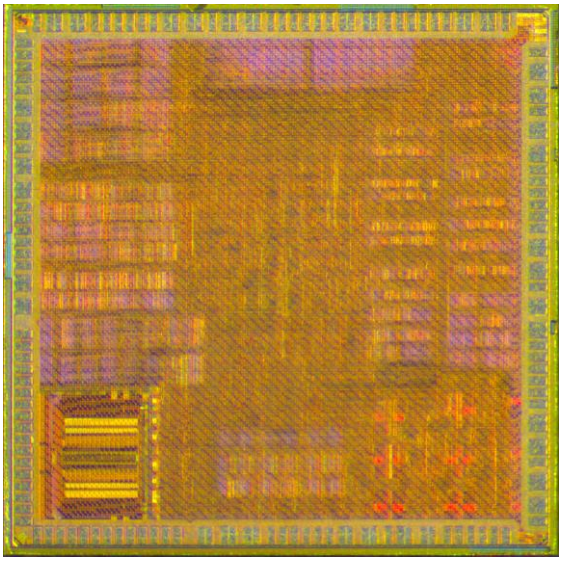

Figure 3. Die photo of the Splash chip.

The chip is still being tested, so far the behavior of the digital backend of the chip as well as the interface between the ADC, including clocks and signals and the digital spectrometer have been verified.

In addition during 2015 the researcher setup the digital design tools (Cadence) at CIEMAT in order to start the development of digital and mixed signal ASICs in the Scientific Instrumentation group of CIEMAT. Furthermore, the researcher took additional training courses related to the design of digital and mixed signal IC design in the Appleton Rutherford Laboratories in Didcot UK during fall of 2015.