Final Report

STAR

Silicon Technology Access to Research

Construction of New Infrastructure

Implemented as

Specific Support Action

Contract number: 515895

Project Co-coordinator: C. Claeys

Reporting period: from 01/10/2004 to 30/09/2007

Project funded by the European Community
under the "Structuring the European Research Area" Specific Programme
Research Infrastructure action

A. ACTIVITY REPORT

1. Progress Report

1.1 Summary of the activities and major achievements

The envisaged activities of the STAR project are the extension on the 300 mm infrastructures at the distributed processing facilities of the three partners involved, i.e., IMEC (Leuven, Belgium), CEA -LETI (Grenoble, France) and FhG (Erlangen, Germany). This part gives the status at the beginning of the project (1.1.1), at the end of Year 1 (1.1.2) and at the end of Year 2 (1.1.3) , and at the end of Year 3 (1.1.4) .

1.1.1 Status of the 300 mm faciliti es at the start of the project

The status of the 300 mm Facilities at the three different locations at the start of the STAR project is briefly summarised.

IMEC 300 mm facilities on 01/10/04

Application	Equipment Name	Equipment Modules	Supplier
Basic Infrastructure & Metrology			
MES	FAB300		Applied Materials
Foup Cleaner	U6410		Entegris
Sorter1	SPP300		Recif
Thickness and CD	Spectra Fx_SCD	Spectroscopic Elipsometer Scatterometrie	KLA-Tencor
Lithography			
248 nm Scanner 248 nm Track 193 nm Track Overlay CD-SEM	AT750S Tel ACT-12 Tel ACT-12 Archer Aim eCD-1		ASM_L Tel Tel KLA-Tencor KLA-Tencor
Furnaces & Deposition & Wet processing			
Pre Gate Clean & Wet Etch	SU-3000	Pre Gate Clean Pre Gate Clean Wet Etch High k Removal	DNS
High k Metal Gate Cluster I	Tricent	MoCVD High k MoCVD Metal Gate RTA	Aixtron
Implant & CMP & Etch			
Front End of Line Etch	DOM Stretch V3	Kyo Kyo Flex Microwave Wet Module	Lam Research

Table 1: 300 mm processing tools available at IMEC on September 30, 2004, the start of the STAR project.

These processing tools were installed in a new 300 mm clean room of 3200 m ^{2}, which was completed in July 2004.

FhG 300 mm facilities on 01/10/04

Fraunhofer IISB 300 mm Equipment			
Application	Equipment Name	Equipment Modules	Supplier
Analysis/Characterization/Metrology			
Defect Inspection	SP1TBI		KLA Tencor
Defect Inspection	ANS 100		Censor
Wafer Geometry Measurement	MX 2012-12-69		Eichhorn Haussmann
Wafer Preparation (VPD)	Wafer Surface Preparation System	fumer, scanner, dryer	GeMeTec
Lifetime Measurement	ELYMAT / ELYMOS 300		GeMeTec
Total Reflection X-Ray Fluorescence	TXRF 8300W		Atomika/Cameca
Optical Microscope	Axiotron 3, Axiocam	microscope, digital imaging	Zeiss
Waferprober	PA 300		Karl Süss
Atomic Force Microscope		defect coordinate software, contact litho option, electrical characterisation	Veeco
Spectroscopic Ellipsometry	ES4G OMA		Sopra
Organic Trace Analysis (Thermo Desorption, GCMS)	TDC / PE ATD 400		Fraunhofer IISB/Agilent
Lithography			
Spin coating	na		Fraunhofer IISB
CMP/Furnace/Wet Process/Polishing/Implant/Metallization			
Chemical Mechanical Planarization/Polishing	PM300 Apollo	cleaning, planarization, polishing	Novellus (Peter Wolters)
Double Side Polishing	AC 1800		Novellus (Peter Wolters)
Multiple Tank Cleaning	na	SC1,SC2, acid,alkaline, O_3, megasonic	Rena
Multiple Tank Etching/Cleaning	na	acid, alkaline, dryer	ASTEC
Implantation	na		Fraunhofer IISB
Metallization	na		Fraunhofer IISB
Oxidation	CVS300		Centrotherm

Table 2: 300 mm processing tools available at FhG on September 30, 2004, the start of the STAR project.

CEA-LETI 300 mm facilities on 01/10/04

Equipment	Supplier	Type	Year
CD SEM	AMAT	VERASEM	2001
XRR, XRF	JORDAN VALLEY		2002
Epi SiGe	UNAXIS		2002
Etch	AMAT	CENTURA DPS 5300A	2003
Microscope	LEICA	INS300	2003
Ellisometer	RUDOLPH	ULTRA S300	2003
Sorter	BROOKS		2003
Particules Detection	KLA	SP1	2003
CD LER,	VEECO	AFM X3D	2004
FTIR	ACCENT	QS3300	2004

Table 3: 300 mm processing tools available at CEA -LETI on September 30, 2004, the start of the STAR project.

1.1.2 Status of the STAR project at the end of Year 1

Within the first year of the project it was scheduled to start with the installation of in total 26 processing tools. The list of the different tools that had to be installed during the first year of the STAR project, according to the original Description of Work (DOW), is given in Table 4. The numbering of the tools is the one used in the DOW. It is important to remark, however, that most of these tools only had to become operational in the second year.

IMEC	CEA-LETI	FhG-IISB
1. High-*k* deposition ALD cluster	**1. Dielectric deposition processes**	**1. Nano-imprint**
2. 193 mm immersion scanner	**2. Metal layer deposition**	**2. Ultra-thin layer depostion**
3. Particle analysis system	**3. Gate stack clean/etch**	**8. APC solutions**
4. High tilt low energy implanter	**4. Prober**	**11. Single wet processing**
5. Single wafer gate stack cluster	**5. Resistance measurement**	
6. Low temperature PeCVD spacer	**6. Transmission X-ray Fluorescence**	
7. Silicide PVD	**7. Profilometer**	
8. Silicide anneal	**8. SiGe epitaxy**	
11. Transmission electron microscope	**9. Ion beam analysis**	
	10. In line transmission microscopy	
	11. Back end of line deposition	
	12. Planarization cluster	

Table 4: Overview of the scheduled infrastructure extension at the three processing facilities during the first year of the STAR project.

The summary of the different processing tools that have effectively been installed during the first year of the project is given in Table 5. More details about the activities at the three different sites, in relation to the original DOW, are given in the 1st Annual Report

IMEC	CEA-LETI	FhG-IISB
1. High-*k* deposition ALD cluster	**1. Dielectric deposition processes**	**1. Nano-imprint**
2. 193 mm immersion scanner	**2. Metal layer deposition**	
3. Particle analysis system	**3. Gate stack clean/etch**	
4. High tilt low energy implanter	**4. Prober**	
5. Single wafer gate stack cluster	**5. Resistance measurement**	
6. Low temperature PeCVD spacer	**6. Transmission X-ray Fluorescence**	
7. Silicide PVD	**8. SiGe epitaxy**	
8. Silicide anneal	**9. Ion beam analysis**	
9. Advanced junction anneal	**10. In line transmission microscopy**	
10. Epitaxial deposition	**11. Back end of line deposition**	
11. Transmission electron microscope	**12. Planarization cluster**	
12. Front end of line CMP	**15.Maskless direct write lithography**	
16. Back end of line Cu EPC	**18. Inteconnect metal/dielectric**	

Table 5: Overview of the effective infrastructure extension at the three processing facilities during the first year of the STAR project.

For IMEC, all the original foreseen processing tools have been installed on time. There was no deviation of the schedule for year 1 as outlined in Table 4. However, two processing tools (item 10 - Epitaxial deposition, and item 12 - Front end CMP) have even been advanced in the time schedule and were already in the process start-up phase before the end of phase 1. Also the timing on the back end of line Cu ECP (item 16) had been advanced and was scheduled to be ordered sooner than originally planned. It was installed in the first quarter of the second year.

For CEA-LETI there were during the execution of the first year of the project some changes compared to the original time schedule given in Table 4. The summary of the status at the end of the first phase was as follows:

- Of the 12 scheduled process tools the installation of 11 of them occurred as foreseen;
- 3 tools (13. back side clean; 15. Direct write lithography and 18. Interconnect dielectric) have been installed in advance;
- Process item 7 (Profilometer) of the original schedule has not been installed and will also be installed in Year 2 ;
- Tool number 15 has been advanced in the time schedule and has been adjusted in view of the strategic importance of this tool, as explained in more detail in section 1.3.2 of the Year 1 Status report.

For FhG, during the execution of phase 1 of the project no major changes in the tool set occurred, but some delay of two items, tool 2 and tool 11, had to be reported compared to the original time schedule given in Table 4. Item 8, which will be integrated in item 2, is directly related to the choice of the equipment for item 2 and is therefore also delayed. However, these delays will not have any impact on the total set of tools that will be installed at FhG during the execution of the project.

It can be stated that the first phase of the STAR project was successfully executed. The majority of the original scheduled processing tools had been installed in agreement with the implementation plan outlined in the Description of Work. Two process tools, which are linked to each other (items 2 and 8 from FhG) had to be delayed in view of more stringent specifications and the equipment market evaluation. For these tools the selection phase was at the end of Year 1 in the final stage. Only for one process tool (item 7 from CEA-LETI) it was decided to shift the installation to the second year. However, this has no impact on the overall goal and timing of the project.

1.1.3 Status of the STAR project at the end of Year 2

Within the second year of the project it was originally scheduled to start with the installation of in total 24 processing tools. The list of the different tools that had to be installed during the second year of the STAR project, according to the original Description of Work (DOW), is given in Table 6. The numbering of the tools is the one used in the DOW. However, it is important to remark that several of these tools only have to become operational in the third year.

IMEC	CEA-LETI	FhG-IISB
10. Epitaxial deposition	**13. Back side clean**	**3. Ion implantation and anneal**
12. Front end of line CMP	**14. Track**	**4. Alternative lithography**
13. Back end of lien CMP	**15. Overaly system**	**5. PVD cluster**
14. Back end of line W CVD	**16. Poly Si deposition**	**6. Wet processing**
15. Back end of line wet processing	**17. Advanced characterization**	**7. Ething system**
16. back end of line Cu EPC	**18. Interconenct metal/dielectric**	**10. Wafer bumping equipment**
17 Back end of line process metrology	**19. Advanced cleaning system**	**12. Cluster tool**
18. Back end of line PVD	**20. back end of line etch**	
	21. Low-k treatment	

Table 6 Overview of the scheduled infrastructure extension at the three processing facilities during the second year of the STAR project.

The summary of the different processing tools that have effectively been installed during the second year of the project is given in Table 7. More details about the activities at the three different sites, in relation to the original DOW, are given in section 1.3.

IMEC	CEA-LETI	FhG-IISB
10. Epitaxial deposition **12. Front end of line CMP** **13. Back end of line CMP** **15. Back end of line wet processing** **16. back end of line Cu EPC** **17 Back end of line process metrology** **18. Back end of line PVD**	**7. Integrated metrology -Profilometer** **12. Planarization cluster** **17. Advanced characterization** **20. back end of line etch** **21. Low-k treatment**	**1. nano-imprint** **2. Ultra-thin layer deposition** **8, APC solutions**

Table 7: Overview of the effective infrastructure extension at the three processing facilities during the second year of the STAR project.

The summary of the status at the end of phase 2 (at 30/09/06) is as follows:

For IMEC 90% of the original foreseen processing tools have been installed on time and are already operational. The deviations from the original schedule are:

- Processing tools 13, 15-18 are already operational, whereas this was not planned until in year 3. Process tool 18 (Back end of line PVD) has even been ordered already in November 05 and is operational, whereas originally it was only scheduled to become operational by the middle of 2007.
- Process tool 14 (Back end of line W CVD) has not been ordered yet. For internal planning reasons and the strategic choice of priorities the tool will not be ordered before the middle of 2007.

Therefore it can be concluded that there was no deviation of the schedule for year 2 related to the total number of installed processing tools. Several tools were even much earlier operational than originally planned. Also the timing on the back end of line PVD has been advanced.

For CEA/LETI 86% of the original foreseen processing tools have been installed on time. The deviations from the original schedule are:

- For 18 of the scheduled processing tools the installation has been done as foreseen;
- Process tools 14 (Track) and 19 (Advanced cleaning system) have not been installed, but their planning is shifted to the third year of the project;
- Process tool 16 (Poly Si deposition) is no longer scheduled for Year 3

For FhG, during the execution of phase 2 of the project no major changes, but some delay of items, especially of tool 2, 3, 8 and tool 11, had to be reported compared to the original time schedule given in Table 16. Item 8, which was intended to be integrated into tool 2, be integrated in item 12, is directly related to the choice of the equipment for item 12.

1.1.4 Status of the STAR project at the end of Year 3

For IMEC only 1 item had to be installed in year 3, and this has been executed on time. Therefore, all original foreseen processing tools have been installed and are operation.

For LETI the process tools foreseen for year 3 have been installed. Globally, it can be stated that 95% of the original foreseen processing tools have been installed on time. There is only 1 process tool that was not installed during the execution of the project, due to a strange in the overall strategy of CEA-LETI. However, this has no impact on the successful completion of the project.

For FhG is was envisaged to have 13 processing items installed and operational. Present 9 items are on schedule, 2 items are ordered and will be installed in 2008, and 2 tiems are no longer on the strategic investment plan. However, these deviations have no direct impact on the overall STAR project.

More details on the STAR activities during year 3 and the final status are outlined in the section 1.3 for the different STAR partners.

1.2 Consortium Management Activities

The total management effort in man-months of the three partners during the third year of the project is given in Table 8.

Participant number	**1**	**2**	**3**	
Participant short name	**IMEC**	**CEA-LETI**	**FhG**	**Total**
Person-months	**18.3**	**7.4**	**8.9**	**34.6**

Table 8: Person-months involved in the management activities during the Third year of the STAR project.

During the third year of the project, no General Meeting with all the partners involved, has been organized. However, there have been several bilateral meetings between the Project Coordinator and CEA-LETI and FhG, respectively. These discussions took place in combination with meetings that were scheduled in relation to other EU projects. During the third year, which was focussing on the continuation of the infrastructure extension at three distributed site, there was no need for organising additional General Meetings.

During the third year of the project there have been no major difficulties encountered in the execution of the project. An important aspect to mention is that the three partners are also partner of the NANOCMOS/PULLNANO and SEA-NET EU FP6 projects. These projects had regular meetings and allowed to informally interact with each other.

There were no specific Milestones or Deliverables defined for the third year of the project. In the DOW a general time schedule is given for the extension of the distributed infrastructure (based on the installation of a set of processing tools). The actual status of the installation of the different processing tools in comparison with the original envisaged time schedule will be discussed in more detail in section 1.3.

1.3 Other specific construction activities

This section gives a description of the infrastructure extension activities performed at the site of the different partners, in accordance with the work packages defined in the Description of Work.

1.3.1 Work package 1: Extension of the 300 mm infrastructure at IMEC

The person-months involved in the execution of work package 1 during the second year of the project are given in Table 9. For this work package the only partner involved is IMEC. However, for the third year for the project IMEC did not needed any additional personnel in order to complete the Specific Action. The needed resources were acquired from other internal or external projects.

Participant number	**1**	**2**	**3**	
Participant short name	**IMEC**	**CEA-LETI**	**FhG-IISB**	**Total**
Person-months	**0**	**-**	**-**	**0**

Table 9: Person-months involved in the execution of WP1 during year 3.

The implementation plan for IMEC is given in Table 10.

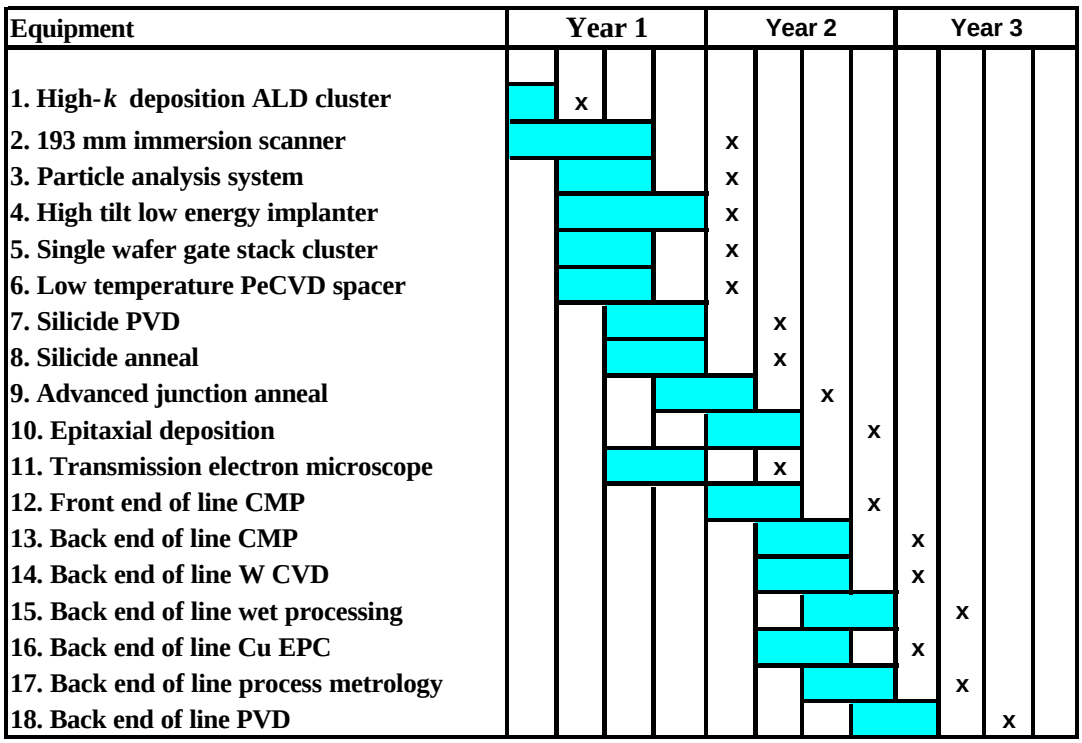

Table 10: IMEC's' STAR implementation plan. Year 1 is covering the period 01/10/04 - 30/09/05, Year 2 (reporting period) covers the period 01/10/05 -30/09/06, while Year 3 is covering the period 01/10/06 -30/09/07.

According to Table 11, IMEC envisaged to install (or start to install) 10 processing tools in the first period, 8 tools in the second period, and 2 tool s in the third year of the STAR project. The "*" in the Table gives an indication when the processing tools had to be operational.

The processing tool 1-9 and 11 were installed and operational before the end of Year 1, while for tools 10 and 12 install ation started already in Year 1 (was only scheduled for installation in Year 2) and were at the end of th at reporting period in the process start-up phase. They became fully operational in Year 2. Processing tools 13, 15-18 became already operational in year 2, although this was not planned until in year 3.
In Year 3, the following process tool has been ordered and installed:

14. <u>Back end of line W CVD</u>

Processing tool aiming at filling the via's (contact holes underneath the first metal line or between me tal lines) with W. This process step is essential for advanced CMOS technologies.

The installed tool is the **"Centura W-deposition"**.

The tool was delivered in May 2007 and is operational.

<u>Status summary</u>

All the original foreseen processing tools have been installed on time and are operational. It can therefore been concluded that for IMEC the project has successfully been executed.

1.3.2 Workpackage 2: Extension of the 300 mm infrastructure at CEA -LETI

The person-months involved in the execution of workpackage 2 during the third year of the project are given in Table 11. For this workpackage the only partner involved is CEA-LETI. The needed resources were acquired from other internal or external projects.

Participant number	1	2	3	
Participant short name	IMEC	CEA-LETI	FhG-IISB	Total
Person-months	-	0	-	0

Table 11: Person-months involved in the execution of WP2 during year 3.

The implementation plan for CEA-LETI, referred to in the Description of Work, is given in Table 12.

Equipment	Year 1				Year 2				Year 3			
1. Dielectric deposition processes					x							
2. Metal layer deposition					x							
3. Gate stack clean/etch					x							
4. Prober			x									
5. Resistance measurement			x									
6. Transmission X-ray Fluorescence					x							
7. Profilometer					x							
8. SiGe epitaxy							x					
9. Ion beam analysis							x					
10. In line transmission microscopy							x					
11. Back end of line deposition									x			
12. Planarization cluster									x			
13. Back-side clean											x	
14. Track											x	
15. Overlay system											x	
16. Poly-Si deposition											x	
17. Advanced characterization										x		
18. Interconnect metal/dielectric												x
19. Advanced cleaning system												x
20. Back end of line etch												x
21.Low-*k* treatment												x

Table 12: CEA-LETI's STAR implementation plan. Year 1 is covering the period 01/10/04-30/09/05, Year 2 (reporting period) covers the period 01/10/05 -30/09/06, while Year 3 is covering the period 01/10/06 -30/09/07.

According to Table 12, CEA-LETI envisaged to install 4 processing tools in third period of the STAR project.
For CEA-LETI there were during the execution of phase 2 of the project some changes compared to the original schedule. These changes have also been reported i n the 1st and 2nd Annual Reports. The modification were a shift of the installation of item 14 and 19 and the decision not to install item 16 because of a change in the internal CEA -LETi strategy.

The summary of the status at the end of phase 3 (at 30/09/07) is described below.

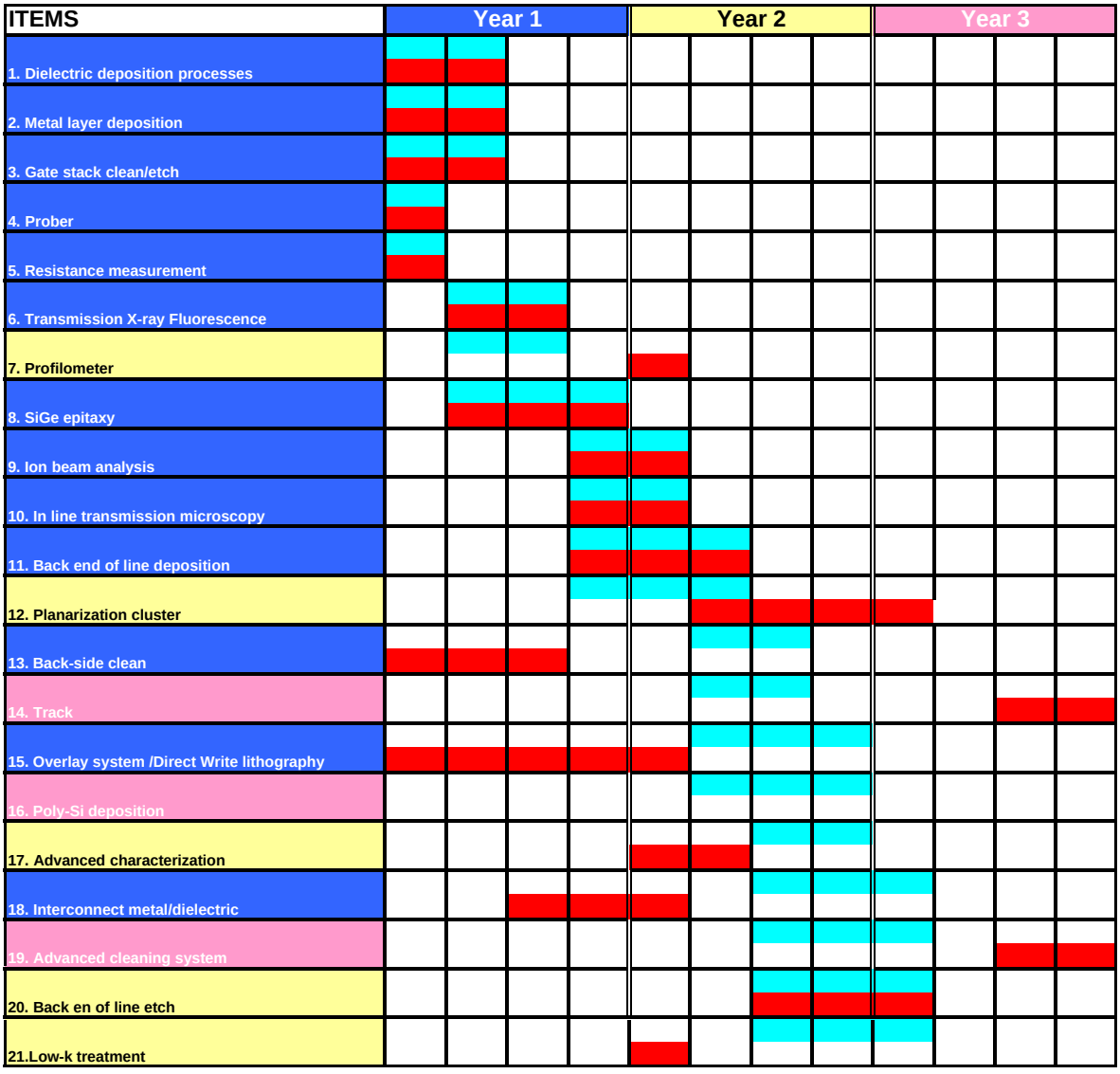

Table 13: Updated time schedule of the installation of 300 mm processing tools at CEA - LETI.

Equipment	Supplier	Type	Specication	Selection & Ordering	Shipment	Delivery	Hook up	Hardware Start up	Process Start up	Aceptance	Operational
1. Dielectric deposition processes	TEL	FORMULA									
2. Metal layer deposition	TEL	TRIAS									
3. Gate stack clean/etch	LAM ASM	2300 LEVITOR									
4. Prober	TEL	P12XL									
5. Resistance measurement	EURIS	NAPSON-WS-3000									
6. Transmission X-ray Fluorescence	RIGAKU	VPD +TXRF 300									
7. Profilometer	KLA TENCOR	HRP 340									
8. SiGe epitaxy	ASM	EPSILON 3200									
9. Ion beam analysis	HVEE IONTOF	MEIS TOF SIMS									
10. In line transmission microscopy	FEI	FIB TEM									
11. Back end of line deposition	SEMITOOL	RAIDER									
12. Planarization cluster	EBARA	FREX-300S									
13. Back-side clean	SHIBAURA	ALLEGRO									
14. Track	SOKUDO	DNS RF3A									
15. Overlay system	LEICA	SB 350 DW									
16. Poly-Si deposition											
17. Advanced characterization	KLA TENCOR FEI	SP2 TITAN TEM									
18. Interconnnect metal/dielectric	AMAT	PRODUCER DIEL									
19. Advanced cleaning system	FSI	MAGELLAN									
20. Back en of line etch	LAM	REACTOR									
21.Low-k treatment											

Table 14: Updated status of the installation of 300 mm processing tools at CEA -LETI.

These Tables clearly show that 20 processing tools are operational today. Only item 16 (POLY Si deposition tool) is not installed.

The details of the processing tools 14 and 19 related to the activities performed in year 3 are described lower.

14. Track

For their development on resist processes d edicated to 193nm lithography and e-beam lithography, CEA LETI acquired a new track, the " **DNS RF3A": SOKUDO**.

With this track, CEA LETI will develop new lithography processes as coating, bake and development of photo resist. It will be use to study Anti R eflective Coating (Top and Bottom) and top coat. This track is interfaced with an ArF scanner.

The "**DNS RF3A": SOKUDO**" track have been delivered at CEA LETI on January 2007 and it is operational since June 20 th 2007

19. Advanced cleaning system

For their advanced cleaning processes CEA LETI bought the **MAGELLAN** System. This tool is a fully automated, batch immersion, wet processing tool. It is able to manage 200 or 300mm standard silicon wafers and operate 50 wafers simultaneously.
Two applications are targeted: pre cleaning before molecular bonding (hydrophilic and hydrophobic surfaces) and advanced FEOL cleanings. The CEA-LETI system is configured with 4 Process Modules: Process Module 1 => for CMOS and Wafer Bonding applications (DI/HCl rinse, HF-Last, Drying); Process Module 2 => for Wafer Bonding applications (SC1+ SC1 rinse / with mega sonic effect); Process Module 3 => for CMOS application (HF + HF rinse) and Process Module 4 => for Wafer Bonding application (Ozone)

The **MAGELLAN** System was shipped on June 6th 2007 and the acceptance signed on November 2007.

Status summary

The summary of the status at the end of phase 3 (at 30/09/07) is as follows:

95% of the original foreseen processing tools have been installed on time. The deviations from the original Schedule are:

- For 20 of the scheduled processing tools the installation has been done as foreseen;
- Process tool 16 (Poly Si deposition) has not been installed due to a change in strategy. However, this has no direct impact on the overall STAR project.

1.3.3 Work package 3: Extension of the 300 mm infrastructure at FhG

The person-months involved in the execution of work package 3 during the second year of the project are given in Table 15. For this work package the only partner involved is FhG. However, the third year of the project FhG did not needed any additional personnel in order to complete the Specific Action. The needed resources were acquired from other internal or external projects.

Participant number	1	2	3	
Participant short name	IMEC	CEA-LETI	FhG-IISB	Total
Person-months	-	-	0	0

Table 15: Person-months involved in the execution of WP3 during year 3.

The implementation plan for FhG, referred to in the Description of Work, is given in Table 16.

	Year 1				Year 2				Year 3			
1. Alternative lithography: nano-imprint				x								
2. Ultra thin layer deposition					x							
3. Ion implantation and annealing									x			
4. Alternative lithography: mask making										x		
5. PVD cluster											x	
6. Wet processing											x	
7. Etch system												x
8. APC solutions		x										
9. Metrology/analytical tool										x		
10. Wafer bumping equipment										x		
11. Single wet processing					x							
12.Cluster tool										x		
13. Integrated metrology						x						

Table 16: FhG's *STAR implementation plan. Year 1 is covering the period 01/10/04 - 30/09/05, Year 2 (reporting period) covers the period 01/10/05 -30/09/06, while Year 3 is covering the period 01/10/06 -30/09/07.*

The progress at FhG is as follows

1. Alternative lithography: nano-imprint

ANO Patterning Stepper NPS300 (SÜSS MicroTech)

Following the ITRS, cost-effective nanoreplication techniques like nanoimprint lithography are possible solutions for replacing conventional lithography systems for sub-50nm resolution. The NPS 300 is a very flexible nanoimprint lithography system available as a manually loaded machine or as a fully automated system. The automated stamp pick up, allows printing different pattern from different stamps on a wafer within a single cycle. Using in-situ imprinting material dispensing and UV curing, the Step & Cure method is used for UV-NIL applications.
The installed tool is the "NPS300" from SÜSS MicroTech and is installed in the cleanroom of the IISB in Erlangen.
The tool was delivered in 2006. Factory acceptance tests were passed and the equipment is operational as of Q4 2006. The access to the tool is organised by IISB Erlangen.

2. Ultra thin layer deposition

Advanced High-K ALD Cluster Eureka 3000 System (JuSung)

The Advanced High-K ALD Cluster tool is used for the deposition of atomic layers of high-k dielectric materials on 300mm wafer surfaces.
The installed tool is the "Advanced High-K ALD Cluster Eureka 3000 System" from JuSung (ofec99-03) and is installed in the cleanroom of the CNT in Dresden.
The tool was delivered in 2007. Factory acceptance tests were passed and the equipment is operational as of Q2 2007. The access to the tool is organised by IISB Erlangen and to be approved by CNT Dresden.

3. Ion implantation and annealing

The investment in a RTP-Modul Corona 800V from Kornic is planned and the equipment is already ordered, but the installation at the IISB site will be in 2008 and therefore out of the funding period.

4. Alternative lithography: mask making

Sputteranlage CS 400 S Clustersystem (Ardenne)

The sputter equipment is a state of art tool for the deposition of high reflective materials on glass substrates. The IPMS scientists had developed a new technology for stress compensated metal insulator stacks, which is one assumption for nanoscaled flat movable mirror arrays used in mask fabrication. The tool plays a key role in the developments of new concepts for mask writing on glass media.
The installed tool is the "Sputteranlage CS 400 S Clustersystem" from Ardenne and is installed in the cleanroom of the IPMS in Dresden.
The tool was delivered in 2006. Factory acceptance tests were passed and the equipment is operational as of Q4 2006. The access to the tool is organised by IISB Erlangen.

5. PVD cluster

No investment in a PVD cluster was done in the funding period.

6. Wet processing

Wet Bench (DNS)

In semiconductor manufacturing a cleaning process is generally performed after most etch implant and deposition processes. It is a key component in defect free preparation of interconnect circuits.
The installed tool is the "Wet Bench" from D NS (nasc31-01) and is installed in the cleanroom of the CNT in Dresden.
The tool was delivered in 2007. Factory acceptance tests were passed and the equipment is operational as of Q2 2007. The access to the tool is organised by IISB Erlangen and to be approved by CNT Dresden.

7. Etch system

Centuura AP, Etch Chamber (Applied Materials)

Structures in the nanometer scale are usually created by dry etch processes. The Centura AP Etch Chamber is a state of the art plasma etch equipment for 300mm wafer mat erial.
The installed tool is the "Centura AP Etch Chamber" from Applied Materials (etcc80 -01" and is installed in the cleanroom of the CNT in Dresden.
The tool was delivered in 2006. Factory acceptance tests were passed and the equipment is operational as of Q1 2007. The access to the tool is organised by IISB Erlangen and to be approved by CNT Dresden.

8. APC solutions

Kristallziehanlage CGS (Crystel Growing Systems)

A new crystal growth equipment for the preparation of sapphire ribbons with dimensions of up to 10 x 50 x 300 mm was installed. The tool uses the EFG method which is a versatile technique for the processing of materials with a melting point above 1800°C.
The installed tool is the "Oxidanlage" from Crystel Growing Systems and is installed in the cleanroom of the IISB in Erlangen.
The tool was delivered in 2005. Factory acceptance tests were passed and the equipment is operational as of Q1 2006. The access to the tool is organised by IISB Erlangen .

9. Metrology/Analytical tool

Review SEM with FIB (Applied Materials)

Defect control is a key technique in the development and improvement of semiconductor preparation processes. A Review SEM has the ability to resolve and analyse defects and structures in the nanometer scale. Focused Ion Beam (FIB) is used for the preparation of samples for improved resolution and other special analytic techniques.
The installed tool is the "Verity SEM" from Applied Materials (mesc24 -02) and is installed in the cleanroom of the CNT in Dresden.
The tool was delivered in 2006. Factory acceptance tests were passed and the equipment is operational as of Q2 2007. The access to the tool is organised by IISB Erlangen and to be approved by CNT Dresden.

SIMS (second ion mass spectrometer) (Cameca)

Secondary ion mass spectrometry (SIMS) is a technique used to analyze the composition of solid surfaces and thin films with a focused ion beam and collecting and analyzing ejected secondary ions. It is the most sensitive surface analysis technique, being able to detect elements present in the parts per billion range.
The installed tool is the SIMS from Cameca (mfac15 -02) and is installed in the cleanroom of the CNT in Dresden.
The tool was delivered in 2007. Factory acceptance tests were passed and the equipment is operational as of Q3 2007. The access to the tool is organised by IISB Erlangen and to be approved by CNT Dresden.

TOFSIMS (IonTof)

High resolution ToFSIMS 'resolves' the problem of overlapping peaks of secondary ions with the same nominal mass and promotes the technique into the level of accurate mass measurement which is often necessary for the identification of secondary ion signals . High resolution is also important for improved analytical sensitivity since the practical detection limits of some species are restricted by mass overlap.
The installed tool is the "TOFSIMS" from IonTof (mfac15 -02) and is installed in the cleanroom of the CNT in Dresden.
The tool was delivered in 2006. Factory acceptance tests were passed and the equipment is operational as of Q2 2007. The access to the tool is organised by IISB Erlangen and to be approved by CNT Dresden.

10. Wafer bumping equipment

No investment in a wafer bumping equipment was done in the funding period.

11. Single wet processing

Advanced Via Cleaner Tool (Semitool)

The Advanced Via Cleaner Tool is a cluster Tool based on the Semitool Raider mainframe for research and process development. It enables the cleaning and treating of single wafers. Is has the capability for various special cleaning methods like ultrasonic and high pressure application of reactants. Samples of organic compounds can be connected to the system to perform special treatment of wafer materials.
The installed tool is the "Semitool Raider Via Cleaner" (nasc61 -01) and is installed in the cleanroom of the CNT in Dresden.
The tool was delivered in 2006. Factory acceptance tests were passed and the equipment is operational as of Q2 2007. The access to the tool is organised by IISB Erlangen and to be approved by CNT Dresden

12. Cluster tool

The investment in a 300mm Clustertool from Kornic is planned and the equipment is already ordered, but the installation at the IISB site will be in 2008 and therefore out of the funding period.

13. Integrated metrology

Nano Raman Spectroscopy (Soliton)

Raman spectroscopy is a spectroscopic technique used in condensed matter physics and chemistry to study vibrational, rotational, and other low-frequency modes in a system. It is used to characterize materials and find the crystallographic orientation of a sample. Nano-Raman Spectroscopy shows a drastic improvement in sensitivity for samples on a small scale.

The installed tool is the "Nano Raman Spectroscopy" from Soliton (mesc39-01) and is installed in the cleanroom of the CNT in Dresden.

The tool was delivered in 2007. Factory acceptance tests were passed and the equipment is operational as of Q2 2007. The access to the tool is organised by IISB Erlangen and to be approved by CNT Dresden.

XRR/XRD X-Ray-Diffractometer (Bede)

X-ray scattering techniques (XRR and XRD) are a family of non-destructive analytical techniques which reveal information about the crystallographic structure, chemical composition, and physical properties of materials and thin films and widely used in the research of semiconductor materials.

The installed tool is the "XRR/XRD" from Bede (mesc28-01) and is installed in the cleanroom of the CNT in Dresden.

The tool was delivered in 2007. Factory acceptance tests were passed and the equipment is operational as of Q2 2007. The access to the tool is organised by IISB Erlangen .

Status summary

During the last year FhG has been installing a variety of processing tool, so that presently 9 items have been accomplished (installed and operational). For internal strategic reason some items had to be shifted and will therefore not be installed before the end of the STAR project:

- **Item 3 (ion implantation and anneal). The equipment is already ordered and will therefore be installed in 2008.**
- **Item 5 (PVD cluster). No investment done in the STAR project period.**
- **Item 10 (wafer bumping). No investment done within the STAR project.**
- **Item 12 (cluster tool). The equipment is already ordered and will therefore be installed in 2008.**

This implies that of the initial 13 items, 9 are installed within the STAR project, 2 are ordered and will become operational in 2008, and 2 are presently not on the strategic investment plan.

1.4 Update of the non-confidential Project information

The updated non-confidential Project information that can be published on the Commission Website is given in Annex 2.

Reporting period:

01/10/2004 – 30/09/2007.

***Project Objectives*:**

The project is aiming to contribute to the establishment a world-wide recognized and unique European-based Research Platform for advanced silicon research and development. The set-up of the overall joint research platform is ambitious and necessary to keep Europe at a world wide top-level. This was done by extending the infrastructure within the 300 mm compatible process driven research pilot-lines under construction at IMEC, CEA/LETI and FhG with mainly complementary equipment, and by cross-linking the three new research facilities for an optimized wafer exchange enabling the operation of a so-called 'distributed processing facility'. This European Research Platform will be accessible to the academic research community allowing them to make use of state-of-the-art equipment in order to boost up their own research programs and/or to enter in joint development programs. This European global access will safeguard and further strengthen the leading European role in important research fields related to advanced silicon processing, emerging devices and nanotechnology.

Project Achievements:

Since the start of the STAR project, i.e., October 1, 2004, a total of 46 new processing tools have been installed in order to extent the 300 mm processing infrastructure at IMEC, CEA-LETI and FhG, respectively. These tools allow research and development on state-of-the-art processing steps and process modules related to sub 45 nm technology nodes. Presently, modes of operation are under investigation to enable the academic research community to have access to the infrastructure. Beside an extension of the large number of existing bilateral agreements between the involved research centres (i.e., IMEC, CEA-LETI or FhG) and universities enabling access the distributed processing infrastructures, a more global approach of the future structuring of the access of the academic research community is on going within the frame of ENIAC. In the later pahse the STAR platform will be integrated into the PRINS research infrastructure. The practical aspects of 300 mm wafer exchange between processing sites have been conceptually worked out in the FP6 EU FLYING WAFER project. The STAR project has been completed on schedule and even some additional processing tools will be installed at the 300 mm processing facilities of IMEC, CEA-LETI and FhG, leading in 2008 in more than 50 installed and operational processing tools .

2. List of Deliverables

The STAR project has as main deliverable the extension of the infrastructure at the three processing sites of the partners. In the original DOW, a tentativ e indication was given when the new processing tools could become operational. This is in the Tables 9 (IMEC), 11 (CEA-LETI) and 14 (FhG) indicated by a "x". Although it is difficult to plan long in advance when a processing tool will become operational, a s this depends on external factors (ordering date, deliverable date, acceptance date) it could be used as a type of monitor in order to have a general feeling of the overall progress of the project. To some extent it can be considered as a kind of 'interme diate' Deliverable.
At the end of the second year of the project the following summary can be made:

- IMEC: At the end of Year 3 it was scheduled that 18 new tools would have been installed (or in the installation phase) and that all of them would be operat ion for users. The status of the different tools has been described in detail in section 1.3.1 . All tools are installed and are operational so that it can be stated that IMEC fulfilled it commitments within the STAR project.

- CEA-LETI: At the end of Year 3 it was scheduled to have 21 process tools installed and operational for users. The present situation is that 20 process tools have been installed and are operational. Tools 14 and 19 have been installed and are operational in Year 3. Related to the CEA/LE TI 300 mm strategy the process tool 16 (poly Si deposition) has not been installed. The status of the different tools has been described in detail in section 1.3.2.

- FhG-IISB: At the end of Year 2 it was scheduled to have 1 3 tools installed. Presently 9 tool are already installed and operational. For 2 additional tools the ordering has been done, but the installation will be performed in 2008. Two additional tools are presently not in the strategic investment plan. Although they will finally only 11 tools ou t fo the 13installed, this has not consequences for the STAR project. The status of the different tools has been described in detail in section 1.3.3.

Overall it can be stated that the STAR project has been successfully executed and that all initial obje ctives have been met. In total 46 new processing have been installed and commissioned before the end of the STAR project. The few process tools that have not be installed are related to strategic decisions taken by the partners in view of the changing microelectronic landscape in Europe. The continuation of STAR will be taken up in the new PRINS proposal, which is the research infrastructure associated with the ENIAC Joint Technology Initiative, and which has recently been launched within FP7.

3. USE AND DISSEMINATION OF KNOWLEDGE

The use and dissemination of knowledge during the third year of the STAR project can be summarised as follows:

1) Presentations and achievements

IMEC

- Several front-end batches of 300 mm wafers were succe ssfully completed. These batches consisted of the following devices:
    - 32 nm bulk CMOS devices
    - 32 nm SOI FinFETs
    - Batches with 32 nm strain-engineered Si devices

  All IMEC advanced development work is presently mainly running in the 300 mm process line and extensive effort has been devoted to reduce the cycle time .

- The new processing tools have been used in several of IMEC's Industrial Affiliation Programs, which are executed with 10 core partners (STMicroelectronics, Infineon, NXP, TI, Micron, Panasonics, Samsung, TSMC, Elpida, Hynix). Each of the programs also has additional partners (IC manufacturers, tool suppliers, material suppliers, software suppliers, …) from all over the world. Twice a year, a Technical Week is organized with all the partners present.

- Annually, IMEC is organizing its Annual Research Review Meeting with about 250 high-level management participants. The press is also invited to these meeting.

- Publications/ Conference presentation

  IMEC had a large number of presentations at interna tional conferences such VLSI Conference, ESSERC 07, IEDM 07, Electrochemical Society Meeting, IEEE Int. SOI meeting,etc. Some of the publications are listed below:

International Electron Devices Society Meeting (IEDM 2007) , December, Washington, USA

"Low V_T CMOS using doped Hf-based oxides, TaC-based metals and Laser-only anneal" S. Kubicek, T. Schram, V. Paraschiv, R. Vos, M. Demand, et al.

« TDDB reliability prediction based on the statistical analysis of ahrd breakdown including multiple soft breakdow n and wear-out.
S. Sahhaf, R. Degraeve, Ph. J. Roussel, T. Kauerauf, B. K aczer and G. Groeseneken

"A Dy_2O_3-capped HfO_2 dielectric and TaC_x-based metals enabling low-V_T single-metal-single-dielectric gate stack"
Y.S. Chang, L.A. Ragnarson. G. Pourtois, R.O . Conner, C. Adelmann et al.

« Gate stacks for scalable high-performance FinFETs »
G. Vellianitis, M.J. Van Dal, L. Witters, G. Curatola et al.

"Analysis of As, P diffusion and defect evolution during sub-millisecond non-melt laser annealing on an atomis tic kinetic Monte Carlo approach"
T. Noda, W. Vandervorst, S. Felcj, V. Par ihar,A. Cuperus, et al.

International Symposium on VLSI Technology, Systems and Applications (VLSI 2007), April, Hsinchu, Taiwan

"Optimization of the MuGFET performance on super c ritical-strained SOI (SC-SSOI)substrates featuring raised source/drain and dual CESL "
Collaert, N.; Rooyackers, R.; Dilliway, G.; Iyengar, V.; Augendre, E.; Leys, F.; Cayrefourcq, I.; Ghyselen, B.; Loo, R.; Jurczak, M. and Biesemans, S.

"Impact of advance d process modules and device architectures on the matching performance of (sub-)45nm CMOS"
Gustin, C.; Mercha, A.; Loo, J.; Parvais, B.; Subramanian, V.; Dehan, M.; Veloso, A.; Hoffmann, T.; Leys, F. and Decoutere, S.

"A 50nm high-k poly silicon gate s tack with a buried SiGe channel"
Jakschik, S.; Hoffmann, T.; Cho, H.; Veloso, A.; Loo, R.; Hyun, S.; Sorada, H.; Inoue, A.; de Potter de ten Broeck, M.; Eneman, G.; Severi, S.; Absil, P. and Biesemans, S

"Line width dependent mobility in high-k TiN a compar ative performance study between FUSI and TiN"
Pantisano, L.; Trojman, L.; Severi, S.; San Andres Serrano, E.; Kerner, C.; Veloso, A.; Ferain, I.; Hoffmann, T.; Groeseneken, G. and De Gendt, S.

VLSI Technology, June, Kyoto, Japan

"Achieving 9ps unloaded r ing oscillator delay in FuSI/HfSiON with 0.8 nm EOT"
Rothschild, A.; Shi, X.; Everaert, J.; Kerner, C.; Chiarella, T.; Hoffmann, T.; Vrancken, C.; Shickova, A.; Yoshinao, H.; Mitsuhashi, R.; Niwa, M.; Lauwers, A.; Veloso, A.; Kittl, J.; Absil, P. and Biese mans, S.

Novel, effective and cost-efficient method of introducing fluorine into metal/Hf-based gate stack in MuGFET and planar SOI devices with significant BTI improvement.

Shickova, A.; Collaert, N.; Zimmerman, P.; Demand, M.; Simoen, E.; Pourtois, G.; De Keersgieter, A.; Trojman, L.; Ferain, I.; Leys, F.; Boullart, W.; Franquet, A.; Kaczer, B.; Jurczak, M.; Maes, H. and Groeseneken, G.

"Highly manufacturable FinFETs with sub-10nm fin width and high aspect ratio fabricated with immersion lithography"
Van Dal, M.; Collaert, N.; Doornbos, G.; Vellianitis, G.; Curatola, G.; Pawlak, B.; Duffy, R.; Jonville, C.; Degroote, B.; Altamirano Sanchez, E.; Kunnen, E.; Demand, M.; Beckx, S.; Vandeweyer, T.; Delvaux, C.; Leys, F.; Hikavyy, A.; Rooyackers, R.; Kaiser, M.; Weemaes, R.; Biesemans, S.; Jurczak, M.; Kottantharayil, A.; Witters, L. and Lander, R.

"Strain enhanced FUSI/HfSiON technology with optimized CMOS process window"
Veloso, A.; Verheyen, P.; Vos, R.; Brus, S.; Ito, S.; Mitsuhashi, R.; Paraschiv, V.; Shi, X.; Onsia, B.; Arnauts, S.; Loo, R.; Lauwers, A.; Conard, T.; de Marneffe, J.; Goossens, D.; Baute, D.; Locorotondo, S.; Chiarella, T.; Kerner, C.; Vrancken, C.; Mertens, S.; O'Sullivan, B.; Yu, H.; Chang, S.; Niwa, M.; Kittl, J.; Absil, P.; Jurczak, M. ; Hoffmann, T. and Biesemans, S.

European Solid-State Device Research Conference (ESSDERC 2007), September, Munich, Germany

"Achieving low VT Ni-FUSI CMOS via lanthanide incorporation in the gate stack"
Veloso, A.; Yu, H.; Lauwers, A.; Chang, S.; Adelmann, C.; Onsia, B.; Demand, M.; Brus, S.; Vrancken, C.; Singanamalla, R.; Lehnen, P.; Kittl, J.; Kauerauf, T.; Vos, R.; O'Sullivan, B.; Van Elshocht, S.; Mitsuhashi, R.; Whittemore, G.; Yin, K.; Niwa, M.; Hoffmann, T.; Absil, P.; Jurczak, M. and Biesemans, S

"Demonstration of phase-controlled Ni-FUSI CMOSFETs employing SiON dielectrics capped with sub-monolayer ALD HfSiON for low power applications"
Yu, H.; Chang, S.; Veloso, A.; Lauwers, A.; Delabie, A.; Everaert, J.; Singanamalla, R.; Kerner, C.; Vrancken, C.; Brus, S.; Absil, P.; Hoffmann, T. and Biesemans, S.

"Multi-gate devices for the 32nm technology node and beyond "
Collaert, N.; De Keersgieter, A.; Dixit, A.; Ferain, I.; Lai, L.; Lenoble, D.; Mercha, A.; Nackaerts, A.; Pawlak, B.; Rooyackers, R.; Schulz, T.; San, K.; Son, N.; Van Dal, M.; Verheyen, P.; von Arnim, K.; Witters, L.; De Meyer, K.; Biesemans, S. and Jurczak, M.

INFOS 2007, June, Athens, Greece

"Reduction of the anomalous VT behavior in MOSFETs with High-k/metal gate stacks"
Ferain, I.; Pantisano, L.; Kottantharayil, A.; Petry, J.; Trojman, L.; Collaert, N.; Jurczak, M. and De Meyer, K.

"Modulation of the effective work function of fully-silicided (FUSI) gate stacks"

Kittl, J.; Lauwers, A.; Pawlak, M.; Veloso, A.; Yu, H.; Chang, S.; Hoffmann, T.; Pourtois, G.; Brus, S.; Demeurisse, C.; Vrancken, C.; Absil, P. and Biesemans, S.

CEA-LETI

- Publications/ Conference presentation.

CEA-LETI has several presentations at International Conference in the third year. Some of these presentations were based on results obtained using the 300 processing tools. The different relevant conference distributions are listed below.

54th International Symposium of the American Vacuum Society (AVS), 2007

"Tungsten and tungsten nitride etch characterization for sub 45nm metal gate"
Th. Morel, S. Barnola and O. Joubert

5th International Conference on Silicon Epitaxy and Heterostructures (ICSI - 2007)

"Low temperature growth kinetics of high Ge content SiGe in RP-CVD",
JM Hartmann

International Conference on Solid State Devices and Materials (SSDM - 2007)

"Additivity between sSOI- and CESL-induced nMOSFETs Performance Boosts"
F. Andrieux, F. Allain, C. Buj-Dufournet, O. Faynot, M. Casse, V. Delaye, L. Tosti, P. Maury, L. Vandroux, N. Daval, I. Cayrefourcq and S. Deleonibus

37th European Solid-State Device Research Conference (ESSDERC 2007)/33rd European Solid-State Circuits Conference (ESSCIRC 2007)

"Analytical and compact modelling of the I-MOS (Impact Ionization MOS"
F. Mayer, T. Poiroux, G. LeCarval, L. Clavelier and S. Deleonibus

"0.12µm P-MOSFETs with High-K and Metal gate fabricated in a Si Process Line on 200mm GeOI wafers"
C. Le Royer, L. Clavelier, C. Tabone, S. Deguet, L. Sanchez, J.M. Hartmann, M.C. Roure, H. Grampeix and S. Deleonibus

"Advanced FDSOI CMOS: the Road to 'On Diamond"
J.-P. Mazellier, O.Faynot, F. Andrieu, S. Cristoloveanu and S. Deleonibus

"Integration of CVD Silicon Nanocrystals in a 32Mb NOR Flash memory"
S. Jacob, B. De Salvo, G. Festes, S. Bodnar, R. Coppard, J.F. Thiery, T. Pate-Cazal, L. Perniola, E. Jalaguier, T. Pedron, F. Boulanger and S. Deleonibus

211th Meeting of the Electrochemical Society (ECS – 2007 Spring Meeting)

"Porous ULK using a PECVD template approach: Impact of matrix structure and porogen loading"
L. Favennec, V. Jousseaume O. Gourhant, A. Zenasni and G. Passemard

"Copper seeding and filling: New strategies for the 32 nm node "
P.H. Haumesser , A. Roule, M. Amuntencei , E. Deronzier, X. Avale, S. Da Silva, J. Klocke, R. Baskaran and G.Passemard

"Influence of annealing treatments on the morphology and electrical properties of GeOI substrates obtained by Ge condensation"
J.F. Damlencourt, Y. Campidelli, B. Vincent, C. LeRoyer, Y. Morand, T. Nguyen, S. Cristoloveanu and L. Clavelier

"Dopants contribution on nickel germanide growth: phase stability and kinetics "
F. Nemouchi, V. Carron, J.L. Labar , L. Ehouarne, M. Putero, D. Mangelinck, Y.I. Morand, S. Descombes, J.P. Barnes , Y. Campidelli, O. Kermarrec , B. Arrazat and G. Rolland

International Interconnect Technology Conference (IITC - 2007)

"Robust integration of an ULK SiOCH dielectric (k=2.3) for high perfo rmance 32nm node BEOL"
M. Aimadeddine, V. Jousseaume, V. Arnal, L. Avennec, A. Farcy, A. Zenasni, M. Assous, M. Vilmay , S. Jullian, P. Maury, V. Delaye, N. Jourdan, T. Vanypre, P. Brun, G. Imbert, Y. LeFriec, M. Mellier, H. Chaabouni, L.L. Chapelon, K. Hamioud, F. Volpi, D. Louis, G. Passemard and J. Torres

"Multi-Level Cu Interconnects Integration and Characterization with Air Gap as Ult ra-Low K Material Formed using a Hybrid Sacrificial Oxide / Polymer Stack "
F. Gaillard , L.G. Gosset, F. Gaillard, D. Bouchu, R. Gras, J. De Pontcharra S. Orain, Cueto, P. Lyan, O. Louveau, G. Passemard and J. Torres

- ***Press release***

CEA-LETI, French research integrates ultra low-k at 2.3
EE Times Europe 01/09/2007
PARIS – Long-time partners, French microelectronics research institute CEA-Leti, Crolles2 Alliance and Applied Materials , Inc. announced Tuesday (January 9) they have integrated an ultra-low k material (k=2.3) into a multi-layer structure on 300-mm diameter wafers.

FhG-IISB

- *Implementation of tutorial "Introduction to APC" at the AEC/APC conference in Dublin on 6 April 2005 and in Aix-en-Provence 27, 2006 and in Dresden April 17, 2007.*

- *ECS Satellite Symposium: Analytical Techniques for Semiconductor Materials and Process Characterization V", ALTECH 2007 joint with ESSDERC, September 13/14, 2007, Munich, Germany*

- *212th ECS Meeting: E3 - Analytical and Diagnostic Techniques for Semiconductor Materials, Devices, and Processes , Washington,DC, USA, October 7-12, 2007*

- *Japan-EU Promotion Workshop of Collaborative Research Toranomon Pastoral, Tokyo, Japan, March 26, 2007*

- *INFOS 2007, 15th biannual conference "Insulating Films on Semiconductors" Athens, Greece, June 20 - 23, 2007*

- *Forschung und Entwicklung zu Fertigungsgeräten und Fertigungsmethoden für Mikro- und Nanotechnologien – Invited Presentation at Universität der Bundeswehr München, Neubiberg, 11.Januar 2007*

- *Schmitt, H.; Frey, L.; Rommel, M.; Lehrer, C.; Ryssel, H.: UV nanoimprint materials: Surface energies, residual layers, and imprint quality, Journal of Vacuum Science and Technology B 25, 785 -790 (2007)*

- *Schmitt, H.; Zeidler, M.; Rommel, M.; Bauer, A.J.; Ryssel, H.: Custom -specific UV nanoimprint templates and life -time of antisticking layers, 33rd International Conference on Micro- and Nano-Engineering (MNE 2007), Copenhagen, Denmark: 23.-26. September 2007*

- *Schmitt, H.: Optimization of the Quartz Template Fabrication for UV Nanoimprint Lithography, 3rd FORNEL Workshop on Nanoelectronics, Erlangen, March 27 (2007)*

- *Presentation at "7th GMM YE User Group Meeting", X -Fab Semiconductors, 21 - 22 May 2007 in Erfurt*

- *ANNA Booth at "8th European Advanced Equipment Control / Advanced Process Control (AEC/APC) Conference", Dresden - Germany, April 18 – 20, 2007*

- *Presentation at "Chemical Mechanical Planarization (CMP) Metrology for 45/32 nm Technology Generations" during "Frontiers of Characterization and*

Metrology for Nanoelectronics, 27-29 March, 2007 Gaithersburg, Maryland, USA

- *Presentation "Semiconductor Equipment Assessment for NanoElectronicTechnologies (SEA-NET) - an "Integrated Project" in the 6th EU Framework Programme" at 8th European AEC/APC Conference, Dresden, Germany, April 18-20, 2007*

2) In order to allow future access to the 300 infrastructures, all three partners participated in the FP6 CA **FLYING WAFER** project, which was aimed at developing a generic concept for the transfer of 300 mm wafers between different processing facilities. The input for the FLYING WAFER model was based on the extension of the infrastructures at IMEC, CEA-LETI and FhG-IISB.

3) The continuation and future extension of the STAR project is forming part of the **PRINS** proposal, which has been submitted as part of the Research Infrastructure initiatives within Frame Work 7 launched by the European Commission. The negotiations for the Preparatory Pahse of PRINS are on going.

4) FhG IISB is a partner in a project for an Integrated Infrastructure Initiative called **ANNA** (European Integrated Activity of Excellence and Networking for Nano and Micro- Electronics Analysis). The ANNA project is a funded project to set up a collaborative, synergistic network of analytical scientists and institutions each with different but complementary competencies and analytical expertise to provide the integrated approach necessary to solve materials problems.