FINAL ACTIVITY REPORT

FRESH

FRom Electric cabling plans to Simulation Help

Contract EC AST4- CT-2005-516059

PUBLISHABLE FINAL ACTIVITY REPORT

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Coordinator:	Mr Jean-Roch GUIRESSE **ESTIA**

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FINAL ACTIVITY REPORT

Abstract

The **publishable final activity report**
describes the work performed in the FRESH Project

Diffusion List

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Executive Publishable Summary

1 - FRESH objectives

The industrialisation of an aircraft electrical harness almost relies on manual methods. When changes are needed, wiring diagrams have to be checked manually and a new harness design process has to be started to integrate modifications. CAD exchanges are also very difficult in this field (hardware/software incompatibilities).To assess electric harness behaviour, simulation is very few used and symbol recognition existing methods are not satisfactory. FRESH proposes to design a specific and innovative recognition methodology to lead to an automatic generating system.
Thus, the project is broken down in four operational objectives:

- To convert electric wiring plans into Computer Aided Design wiring diagrams language.
- To translate CAD generated wirings language into universal language.
- To adapt and improve available software to transfer wirings diagrams (universal language) into electrical harness.
- To simulate electrical harnesses physical behaviour and take benefit from simulation verification and optimisation capabilities.

And as a consequence:

- To reduce electrical harness development costs.
- To grant an error free intervention level.
- To reduce harness modification, maintenance and overhauling costs.

2 - FRESH partnership

Coordinator: ESTIA (Ecole Supérieure des Technologies Industrielles Avancées)

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3 - Work performed

FRESH comprises 7 major Work Packages, without counting WP0, which deals with management.

- **WP1** deals with **specification**: selection of an example of paper wiring diagram as base of the research, ergonomic standard for targeted harness geographical plan and envelope boundaries of wiring and harness simulation.

  WP fully achieved

- **WP2 addresses the wiring diagrams recognition:**

  WP fully achieved

  - Objectives

  As per Technical Annex, the objectives of WP2 are to research on wiring diagrams recognition, so as to fully integrate scanned paper diagrams into the whole system ; to research and implement algorithms to provide a subsystem which can be easily interfaced and integrated with the other components of the whole system. The results of the work package are therefore clearly R&D related, and can be divided into a scientific part : to research on the recognition methodology of the electric diagrams of an aircraft and a technical part which concentrates on the development of a recognition tool, which transfers paper plans in reconstructed wiring information.

  - Architecture

  The WP2 architecture is as shown in the following figure and retraces the flowchart of the global diagram recognition process : starting with a scanned wiring diagram, WP2.1 concerns image preprocessing and thresholding, providing its output to WP2.2 that concentrates on segmentation as to separate text and graphics and identify elementary graphical elements. WP2.3 and 2.4 continue on further analyzing the segmented zones, the former where text is concerned, the latter working on symbol recognition. WP 2.5 and 2.6 concern interactions with the other work packages, more particularly common knowledge presentation and software interactions.

  - **Task 2.1 Image Thresholding**

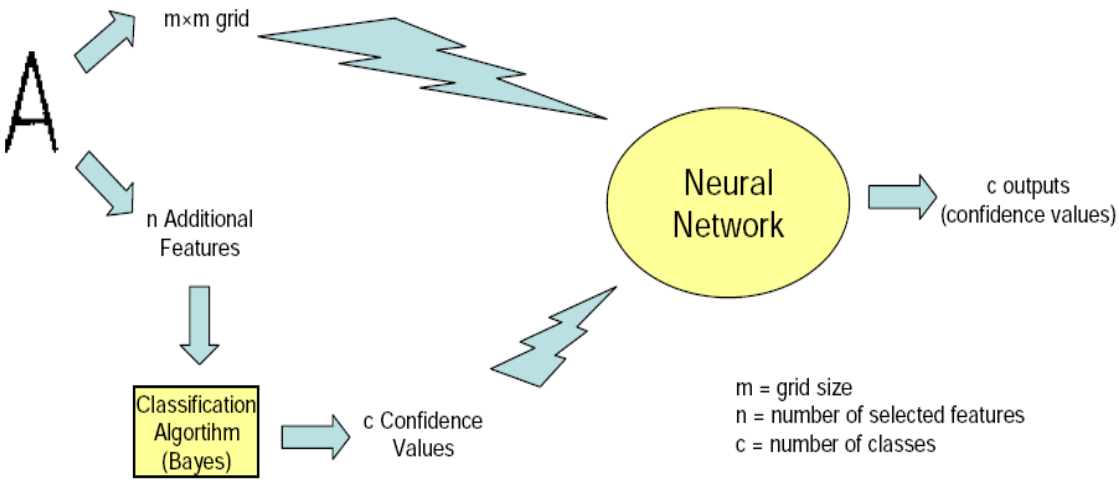
  The aim of WP2.1 is to prepare the scanned image in order to facilitate further analysis processes. It is more particularly concerned by separating the signal from the background, manage image degradations, and be adaptive to context.
  The WP2.1 thresholding method is fully described in deliverable reports D2.1.1 “Report on cleaning, thresholding and preprocessing methods” and D2.1.2 “Acquired algorithms and associated SW prototype tools”.
  It is based on the application of an initial Canny edge detection, followed by a quad-tree based dynamic thresholding algorithm near the edges, and an average propagation algorithm on more uniform zones as shown in the following representation.

- **Task 2.2 Image Segmentation**

Once the image correctly cleaned with the WP2.1 thresholding tools, WP2.2 goal is to offer tools to proceed by segmenting the resulting image in order to detect connected components, group blocks together, separate text from graphics, detect characters and do word grouping. This has been reported in deliverables D2.2.1 “Report on image segmentation” and D2.2.2 “Specification of the image segmentation method & relevant SW prototype tool”.

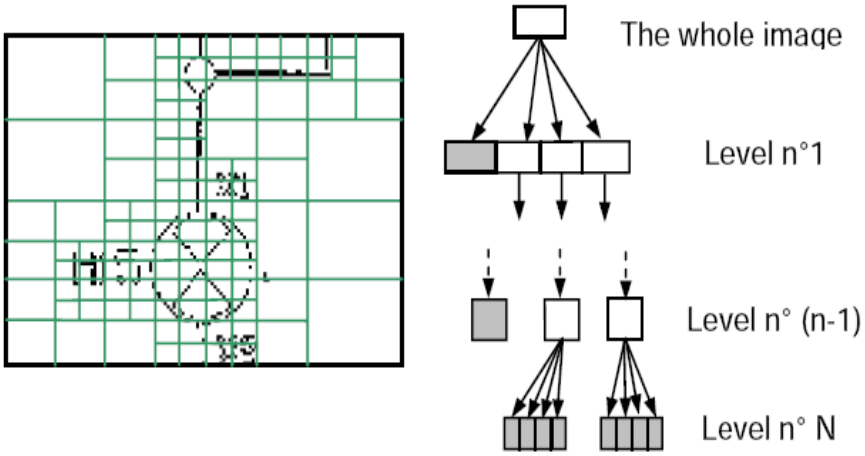
- **Task 2.3 Text Identification**

Based on results from WP2.2, giving detected and segmented text zones, WP2.3 proceeds by analyzing these zones in order to perform character recognition, word grouping and do syntax verification on the detected word zones. Research has been conducted along two distinct pathways, and has resulted into two complementary approaches.
The first approach is based on neural networks, the second combines Zernike moments with a KNN classifier and uses a confusion matrix to fine-tune results. The general architecture of the first approach is depicted below.



- **Task 2.4 Symbol Identification**

The biggest and most difficult part of WP2 concerns symbol identification. In order to achieve discrimination between ±500 symbols that are possibly very similar or very



different, that may be composed of other symbols or disconnected we have developed a two phase recognition process. The first step consists in a rapid indexing and selection process, filtering out 95% to 99% of inappropriate symbols. The second step then proceeds to disambiguate between the remaining candidates.
In order to achieve the first phase of indexing and preliminary selection WP2.4 has delivered a method based on a vector of discrete measures (Boolean or integer) where each measure consists of a robust visual characteristic. This robustness achieves to minimize influence of noise and perturbations that may subsist from phases WP2.1 and WP2.2. It is not necessarily full fault tolerant to segmentation errors, but achieves in filtering more than 95% of spurious candidates through distance minimization between descriptors.
Final disambiguation is then conducted on an ARG based structural approach combined with a genetic graph matching algorithm, published in an international workshop session GREC 2007.
The whole WP2.4 process has been fully tested and documented in the reference deliverables D2.4.2 “Symbol Recognition Process & Performance Evaluation” and D2.4.3 “Software Integration for Symbol Recognition Process”.

- **Task 2.5 Integration into CAD**

In WP2.5 analysis of the complete data structure necessary for the generation of a CAD diagram, and thus to define all the information to extract from the paper document, their format and structuring

- **Task 2.6 Design of Semantic Knowledge**

In order to correctly integrate all visual description knowledge with the physical modeling needed for further WP interaction WP2.6 has established minimal requirements for a centralized knowledge platform. It both contains all graphical knowledge for the symbol recognition process of WP2.4 (geometric composition, relative positioning of symbol parts, connectors and symbol drafting constraints) as well as the text analysis in WP2.3 such as training data for font specific OCR, relative positioning with respect to the symbol parts and all annotation syntax rules and dictionaries. Specifications are given in WP2.6 reference deliverables D2.6.3. and D2.4.4.

- **WP3** deals with the **conversion of paper or CAD wiring diagrams into a universal language (PIVOT)**.

WP fully achieved

- Objective:

Taking into account the previous problems, the main objective of the work package was defined as the research on methods and tools that would convert the different styles of wiring diagrams (Paper designs, AutoCAD and CATIA files) to PIVOT language. Once translated to PIVOT, the correspondent files would contain both the geometrical and electrical description of the mock-up and, additionally, they would have a format compatible with the modules of customization and simulation of the designs.
The benefits that with this conversion process brings will be then, firstly, that as all the wiring diagrams will be described using the same structures, we will have a homogeneous representation of the designs and, secondly, the information contained in the PIVOT structures will allow us to conduct simulation trials of the mock-ups. As we will see in the next sections, these goals have been fulfilled with success.

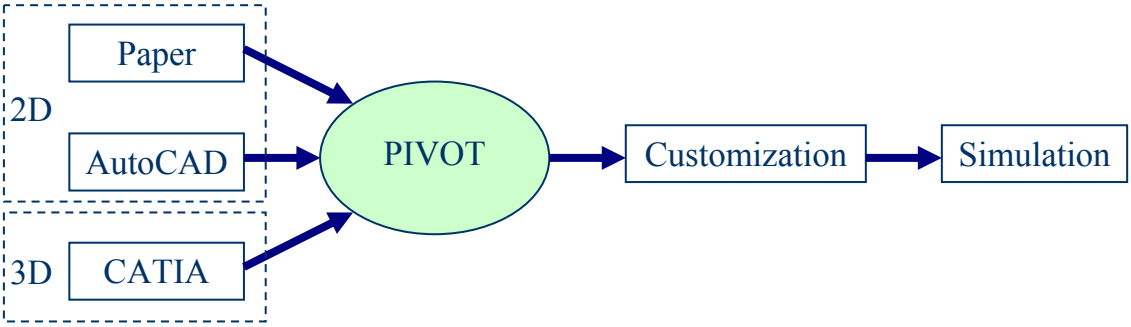


Fig.1. Diagram of the conversion process performed in WP3.

In the previous diagram (See Fig.1.) it is shown the purpose of the conversion process, but there is an element, PIVOT, that has not been defined yet. So, what is PIVOT?

PIVOT is a new intermediate language that has been developed within the FRESH project in order to represent the wiring diagrams and it has the following characteristics:

- It is able of describing the geometry and the electrical properties of the mock-ups.
- It is based on XML.
- It is produced by the recognition modules.
- It is consumed by the design and simulation modules

- Description of the tasks:

Three are the tasks in which the work package was divided in order to achieve the previous goals:

- 3.1 Envelope of styles: it consists in the identification of the elements that appear in the mock-ups described by the source documents (Paper designs, AutoCAD and CATIA files) and to point out which ones of these objects will be included among the PIVOT structures.
- 3.2 Research on converting tools: it is focused on the development of software tools that analyze the original mock-up files, extract the geometry, adds the correspondent electrical description and create the appropriate structures for storing it.
- 3.3 Universal language implementation: it is the task in which the PIVOT language is defined. Complementarily, the parsers for reading and writing the files in this format are also developed.

From these three tasks, the most difficult and important one has been the second one (Research on converting tools), because it consisted in the development of the different methods that have allowed us to analyze the different formats in which were stored the mock-ups, extract the information contained in them and enrich it through the analysis or the user interaction. As regards the other two (Envelope of styles and Universal language implementation), they have been closely related between them, because task 3.1 consists in the identification of the elements that will constitute the PIVOT language while task 3.3 defines the PIVOT language and creates the parsers for writing and reading it. These two last tasks have not been trivial and have had also its importance because the structures defined in them have determined the output of the converting software.

- **Task 3.1: Envelope of styles**

The study of the objects contained in the different formats has been completed satisfactorily. A number of geometrical objects in 2D and 3D (Points, lines, circles, arcs, …) have been identified as the generic elements with which all the geometry of the mock-ups can be represented. Complementarily, abstract objects for describing the electrical behaviour of the mock-ups have been pointed out. These structures have been later used in task 3.3 as the basis of the PIVOT language.

As regards the levels of intelligence of the different styles, it has been found that in general the representations of the mock-ups only contain a geometrical description. There are some cases, for example the CATIA mock-ups designed with the harnessing modules, in which there is additional information available, but they are exceptions.

Methods for extracting the correspondent geometrical and electrical information to a format that can be analyzed have been developed. In the previous case of the CATIA file, for example, a macro has been developed inside the CATIA framework for exporting the geometry to standard STL files, while another feature of CATIA exports the electrical properties of the mock-up elements to XML files.

In many cases, there are paper designs or AutoCAD files in 2D that complement the information contained in the 3D CATIA mock-ups. Both this circumstance and the case in which the XML files with the electrical properties are available have been taken into special consideration while developing the converting tools of task 3.2, because they allow the user to complete semi-automatically the electrical description of the mock-up.

- **Task 3.2: Research on converting tools**
  - ➔ AutoCAD: Taking as reference the work done for the paper recognition process, two tools have been developed for analyzing the AutoCAD files. The first one, AutoCAD to PIVOT converter, reads the information directly form AutoCAD files, identifies the geometric elements and generates a PIVOT file containing these data. These PIVOT files are preliminary because they do not contain electrical information about the mock-up and because the geometrical data is not clearly organised. They are then analyzed by the second application, PIVOT Editor, which offers a graphical view of the mock-up to the user where he/she can identify and classify the different elements of the mock-up. This operation adds the necessary information and helps to group the geometrical objects according to the elements of the mock-up they are part of. Then, the results are stored in PIVOT files more elaborated than the previous ones.

  - ➔ CATIA: The conversion process has been automated. An analysis of the geometry of the mock-up elements extracts the connections between them and the length of the wires which are the most important data needed for the electrical simulation of the mock-up. The interaction of the user is only needed for defining the types of the elements before performing the analysis. Any complementary data containing an electrical description of the elements may be added during this step. The definition of the types in that case would consist in an assignment between the elements of the mock-up and the IDs that appear in the complementary files.

Finally, if he wants, the user may also check the results of the analysis and adjust them.

The strategies applied to the AutoCAD files are similar to those used in WP2 when analyzing the 2D diagrams scanned from the paper designs. In the contrary, the techniques applied to the CATIA files are quite different because they study elements in 3D. Because of the differences and its innovative character, next it is given a more detailed explanation of the methodology used for analyzing the geometry of the CATIA mock-ups.

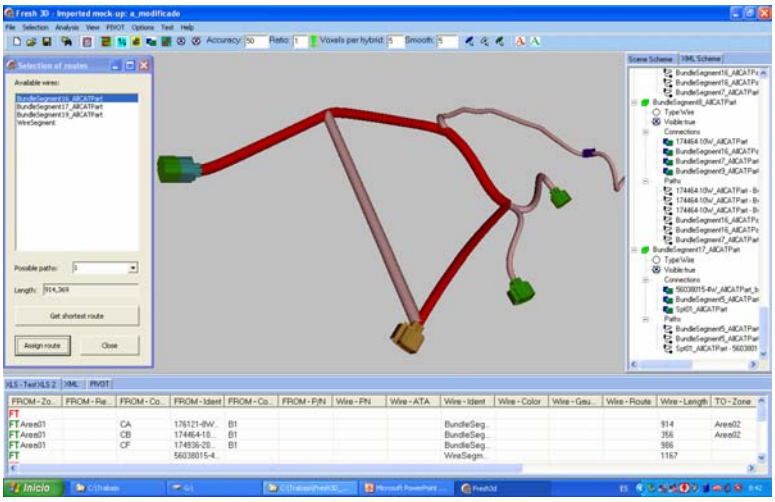


Fig.4. Screenshot of the software tool developed for converting the CATIA mock-ups to PIVOT files. In the image it is shown how the user chooses the correct wire route between the different options.

- **Task 3.3: Universal language implementation**

The PIVOT structures have been designed taking as reference the elements of the mock-ups identified in task 3.1. Once the UML diagrams of these objects have been defined the correspondent PIVOT DTD has been created.

Several versions of PIVOT have been tested in order to determine which one could contain the electrical and geometrical description of the mock-up more easily and with no loss of information. The feedback of the other project partners has been taken into account during this process. Finally, version 1.2 of PIVOT language has been validated and confirmed as the official version for the project.

PIVOT parsers for reading and writing the files have been developed in Delphi and Java. The parser in Delphi has been delivered to Algo'Tech so that it can be integrated in the WP4 software.

Due to its importance not only for this work package but also for the customization and simulation modules that will have to read their structures, the characteristics of version 1.2 of PIVOT language are briefly explained in the next section.

- **WP4** deals with the **harness numerical geographical plan**: to adapt and improve freeware to transfer wirings diagrams into electrical harness.

  WP fully achieved

  The development on the provision of the Graph Layout functionality and the Autorouting Algorithm was achieved.

  It is now possible to create the harness and to proceed, after this creation, to all operations of modification, destruction and addition to obtain the result required. The work achieved about the Harness Man-Machine Interface is:

  - the development of a graph layout algorithm to place graphical objects in a schematic automatically and in an aesthetic way.
  - the development of a routing algorithm that automatically determine the routes that polylines follow in a schematic from a source object to a target one.

  The implementation of an interface of Man Machine Interface of harness into CAD software of Algo'Tech Informatique was carried out. Some developments have been done in order to the Man Machine Interface of the harness had completely compatible with the other parts of the CAD tool.

- **In WP5 (Wiring and Harness Simulation)**, a research will be undertaken on the algorithms and models to simulate the diagrams in a factual way.

  WP fully achieved

  - Objective

  The main objective of this work package is to develop a user friendly simulator to study the electrical behaviour of components present in common aircrafts, such as harnesses and wires. To achieve this objective it was necessary to characterize the envelope and accuracy boundaries for wiring and harness elements to be modelled, to research on algorithms and implementation for dynamic event simulation and to research on the man machine ergonomics for simulation results display, simulator implementation and validation.

  - **Task 5.1 Harness components modelling**

  The main objective of this task is the modelling of the electrical components of common aircrafts in a "power consumption" point of view. For this purpose voltage and current consumption at steady state or transient behaviour would be necessary. The end user's (SOGERMA) know-how is very important in this point. Their experience in the definition of values of some electrical parameters is very useful, and helpful to decide whether some of these parameters could be neglected if their power impact was very little in the total power of the system. For this reason some meetings were arranged between CEIT and SOGERMA to exchange technical documentation about the electrical components detailed in chapter ATA-24 (Electrical Power) of some aircrafts. After these considerations about how to mathematically model the requested components, some libraries of components were created using the simulator developed by ALGO'TECH. The models were defined graphically using simpler components modelled previously by ALGO'TECH.

  Because of the problems appeared in SOGERMA during the realization of this task, there was lately a lack of an end user to provide technical information about new electrical components to model and more detailed data about the already modelled ones. For this

reason, during last months this task consisted of developing the already existing Delphi models in VHDL-AMS language. Some of these models were obtained by means of the VHDL-AMS translator developed by CEIT, based on the data structure of ALGO'TECH simulator and ".ini" files. Complex models were obtained from simpler ones according to a structural architecture of VHDL-AMS files. Other components showing an event-driven behaviour, such as circuit breakers, were developed by hand, without using the VHDL-AMS translator.
In conclusion, although not all the electrical components present in a common ATA-24 list were modelled because of the problems related to SOGERMA, the work done in this task served as a necessary input for other tasks in this project.

- **Task 5.2 User interface for Models Edition**

This task is subdivided in two tasks, 5.2.1 and 5.2.2, as follows:

- Task 5.2.1

The objective of this task is to allow user to write his own models and to modify standard models developed in the task 5.1. For this purpose, it was necessary to choose a textual modelling language to describe components behaviour. After modelling, this language would need to be checked and compiled to be understandable by the harness behaviour simulator.
After choosing VHDL-AMS, like the best modelling language for this application, a translator tool was developed to convert existing simulator models into VHDL-AMS models. These resulting VHDL-AMS models are shown in an Editor window, thus allowing end user to visualize them and to introduce some changes in their electrical characteristics if desired. In order to correct the possible changes made by the user, a lexical, syntactic and semantic analyzer was developed.
Finally, when the model written in VHDL-AMS language is correct, the model is saved in Delphi language, which is the programming language understandable by the simulator developed in this project. In conclusion, these tools allow the user to manage the models of the simulator.

- Task 5.2.2

A graphical user interface is designed and developed to allow the user of the simulator to generate models from a block diagram view and to modify the existing ones. As part of this interface, a model editor and a VHDL-AMS editor can be mentioned.
Thanks to the model editor, information about the models is shown in a friendly user interface and can be modified by the user. After converting a model into a VHDL-AMS model with the translator integrated in the simulator, this model can be visualized and modified in the VHDL-AMS editor.
The aim of the graphical user interface is to make friendlier and intuitive the management of the models of the present simulator. This interface allows the user to edit the electrical models graphically. Thanks to the model editor, the user of the simulator can define, modify or delete the model parameters or edit the mathematical expressions describing the behaviour of their internal components. Furthermore, if the user wants to edit the code of a certain model, he can do it directly thanks to the development of the VHDL-AMS editor.

- **Task 5.3 Diagram Analysis for Simulation**

The objective of this task is to analyze CAD electrical diagram, to build a net-list of components which gives a simulator friendly view of the diagram.

- **Task 5.4 Flexible Model Association to components**

To help simulation user to choose the right model or parameterization for each component.

- **Task 5.5 Specific analysis**

The objective of this task is to simulate the behaviour of electrical components using the corresponding developed models and to give accurate and fast results for users or other software.
To achieve this objective, it was studied the way to develop general electric models in order to be used also in other simulators apart from the simulator result of this project. For this purpose, it would be necessary a modelling language known by most of the users (standard) and easy to understand (intuitive) to allow users to introduce some modifications in the models if required.
Different solutions could be used, such as using binary files or custom text file format (based on XML for example), Delphi script or a standard modelling language. The last solution was chosen, using VHDL-AMS as the modelling language.

- **Task 5.6 Result display**

The objective of this task is to provide the best way to disseminate and display simulation results to user, in order to allow advanced results analysis.
In order to exploit simulation results in other environment, for reporting or technical documentation, some export functions were developed by ALGO'TECH. These functions offer to the end user of the simulator the possibility of exporting tables of values to MS Excel, charts to MS Word and electrical diagrams to various format as MS Word, PDF, html, gif, png or jpg.

- **Task 5.7 Validation**

The objectives of this task are to prove the scientific value of simulation results and the efficiency of the simulator, and to verify the ergonomics adequacy. The purpose of this validation is to determine the capability of the present simulator to fulfil the end user technical requirements. The simulation results were validated scientifically: they were compared to the theoretically expected ones, to the measurements made in some test benches and to the results obtained with other simulators. Accuracy and speed of results were estimated to define the range of validity of models and analysis modes. Not only the accuracy of the single models was tested, but also their functional behaviour as part of a complete electrical installation. Because of the problems with the initial end user of the simulator, SOGERMA, there was a lack of technical and experimental information about electrical components of common aircrafts. For this reason the validation task was focused on standard electrical components. In particular, lots of effort were done in the validation of the models of circuit breakers. These components are not considered in other simulators, so it was necessary to build a proper test bench to compare the simulated results with the real ones. After verifying and analyzing the results of the simulator, it was observed that for security reasons it is necessary to take into account the voltage drops in the cables to design properly the protections of a circuit.

The end user can define models of electrical components and edit the existing ones thanks to a friendly graphical user interface and a VHDL-AMS modelling scheme integrated in the simulator.
The multi-technological capabilities provided by VHDL-AMS language make possible the representation of non-electrical behaviour such as electromechanical devices and thermal phenomena. This feature could be very interesting in order to integrate future improvements into the current VHDL-AMS scheme, and thus, into the simulator.

- **WP6** deals with **Prototyping and Validation**

WP fully achieved

- Objective: To validate acquired technologies efficiency and industrial promises

The process of validation involved all work-packages leader, the acquired technology end user.
Validation addressed the following acquired technologies:

- Paper documents recognition process (WP2)
- Pivot language (WP3)
- Harness conception (WP4)
- Harness simulation (WP5)

The validation process had been undertaken according to two steps:
- a first step of validation from month 23 to 26 with the publication of remarks and guidance for prototypes refinements. Then guidance and remarks went to the prototyping tasks in WP2, 4, 5, which had refined the prototypes accordingly.
- A second validation step had been accomplished from month 33 to 35 using the refined prototypes.

- Paper documents recognition process validation

LORIA, CEIT, ALGO'TECH) had analysed the prototype coming from WP2.
Validation issues were on:

- Process ergonomic
- Time to full recognition
- Recognition process robustness and reliability.

- Validation of Harness conception process

ESTIA, ALGO'TECH analysed the prototype coming from WP4.
Validation issues was on:

- Friendliness and time to conceive the harness
- Information display modes accuracy and representativeness
- Adequacy of harness verification tools

- Validation of simulation process

CEIT, ALGO'TECH analysed the prototype coming from WP5. Validation issues will be on:

- Simulator human machine interface efficiency and friendliness

Results robustness and accuracy, in particular on electrical tensions and intensity and on power lost on line.

- Electrical continuity of the signals
- The linkage of events
- Modelling accuracy

The first interfaces and prototypes were presented to the end user before during San Sebastian meeting. A first complete demonstration has been done during the Bourget Air Show in Paris to the Aeronautic industrialists, Aerospace valley. The final prototype was presented during the final meeting in Nancy.

- **WP7 addresses Dissemination/Exploitation (finished)**
  WP fully achieved
  - Objective: general awareness on project results was given and the industrial exploitation of project results was prepared, validated and achieved. Dissemination of the obtained results in order to pave the way to the exploitation plan.

  - Main results: a general agreement on the final issue of PUDK has been reached by the whole FRESH partners. In terms of Dissemination, the specific FRESH page on the www.aero-scratch.net/fresh.html web site has been implemented with the summaries of all the public deliverables of the project. Moreover, technical papers have been issued and conferences have been given at the Bourget Air Show of June 2007 with presentation of the project results (display of the first prototype).

4 - FRESH achievements compared with expected results

At the end of this third year, FRESH achievements are in conformity with the expected results: they have started in the different fields of research targeted and was fully performed at the end of the project. Results have been obtained concerning:

- The setting up of a recognition system of paper wirings, further to the specification established by the end-user: adaptative thresholding, image segmentation, and symbols identifications have been achieved. Integration into CAD and design of semantic Knowledge are finished and validated. The prototype was presented during the Bourget Air Show and the final meeting.
- The development of modules necessary to reconstruct requested information related to the electrical harness: universal language (PIVOT) has been specified and the tool of conversion for CATIA files has been developed.
  The Universal Language Implementation has been also finished with the testing of the final version of PIVOT and the development of a module for saving and reading PIVOT files.
- The provision of the Graph Layout and the Autorouting Algorithm was carried out. Orthogonal algorithms and heuristics have been developed for the provision of Automatic Graph Layout. The implementation of an interface on several pages and a friendly insertion of Man Machine Interface of harness into CAD software was improved, validated and finished.
- The simulation of the harness: All models have been created using the Pack'Elec simulator developed by Algo'tech. The graphical interface and tool used to list all existing external models (models defined outside of the simulator was specified and realized.
  A VHDL Editor Interface was developed and the syntax checker for VHDL-AMS files was implemented, developed and validated by CEIT and Algotech Informatique.
  The model circuit analysis is fully specified and achieved. The new interface which allow to associate several models to a class of components has been validated.

5 - Intentions for use and impact

The first economic effects of the FRESH project will take place in 2005 yet: the project coordinator has programmed to start a first phase of industrialisation of R&D work performed in the project. This industrialisation phase will give birth to three products:

1) A product for paper schemes recognition that will be adapted to other industrial sector like schematics of vehicles (cars, buses…), boats or even industrial schematics.
2) A product for the realisation of harness, with applications in the industrial and services fields.
3) A product dealing with simulation for maintenance and training purposes.

6 - Main elements of publishable results of the PUDK

A general agreement has been approved by the consortium in terms of:

- scientific and commercial dissemination
- encouraging the implementation of the developed technologies in agreement with the FRESH consortium
- prospecting new market (inside and outside the aeronautical field)
- software and final product manufacturing

At the end of the third year, the Plan for Using and Disseminating the Knowledge has been validated by the consortium. Each partner has chosen his main exploitable results (M.E.R) and has defined the intellectual property rights for each M.E.R claimed.