

 Content archived on 2024-06-18



Formal design methods for globally asynchronous/locally synchronous embedded computing systems

Fact Sheet

Project Information

DYNAGALS

Grant agreement ID: 220146

Project closed

Start date

1 March 2008

End date

28 February 2010

Funded under

Specific programme "People" implementing the Seventh Framework Programme of the European Community for research, technological development and demonstration activities (2007 to 2013)

Total cost

€ 111 667,01

EU contribution

€ 111 667,01

Coordinated by

INSTITUT NATIONAL DE
RECHERCHE EN
INFORMATIQUE ET
AUTOMATIQUE

 France

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Objective

We propose a novel approach to tackle the design-productivity gap existing in the field of complex and heterogeneous embedded computing systems. We take as a starting point the SystemJ programming language, which combines the data processing and encapsulation elegance of Java with with the reactivity and synchrony of Esterel and the asynchronous decoupling of CSP (that is, with rendezvous communications). Our research proposal aims at improving SystemJ in two directions: first for the formal verification of SystemJ programs, and second for the automatic synthesis of hardware/software embedded code. An implementation within a complete tool is also planned. These two goals will help SystemJ becoming one of the leading system-level design language for complex and heterogeneous embedded systems. The first goal (formal verification) is essential for the validation of the system under design. As embedded computing systems are often safety-critical, formal verification is a crucial feature for a system-level design tool. We shall use observer-based model-checking, with state-space reduction techniques. The second goal (code synthesis) is crucial too because it avoids the tedious and error-prone phase of manual coding from the high-level specification. Instead, we shall be able to generate automatically a mixed hardware and software implementation, proven to be faithful to the high-level specification written in SystemJ. Such a proof of faithfulness shall be based on the formal semantics of SystemJ. These scientific research results shall be implemented within a tool suite, and we shall conduct case studies to evaluate its practical usefulness for the design of embedded systems as well as its performances.

Fields of science (EuroSciVoc)

[natural sciences](#) > [computer and information sciences](#) > [software](#)

[natural sciences](#) > [computer and information sciences](#) > [data science](#) > [data processing](#)

Keywords

[Automated code synthesis](#)

[Computer engineering](#)

[Embedded systems](#)

[Globally asynchronous locally synchronous systems](#)

[Model checking](#)

[Programming](#)

[Programming languages](#)

[Software technology](#)

Programme(s)

[FP7-PEOPLE - Specific programme "People" implementing the Seventh Framework Programme of the European Community for research, technological development and demonstration activities \(2007 to 2013\)](#)

Topic(s)

[PEOPLE-2007-4-1-IOF - Marie Curie Action: "International Outgoing Fellowships for Career Development"](#)

Call for proposal

FP7-PEOPLE-2007-4-1-IOF
[See other projects for this call](#)

Funding Scheme

[MC-IOF - International Outgoing Fellowships \(IOF\)](#)

Coordinator



INSTITUT NATIONAL DE RECHERCHE EN INFORMATIQUE ET AUTOMATIQUE

EU contribution

€ 111 667,01

Total cost

No data

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Activity type

Research Organisations

Links

[Contact the organisation](#)  [Website](#) 

[Participation in EU R&I programmes](#) 

[HORIZON collaboration network](#) 

Last update: 16 July 2019

Permalink: <https://cordis.europa.eu/project/id/220146>

European Union, 2025