High Quality European GaN-Wafer on SiC Substrates for Space Applications

Berichterstattung

Projektinformationen

EUSIC

ID Finanzhilfevereinbarung: 242360

Projektwebsite

Projekt abgeschlossen

Startdatum
1 November 2010

Enddatum
31 Oktober 2013

Finanziert unter
Specific Programme "Cooperation": Space

Gesamtkosten
€ 3 282 694,02

EU-Beitrag
€ 1 989 426,00

Koordiniert durch
SiCrystal AG
Germany

Dieses Projekt findet Erwähnung in ...

MAGAZIN RESEARCH*EU

Wasser des Lebens: Verwüstung, Zugang zu sauberem Wasser

Final Report Summary - EUSIC (High Quality European GaN-Wafer on SiC Substrates for Space Applications)

Executive Summary:
The main objective of the project „High Quality European GaN-Wafer on SiC Substrates for Space Applications" (EuSiC) was the development of high quality semi-insulating 3 inch SiC-substrates, which are superior to that available from non-European sources. The development activities covered the entire value chain including crystal growth-, wafering-, epitaxial-, and device/component-related topics.

The composition of members of the consortium was aiming to evaluate the complete process-line from along the typical supply chain from substrate to device. Thus the internal feedback loops as well as the external feedback-loops between project partners were the most important tools for examination and improvement.

The main development workload was located at SiCrystal. A new high quality crystal growth process for 3 inch semi-insulating SiC substrates had to be developed. Necessary feedback loops were activated with time, starting at wafer manufacturing level and extending over time to device level. This stepwise approach ensured involvement of the following processes at an appropriate point in time to verify the new developments. The final GaN-device quality feedback served as a verification of the resulting quality of the complete supply chain and thus granting the successful realization of substrate and epitaxy quality goals. The participating epi-houses were working in parallel, so that a broader coverage of technology variants and process spread due to specific differences in epi-reactor technology could be screened.

The data of s.i. SiC substrates and later epi and device process steps were reviewed at the mid of the project time and finally at the end of the project. The analysis of the data included cross-correlations of different properties as well as investigations on the distribution of all properties, including detailed analysis of individual results where appropriate. In this way, key parameters and characterization properties were identified and irrelevant parameters could be dropped. The origin for deviations from the project partners' expectations was traced and conclusions for the next wafer and epi-wafer shipment to project partners were drawn. For verification of the specification a set of "golden" wafers was identified on the basis of device performance. In this way each a specification for bare wafers as well as epitaxial wafers was established.

These specifications represent the final result and achievement of this project. The verification of the specification for the complete process line for semi-insulating 3inch SiC wafers to high power GaN HEMT components has been successfully executed. Redundancies and irrelevant properties could be removed from the specification within the framework of this project. Device performance as reported by project partner UMS also including epi and device benchmark data was used as an indicator for the judgement of specifications. A multitude of process parameters and inevitable process fluctuations were checked successfully, only being limited by capacity demand. Further fine optimizations within a productive scenario with better statistical preconditions seem appropriate. As main improvements updates for the specifications for wafer and epi-wafer geometry, epi-layer sheet resistance and epi-layer Al-content are to

be mentioned.

As a final result the project accomplished to demonstrate state of the art device performance as well as verification and in some parts further optimization of process parameter specifications for the main supply chain interfaces at substrate and epi-wafer level. Main topics for a future (industrial) use of these specifications should include several economic optimisations in the implementation in terms of yield and process stability.

EuSiC has significantly reduced the dependence on critical technologies and capabilities from outside Europe for future space applications by establishing an independent, purely European sustainable chain for Gallium Nitride (GaN) based space technologies. Final target of the project was to provide 3 inch semiinsulating SiC substrates having a quality which is superior to that available from non-European sources. During this project European high quality semi insulating SiC substrates were developed by SiCrystal which are equal or better than the non-European substrates. Devices based on AlGaN/GaN epi layers with structural and electrical properties close to the corresponding data on Cree substrates were achieved
Project Context and Objectives:
There is a significant European activity in GaN-based power microwave devices for space applications, which extends from epitaxy through device fabrication to a diverse range of circuit demonstrators. However, access from a European supplier to the substrate of choice, namely semi-insulating 3 inch SiC was restricted at the beginning of the project. The leading manufacturer of SiC substrates CREE is located in North America and substrate supply is exposed both to risks due to international politics which led to US export restrictions as well as to technical risks by a dependency on a supplier who is committed primary on his own device strategy.

Before the EuSiC project, neither 3 inch nor 4 inch (100mm) diameter semi-insulating SiC substrates were available from a European source. Thus the intention of this project was to improve the quality of semi-insulating SiC substrates at SiCrystal AG, the leading manufacturer of SiC substrates in Europe. The provided substrates have been analyzed and evaluated by epi-growth specialists IAF, III-V-Lab, and Linköping University (LiU). Finally, devices have been built and verified on the created GaN epi-wafers by UMS.

The project „High Quality European GaN-Wafer on SiC Substrates for Space Applications” (EuSiC) aimed at establishing an independent, purely European sustainable supply chain for Gallium Nitride (GaN) based space technologies.

Three project main goals were identified as follows:
- First, development of high quality 3 inch semi-insulating SiC substrates.
- Second, bringing together all parts of the supply chain namely, substrate manufacturer, epitaxial houses and a MMIC foundry.
- Third, verifying a completely European source of GaN devices on semi-insulating SiC, which is superior to that available from non-European sources.

The composition of members of the consortium as well as obvious technical advantages strongly

suggested structuring the work packages and their interaction along the typical supply chain from substrate to device.
The main development workload was located at SiCrystal. A new high quality crystal growth process for 3 inch semi-insulating SiC substrates has been developed. Necessary feedback loops were entered with time, starting at process level and extending over time to device level. This stepwise approach ensured involvement of the following processes at appropriate time to verify new developments. The final GaN-device quality feedback approved the resulting quality of the complete supply chain and thus verified the successful realization of substrate quality goals.
The participating epi-houses have been working in parallel, so that a broader coverage of technology variants with specific differences in epi-reactor technology could be screened.
This architecture allowed for precise feedback at appropriate time thus accelerating overall development speed.

The work plan was distributed among a total of five technical work packages and two non-technical work packages. It was taken into account that there were different organizational and structural fields of activities.

WP 1: Crystal quality (SiCrystal)
WP 2: Geometry and surface quality (SiCrystal)
WP 3: Quality assessments and inspecting methods (SiCrystal, IAF, LiU, III-V Lab,
UMS)
WP 4: Epitaxial growth (IAF, LiU, III-V Lab)
WP 5: Device manufacturing and evaluation (UMS)
WP 6: Dissemination and use (SiCrystal, IAF, LiU, III-V Lab, UMS)
WP 7: Management (SiCrystal, IAF, LiU, III-V Lab, UMS)

WP1 - Crystal Growth
WP1 addressed the development of a high quality crystal growth process for semi-insulating SiC substrates. The development was based on growth processes available for high quality conductive material. Main focus for quality development was set on micropipe densities and crystallographic orientation homogeneity, which is relevant to improve single crystal mosaic structure.
The development was permanently monitored and verified by quality feedback on substrate, epi and device level in WP3 to WP5. The guiding material specification has been revised in WP3 during the course of the project on the basis of this quality feedback information.

WP2 - Geometry and Surface Quality
WP2 addressed the substrate surface preparation processes at SiCrystal to provide 3” semi-insulating SiC wafers with superior geometry and surface quality to the epi-houses III-V-Lab, IAF and Linkoping. To achieve this goal, this work package was divided into tasks, addressing optimization of geometry (wafer shape parameters) and high-end surface quality by chemical-mechanical polishing (CMP). Experience on surface finishing of conductive SiC-substrates at SiCrystal was the basis for this development.

WP3 Quality Assessment and Inspection Methods
In WP3 missing methods were established for improved quality feedback at SiCrystal for semi-insulating

SiC substrate characterization and quality feedback data at the various check-points for quality and characterization was provided.
The epi-ready substrate resulting from WP1 and WP2 at SiCrystal was characterized routinely with a standard set of production level measurements that are approved for conductive material, including: wafer shape, x-ray orientation homogeneity, surface roughness, crossed-polarizer analysis, visual classification of defects (e.g. planar defects, macro defects, grains, cracks, scratches) and microscopic inspection for structural defects.
Missing methods specifically needed for 3 inch semi-insulating SiC substrates at SiCrystal were provided by the project partners.

WP4 Epitaxial growth
The objective of WP4 was the monitoring and verification of substrate quality development in WP1 and WP2 by evaluation of the substrate quality through the growth and characterisation of GaAlN/GaN HEMT heterostructures. Benchmarking with commercially available substrate material and SiCrystal's semi-insulating SiC substrates supported the quality assessment.
All epi-houses evaluated the quality of the 3-inch semi-insulating SiC substrates delivered by SiCrystal, by a standard and quality proven HEMT structure that will be grown on top of the wafers. Reference substrates from a commercial US SiC supplier will be used in the same epitaxial run for comparison.
Standard characterization techniques were as following: optical microscopy, contactless sheet resistance mapping, wafer curvature measurement, Hall-effect, ellipsometry, x-ray diffraction, atomic force microscopy, secondary ion mass spectrometry.
The overall objective of the assessment and inspection methods used to assess the insulating SiC is to establish criteria which can be used by all parties (supplier and user) to quantitatively define what is acceptable / not acceptable and drive development / improvement of the insulating SiC. Ultimately such criteria need to be related to the impact on device performance and impact on the epitaxy process and thus it is critical that the substrate assessment criteria are characterised both by their impact on the epitaxy and the device performance (yield and reliability).
The parallel involvement of three epi-houses allowed for an accelerated development and offered the opportunity to verify the substrate quality and process chain stability by different epi-reactor concepts and device parameters.

WP 5 - Device Manufacturing
In WP5 the quality and performance of GaN epi-wafers based on the new semi-insulating SiC substrates was evaluated by device manufacturing. Using an industrial GaN process (as developed at UMS) provided useful information about the manufacturability of GaN devices and MMICs with enhanced reliability.
Within this work package more than 40 GaN-wafer were processed coming from the different institutes (IAF, III-V-Lab, LiU) performing the epitaxial growth in two iterations throughout the project.
The material was inspected, processed and finally analysed. A standardized incoming inspection, as being done for material from other industrial suppliers, was performed. This includes analysis of structural crystal properties, mechanical, optical and electrical characterisation.
Afterwards the GaN epi-wafers were fully processed in the UMS GaN manufacturing line. UMS chose suitable mask sets coming from other UMS projects/activities. Dependent on the epi-process chosen (GH50/GH25), the mask set contained process control monitors (PCM) and devices/MMICs. The PCMs

are standardized and can be therefore easily used for statistical analysis of wafer performance, quality, homogeneity and comparison to other industrial material. Through the in-line testing of DC and RF parameters (I2, I3, I5), the wafer processing was fully monitored.
After finalization of the wafer processing additional electrical characterizations were performed as load-pull and pulsed S-parameter characterization. This allowed the assessment of the electrical performance which can be achieved on this new high quality European GaN-wafers. Furthermore, on-wafer reliability and storage tests were performed on these wafers to check the long term stability of the devices. The tests have been performed on PCM structures only due to the limited time and resources.

WP 6 - Dissemination and Use
The EuSiC project aimed at developing and establishing a new European SiC substrate source for GaN wafers to be used for space applications, with opportunities to expand to other kinds of applications. For the establishment of a European market for this material, it was vital to openly communicate the status and the achievements of the project to others. This was done by scientific publications and conference contributions mainly in the 2nd half of the project.

WP7 Management
WP7 focused on Management and Administration including financials and progress reports.
Project Results:
1. Material development
During the first project year the re-launch of semi-insulating crystal growth and preparation process at SiCrystal was successfully accomplished and a first quality improvement campaign was started. The fraction of high resistivity wafers in a crystal (> 1E5Ωcm) could be improved to a value significantly higher than 90%.
Several crystals showed over the complete length or in the upper half grains with a different crystallographic orientation. Also modification changes were observed, which can act as source for micropipes.

The main results from the first project year were:
Material quality of delivered crystals at least met, but in some cases exceeded the required quality by far.
Geometrical values (Warp, Bow, TTV) of manufactured and delivered wafers were much better than specified in the Description of Work.
Surface roughness RMS of manufactured and delivered wafers was also much better than specified in the Description of Work. Typically values of 1nm and < 0.7 nm were achieved.
For full area MPD detection an automated non-destructive detection method was identified as method of choice to measure reliable MPD-values.
Quality of SiC substrates from SiCrystal was already very close to commercially available substrates from Cree.
The SiC substrates were analysed and compared to Cree SiC substrates for benchmarking. The crystallographic quality checked in X-Ray Omega scan and optical cross polarization imaging was good and comparable to Cree wafers.
GaAlN/GaN HEMT structures were grown for substrate evaluation. The crystallographic quality and the surface morphology of such HEMT structures were very good compared to the results obtained on Cree substrates.

Observations:
The surface roughness of the substrates was found to have an impact on the electrical properties as mobility, sheet resistance or pinch-off voltage of these grown HEMT structures.

During the second project year a new seed generation with larger diameter and significantly lower orientation deviations at the wafer rim was developed. The orientation deviation at the wafer diameter is close to zero and even at the seed-rim the values are below the target value 0.3°.
Semi-insulating wafer crystal growth was performed using seeds with larger diameter and improved orientation-homogeneity.
Electrical substrate characterization was done with a COREMA system for contactless resistivity mapping on 32x32 points across the entire wafer area. Minimum resistivity of 1E7 Ωcm is required to achieve good sheet resistance of the HEMT structure.
The 3inch semi-insulating SiC substrates showed a very high mean bulk resistivity larger than 1.0E11 Ωcm with good homogeneity.
The structural properties of the 3 inch semi-insulating SiC substrates were investigated by a crossed polarizer system, which allowed qualitative analysis of lateral stress distribution of a whole substrate. The high quality of the substrate was confirmed by the low contrast given by the crossed polarizer image, which was free of any grains and modification instability. Additionally, X-ray omega scans were conducted to verify the structural homogeneity of the substrates. Achieved FWHM values, calculated from the X-ray rocking curves, were close to the resolution of the equipment.
The micropipe (MP) density was determined using an automated optical microscope (pattern detection on transmission mode). Micropipes are a well-known silicon carbide specific defect, with a high impact on device quality. Only single micropipes were found on the substrate area. The average MP density of substrates grown in the second project year was significantly lower than 1 cm-2 .
Based on the feedback to substrate surface quality, a chemo-mechanical polishing (CMP) process step for semi-insulating SiC was developed. The surface morphology of the substrates was analysed using AFM technique. All scratches from the mechanical polishing step could be removed. The surface roughness could be reduced from 1.5nm to 0.2nm.
In the second project year, all of the three epi-houses received five (milestone 1) + ten (milestone 2) 3 inch s.i. SiC substrates from SiCrystal. These wafers have been characterized directly after delivery with respect to their structural, electrical und morphological properties and compared to commercially available Cree substrates.
A high electron mobility transistor (HEMT) structure has been grown on 3inch semi-insulating SiC substrates prepared during the first project year. The barrier and the cap layer of the HEMT structure consisted of a Al(18%)Ga(82%)N barrier and a GaN cap. The epitaxial layers were characterized with respect to their electrical, morphological and structural properties. Feedback on the substrate quality and the impact on the epitaxial growth has been transferred to SiCrystal for improving the next development cycle of s.i. SiC substrates.
The barrier thickness and composition was determined by high-resolution x-ray diffraction in conjunction with dynamical simulations. The growth conditions of the AlN nucleation layer and of the GaN buffer were optimized for a low dislocation density (low 1E8 cm-2 range as determined by plan-view transmission electron microscopy), smooth surfaces (root mean square roughness well below 0.2nm over an 2×2µm2 area and low carrier concentration in the buffer and high buffer isolation (above 1E12 Ω/sq)). Differences in the high-resolution x-ray diffraction Omega-scan 00.2 and 10.2 GaN linewidths were observed, namely

around 0.04° and 0.03° in the (002) reflection and 0.05° and 0.07° in the (102) reflection for Cree and SiCrystal substrates, respectively. Probably this difference was due to the different nucleation on 4H and 6H substrates.
The qualified GH50-10 GaN HEMT Technology was used to evaluate the quality of semi insulating 6H SiC manufactured by SiCrystal during the first project year (milestone 2). The investigation program comprised incoming inspection, GaN-component manufacturing and device characterization of the epi wafers. In addition, a benchmarking of the European epi wafers to UMS qualified epi wafers with regard to UMS GH50-10 technology specifications was performed. Device manufacturing of 18 epi wafers at UMS (Milestone 2 delivery) created by the three epi-partners III-V Labs, Fraunhofer and Linköping have been successfully performed. All 18 epi wafers, 13 manufactured on SiCrystal SiC substrates and 5 epi wafers manufactured on Cree substrate exhibited generally good results.
The sheet resistance was in the expected range or very close to the specification limits except two wafers (epi from IAF and 3-5Lab, respectively).

From trend charts for the drain source current at Vds=10V, Vgs=+1V in mA/mm a spread of Ids_plus on a wafer and from wafer to wafer was observed. The wafer to wafer variation was obviously caused by the fact that different substrate and/or epitaxy runs have been processed in one lot.

More frequent growth of the UMS GH50-10 epi wafer specification will certainly improve in the future the uniformity of important device parameters.
Output power parameters were measured using two different Output matching conditions.
After device manufacturing and characterisation of 18 wafers, including 5 wafers on Cree substrates, transistor results obtained on SiCrystal substrates were equivalent to those results obtained on commercial reference substrates from Cree.

The main results from the second project year were:
The structural quality was significantly improved and close to target of specification update. Overall defect density was comparable for SiCrystal and Cree substrates. Substrate resistivity of SiCrystal and Cree substrates was at a very similar level. The geometry of SiCrystal substrates themselves were considered to be at least as good as Cree substrates.
There was no difference between surface roughness of HEMTs on Cree and SiCrystal substrates (AFM).
The large area surface morphology was similar to that of HEMT structures grown on Cree substrates (optical inspection).
Contactless measurements of the mobility and sheet carrier concentration revealed similar values for HEMTs on Cree and SiCrystal substrates (Hall measurement).
No specific difference between HEMT structures on Cree and SiCrystal could be observed. Differences were mainly due to the different Al content of the layers (CV profile).
Transistor results obtained on SiCrystal substrates were equivalent to those results obtained on commercial reference substrates from Cree.
The lagging behaviour of IAF epi wafers was similar to UMS standard wafers.
The measured Pout values were between 2.5 and 5.5 W/mm.
WLR HTRB tests were performed.

Observations:
FWHM of the SiC peak of Cree substrate was smaller and more homogeneous across the substrate than for SiCrystal wafers (bulk property).
There was higher strain on SiCrystal substrates (cross polarization imaging).
There might be an influence of substrate quality on sheet resistance.
Al content in the AlGaN layer was different for different substrates, therefore the Rsheet differed.
The line width of the symmetric 002 GaN reflection was significantly increased for HEMTs on Cree substrate. At the same time the asymmetric 102 reflection was significantly smaller for these wafers in comparison to SiCrystal substrates (XRD line width).
The sign and the amplitude of the wafer bow after epitaxjal growth could be concave and convex, independent of the substrate supplier. No specific difference between Cree and SiCrystal could be observed (wafer bow).
The specification of the HEMT structures had to be specified for each epi source to achieve same quality level of GaN device performance.
The measured Pout values W/mm depended on the epi wafer supplier.
At WLR HTRB tests have shown Schottky degradation in backward and forward direction.

Quality of crystals produced during the second project year surpassed the current specification as well as the not yet released final specification at end of project. Thus, a very good crystal quality could be demonstrated. However, overall wafer yield was not as high as demanded by an industrial production process. Therefore, during the third project year, an improved process for crystal growth was established to achieve an increased yield while keeping the crystal quality on the high level achieved in the first two project years.

The achieved electrical resistivity of the grown crystals complying with the target specification of >1E10 ?cm was again excellent.
The substrates of 4 crystals were investigated by using the micropipe recipe for the automated optical microscope. Micropipe density (MPD) and MPD defect area histograms were investigated. All of the investigated had a MPD significantly below 1 cm-2 (specification limit of milestone M11). For additional verification purposes a manual verification was done on sampling basis.
The overall yield of high quality wafers could be improved from 35% to 52%. Also, in the new growth process, the significant improvements demonstrated for crystals grown in the second project year in comparison to crystals grown in the first project year could be maintained.
After process development, four crystals were grown and processed to prepare 21 substrates for epitaxial growth.
In crystal preparation, the multi-wire sawing step and in double-side polishing we took care to preserve the stable process conditions we achieved during the previous delivery. From the four process variations implied in the second project year and tested at the three epi-houses, one process sequence made it possible to grow epitaxial layers close to Cree benchmark. Therefore, this process has been used as starting point for the developments done for the wafers processed in the third project year. After polishing, a dry etching step was performed. The main targets of the work during the development were to achieve a) high material removal, b) final surface roughness <0.25 nm Ra and c) very low subsurface damage for the CMP Process.

Concerning the surface roughness, a significant improvement was achieved. The average roughness Sa-Value has dropped by approx. 46% from 0.430nm in the second project year to 0.233nm in the third project year. SiCrystal's improved CMP process has also proven to be very stable in terms of wafer to wafer roughness reproducibility and generates very homogeneous scratch-free wafer surfaces, too. The overall SiCrystal CMP quality exceeds expectations and is at the same level as the well-known Novasic 100mm SiC-CMP process.
It is expected that sub-surface damage caused by mechanical polishing of the substrates has a negative influence on the quality of the epitaxial layers. SiCrystal has developed a destructive method to reveal and quantify sub-surface damage on polished SiC surfaces. This method consists of two steps: The first step is based on etching in molten KOH with a special recipe. The basic idea is to remove structurally damaged material close to the surface and thereby converting the inhomogeneous damage layer into a surface morphology which can be evaluated quantitatively.
The second step comprises the quantification of damage thickness by surface roughness measurement using an optical profilometer. Care has to be taken that unavoidable selective etching (formation of etch pits) is excluded from the evaluation. The resulting roughness value (Rt) is corrected to reflect quantitatively the thickness of the revealed damage layer. The resulting image after damage-etching gives additional information about the lateral structure and often allows conclusions concerning the origin of damage.
Measurement of surfaces showed that we could improve the damage layer to < 0.35 nm during the third project year.
Final quality inspection results showed that quality meets the specified values for all geometry parameters but for Bow and Warp. The average Warp value is 10.4µm and slightly above the targeted max. value of 10µm. The average Bow value is 4.96µm and below the specified 5µm. As the geometry values were still close to the target specification no negative influence on the epi-process in WP4 was anticipated. The surface roughness average was 0.233nm Sa and was well below the target value of 0.35nm.
In the third project year, each of the three epi-houses received again ten 3 inch s.i. SiC substrates from SiCrystal, which originated from 4 different SiC growth boules. Also 4 different surface polishing finishes have been used to prepare the epi wafer surfaces for comparison. These wafers have been characterized directly after delivery with respect to their structural, electrical and morphological properties and compared to commercially available Cree substrates. Subsequently, a HEMT structure consisting of an isolating GaN buffer, a 22nm thick barrier layer with nominally 18% Aluminium and a 3nm thick GaN cap has been grown by MOCVD on SiCrystal s.i. SiC substrates and benchmarked to Cree substrates. The epitaxial layers have been characterized with respect to their electrical, morphological and structural properties.
Different strain states of the AlN and GaN layers have been detected depending on the polishing procedure. The reason for this observation is not clear yet but it is assumed that the different surface polishing procedures resulted in a different terrace structure of the individual substrates, thus providing different interfaces of the substrate and the AlN nucleation layer. The overall dislocation density of the epi layer based on omega-scans in two configurations tended to be the same for HEMT structures on Cree and SiCrystal substrates.
The sheet resistance tended to be slightly lower for HEMT structures on Cree than on SiCrystal substrates due to different Al incorporation. We observed a higher Al-content and thinner AlGaN layers on Cree substrates leading to the lower sheet resistance on these substrates. Probably the thermal conductivity between 4H-Cree-SiC and 6H-SiCrystal-SiC is slightly different. In fact, we have measured slightly different thermal conductivities of 420 and 400Wm-1K-1 for Cree and SiCrystal substrates. The overall

trend of sheet resistance vs. Al-content was the same for Cree and SiCrystal substrates which suggests that apart from the different Al-incorporation the electrical properties of the two-dimensional electron gas at the AlGaN/GaN interface remains the same for Cree and SiCrystal substrates.
The morphology of the epi wafer surface for Cree and SiCrystal was the same. Clearly atomic terraces were observed indicating also smooth interfaces.
The electrical properties of the buffer were examined using Hg-profiling of the depth dependent carrier profile. The background carrier concentration on both types of substrates was as low as 1012 cm-2.

For the wafer fabrication the qualified UMS GH50-10 process has been used. The GaN epi wafers have been grown by MOCVD on s.i. SiC substrate manufactured by SiCrystal by epi partners Fraunhofer IAF, ATL 3-5Lab und University Linköping. For comparison and device benchmarking epi growth on Cree substrates was performed. In order to compare the GaN HEMT devices Load-Pull and lagging testing were performed. Results from wafer level reliability testing will also be reported.
The quality of the SiCrystal semi insulating SiC substrates was very promising and in fact AlGaN/GaN epi layers with structural and electrical properties close to the corresponding data on Cree substrates were achieved. Deviations of GH50 component performance comparing qualified Cree epi wafers were rather related to the epitaxy quality than to the substrate quality. In addition we have to take into account that even for the GH50-10 qualified technology on qualified Cree epi wafer we observe form time to time for example too high leakage current.

The summary of the component results obtained on SiCrystal s.i. SiC substrates is:

4 wafers from IAF fulfilled all electrical specifications, but the Schottky diodes were not stable and the lagging is slightly too high.

The Cree reference wafers exhibited a problem with a high leakage current and the Schottky diode was not stable too. Output power and lagging were as required.

Linkoeping wafers had not enough output power, but the HTRB wafer level reliability results and the leakage current up to Vd = 150V were good.

Leakage currents of 3-5 Lab wafers were in UMS specifications at Vd = 50 V, but not in UMS specification at Vd = 150 V. The Schottky diode stability was improved compared to the IAF and Cree epi wafers. Only one wafer on SiCrystal substrate showed the required output power of 5.5 W/mm. Power measurements were performed on 9 of 12 manufactured wafers.

The summary regarding power measurements, lagging and HTRB tests is:

The measured Pout values were between 3 and 6.1 W/mm depending on the epi wafer supplier. For standard GH50-10 wafers Pout was about 5.5 W/mm.

The lagging behaviour of IAF epi wafers was slightly higher to UMS standard wafers. For epi wafers from Linkoeping University the lagging was increased. The highest lagging values were measured on wafers with epi from 3-5 Lab.

The WLR HTRB tests showed for the selected epi wafers (1 from University Linkoeping and one IAF on Sicrystal SiC substrate) Schottky degradation in backward and forward direction. The Linkoeping wafer was more affected.

The cascade HTRB tests (21 devices per wafer; testing devices with 4mm gate width) showed different results with more measured devices and harder stress conditions on the wafer. 16 stressed devices on the reference wafer degraded in reverse direction (gate leakage increase) and 5 also in forward direction (local reduction of the Schottky barrier). This is not a good reference.
All 4 measured wafers from IAF showed non stable Schottky diodes. The behaviour is equal to the observations on the standard wafer, all device degraded in reverse direction showing increasing of the gate leakage current.
The 4 measured 3-5 lab wafers showed more stable Schottky diode behaviour. For 3 wafers 7 of 21 devices degraded and for one wafer 10 of 21 devices degraded (for 9 devices gate leakage current increased; 1 device had a bad diode characteristic before the stress).
The other 3 wafers showed only an increasing of the gate leakage current.
The wafers with the most stable Schottky diode characteristics were wafers with epi from Linkoeping. 2 of 3 wafers showed very stable Schottky diodes, for one wafer 8 of 21 devices degraded.

The main results from the third project year were:
Yield of high quality wafers could be increased from 35% to 52%.
The structural quality was significantly improved and close to the target of the specification update.
A characterization method for the evaluation of sub-surface damage was established to monitor the development of an improved CMP-process (target: nearly damage-free surface).
The CMP polishing of the SiCrystal substrates was improved a lot since the beginning of the project. The surface roughness is comparable to the surface roughness of the reference Cree substrates.
The improved CMP procedure showed a very good damage depth close to zero.
All SiCrystal wafers had lower TTV (Total Thickness Variation) compared to Cree substrates.
Crystallographic quality and surface morphology quality of HEMT structures grown on SiCrystal substrates were good and well comparable to the epi-layers grown on SiC Cree substrates.
The same strain degree was observed on HEMT structures grown on SiCrystal (delivery 4) and Cree substrates.
Optimized AlGaN/GaN HEMT layers on SiCrystal substrates were electrically and structurally comparable to layers grown on Cree substrates.
Deviations for GH50 component performance comparing qualified Cree epi wafers were rather related to the epitaxy quality than to the substrate quality.
Observations:
There might be an influence of substrate quality on the electrical properties spread of HEMT structures.
All SiCrystal wafers had a higher Warp before epi-growth compared to Cree substrates. After epi-growth, SiCrystal and Cree wafers were comparable.
The line width of the symmetric 002 GaN reflection was increased for HEMTs on SiCrystal substrates compared to Cree substrates.
A significant larger change in the bow value before and after epi growth was observed on the last wafer delivery, compared to previous delivery in December 2012.

The XRD peak position of the AlN nucleation layer indicated that it is under tensile strain when grown on SiCrystal substrates compared to CREE substrates, which were fully relaxed. This might be correlated to the bow value, mentioned above.
Spread in the electrical properties of HEMT structures was higher on SiCrystal substrates than on Cree substrates.

2. Benchmark
The benchmark report is based on technical results achieved during the project months T0 to T0+18.

- SiC Substrate quality benchmark
X-ray omega scans were performed in order to investigate the bulk structural properties of the different substrates. As a figure of merit the line width of the SiC(0008) and SiC(00012) reflection was taken for 4H Cree and 6H SiCrystal substrates.
Overall the structural quality of SiCrystal and Cree substrates was good, however it was found that the line widths of Cree material tended to be lower and more homogeneous than for SiCrystal material.
Cross polarized imaging systems were used for the visualization of the micropipe and defect distribution as well as the crystal strain across the wafer. Often heavily distorted regions at the edges of the wafer and defect clustering could be observed. Areas with higher strain and defect clustering were visible for both types of substrates. In general the Cree substrates seemed to be slightly more homogeneous over the complete wafer with lower strain.
The surface morphology of the substrates was analysed using atomic force microscopy in order to evaluate the substrate on a nanometer scale. All SiCrystal substrates with chemo-mechanical polish (CMP) revealed a rough surface with scratches arising from the standard polishing procedure. However, the samples from one boule with SiCrystal CMP surface revealed a morphology very comparable in roughness to the Cree substrate surface that is achieved using CMP.
The Candela CS20 optical surface analyzer is a laser-based, nondestructive inspection system for semiconductor wafers. Four signal detection channels measure the topographic and reflectivity variances on the surface and detect defects in the optically transparent substrates and films while conventional dark field tools cannot use this technique. Additionally it can image and automatically count sub-micrometer scale crystallographic defects. It was found that the SiCrystal wafers had a slightly higher number of structural defects in comparison to a typical Cree substrate.
Electrical substrate characterization was done with a COREMA-WT system for contactless resistivity mapping on 32x32 points across the entire wafer area. The non-destructive contactless capacitive measurement technique requires no sample preparation and generates full wafer resistivity topograms revealing lateral resistivity variations as small as 1% with high lateral resolution in the range between 105 to 1012 Ω×cm. Low ohmic parts or inclusions can be identified which could drastically decrease the performance of high frequency properties of transistor devices.

Both Cree and SiCrystal s.i. SiC substrates showed a very high mean bulk resistivity larger than 1010 Ohm*cm and good homogeneity across the entire wafer. Both substrates showed perfect compensation of residual carriers in the material, so the Va-doping of the boule for SiCrystal substrates resulted in a similar resistivity as the intrinsic compensation, which is used by Cree for the growth of their SiC material.
The COREMA-VT system can evaluate the temperature dependence of the resistivity up to ~600 K. The Arrhenius plot obtained by variable temperature measurements yields the Fermi level and other details of the compensation process. The system is intended for the growth optimization and quality assessment of semi-insulating SiC and gives additional information about the compensation level in semi-insulating SiC substrates.
The measurement was done in the dark. On illumination by ambient light, the Cree substrate showed a persistent photoconductivity, while the SiCrystal substrate did not show such behaviour. The activation energy of the SiCrystal wafer (818 meV) can be directly correlated to the Va doping of the substrate, verifying the good compensation of the material. For Cree material the measured activation energy was 975 meV.

Micropipes were investigated in the wafers using optical microscopy. We observed low micropipe densities below 1 cm-2 for both types of substrates with one substrate each having a considerably higher density of micropipes.
Thickness, bow and warp were measured before epitaxial growth using a surftest profiler.The wafer is fixed at three edge positions and the positions of the wafer surface on both sides are measured as line scans along the central horizontal and vertical axis.
The thickness spread per wafer was very comparable well below 5 µm for both SiCrystal and Cree substrates. This result was also reflected in the very low TTV and LTV values for both suppliers. Bow and warp values are lower for SiCrystal compared to Cree substrates.
Selected wafers have been studied by x-ray topography using a Bede L4 Lang Camera. This includes a scanning measurement using a selected reflection plane, in this case the symmetric [008] and [0012] plane for 4H Cree and 6H SiCrystal substrates, respectively, giving an image of the actual crystal structure on a photographic plate. The topography measurement takes about 700 sec per mm, giving a total measurement time for a full wafer of close to 15 hours. The dimension of the topograph is geometrically distorted, in this case horizontally compressed, due to the geometry of the reflection plane towards the film. The relative intensities of the images are typically not comparable but a result of the scanning and crystal orientation settings.
Amplified images of selected parts of a SiCrystal substrate showed the presence of different structural defects. A comparison with a topographic image of a Cree substrate has been performed. The Cree substrate showed a larger crystal wafer bending, and the measurement had to be performed in 9 different segments using different omega and 2theta angles. This wafer had a more homogenous background contrast indicating a general lower dislocation density, but a stronger local contrast probably related to grain boundaries.
A higher density of micropipes was seen in the regions where structural contrast is seen in the topograph.

Conclusion

The overall results for the substrate quality were very promising as the structural and electrical data on Cree and SiCrystal s.i. SiC substrates were very similar.

Summary key results:
Substrate surface: CMP polish from Cree and NovaSiC seemed to be nearly identical and slightly better than the actual SiCrystal standard mechanical procedure. Subytrates with SiCrystal CMP were comparable to Cree.
Substrate bulk properties: Substrate resistivity of SiCrystal and Cree substrates was very good at a very similar level. Overall defect density was comparable for SiCrystal and Cree substrates. Micropipe density of SiCrystal substrates was at least as low as of Cree substrates. Good crystalline quality was detected both for Cree and SiCrystal wafers but with lower dislocation density for Cree. FWHM of the SiC peak of Cree substrate was smaller and more homogeneous across the substrate than for SiCrystal wafers. Higher strain on SiCrystal substrate was detected.
Geometry: SiCrystal substrates themselves were considered to be at least as good as Cree substrates

- GaN Epi quality benchmark

This chapter describes the work that has been undertaken to benchmark the GaN epi layer quality on s.i. SiC substrate from Cree and SiCrystal. AlGaN/GaN HEMT structures have been grown on these substrates by the three epi houses (III-V-Lab, Fraunhofer IAF and University of Linköping). The layers have been characterized and benchmarked regarding epi layer quality against commercially available substrate material.

For milestone M1 all of the three epi-houses received five 3 inch s.i. SiC substrates from SiCrystal, which originate from 2 different SiC growth boules. For milestone M2 ten 3 inch s.i. SiC substrates have been supplied by SiCrystal coming from 3 growth boules. These wafers have been characterized directly after delivery with respect to their structural, electrical und morphological properties and compared to commercially available Cree substrates.
Subsequently a HEMT structure consisting of an isolating GaN buffer, a 22 nm thick barrier layer with nominally 18% Aluminium and a 3 nm thick GaN cap has been grown by MOCVD both on SiCrystal s.i. SiC substrates and on Cree substrates. The epitaxial layers have been characterized with respect to their electrical, morphological and structural properties and benchmarked to epi layers grown on commercially available Cree substrates.
Finally a feedback on the substrate quality, the impact on the epitaxial growth and the comparison to Cree substrates have been transferred to SiCrystal for improving the next development cycle of s.i. SiC substrates.

All epi houses got the same amount of wafers from the different boules to enable a comparison of different crystal quality and surface polishing treatment and to benchmark its influence on epi layer quality. After an extensive wafer income inspection at each epi house, an AlGaN/GaN HEMT structure has been grown on these substrates. All three epi houses use different MOCVD systems for the epi growth (IAF: multi wafer planetary reactor, III-V-Lab: multi wafer close couple shower head reactor, Linköping: Epigress single wafer reactor). Finally these wafers have been characterized with respect to their electrical, morphological and structural properties and benchmarked to commercially available Cree substrates.

The epi layer structure was grown by MOCVD (metal organic chemical vapour deposition) on s.i. SiC substrates from Cree and SiCrystal and based on a jointly agreed structure between the epi-houses (III-V Lab, Fraunhofer IAF and Linköping University) and the device house (UMS) to ensure to get a suitable structure for testing the quality of the SiC substrates and perform device processing.

The roughness of the epitaxial layer structure was measured by atomic force microscopy (AFM) on different scan ranges. HEMT structures on SiCrystal and Cree substrates showed similar morphology with RMS roughness values in the range from 0.2 nm to 0.35 nm.
The Lehighton eddy current system monitors the homogeneity of sheet resistance of the two dimensional electron gas (2DEG) of the HEMT epi layer structure, which mainly depends on the Al content and the thickness of the AlGaN barrier layer, the GaN cap thickness and the quality of the epi layer stack. The sheet resistance is therefore proportional to the sheet carrier concentration and the mobility of the carriers in the 2DEG channel. Also the substrate quality and morphology itself influence these two values, because layer strain and epi quality are directly affected by the substrate quality and the defect density.
Wafers which are coming from different boules showed a significant difference in sheet resistance. Similar results have been investigated also by III-V-Lab und University Linköping.
The standard deviation for the sheet resistance for the measurement of 66 points across the 3 inch wafer was very good and amounted to about 2%.

A MDC Mercury prober system was used to evaluate the CV characteristics and the carrier depth profile for the HEMT structures on Cree and SiCrystal substrates. The buffer showed a fast drop in carrier concentration inside the GaN buffer layer, demonstrating good buffer isolation. The sheet carrier concentration in the 2-DEG channel was slightly below 6*1012 cm-2 (Cree) and below 3*1012 cm-2 (SiCrystal), which are typical values for HEMT structures with 18% Al (Cree) and 16% Al (SiCrystal) and 22 nm AlGaN barrier layer, respectively. The pinch-off voltage was in the range of -1.8 V (Cree) to -1.1 V (SiCrystal), the capacitance at pinch-off condition was small and amounted to C(-5 V, 10 kHz) = 4 pF.
Wafer bow and warp are important parameters for the successful epitaxial growth because of the thermal contact and the heat transfer of the satellite disc to the wafer, which directly influences growth rate and composition of the epitaxial layers.
The sign and the amplitude of the wafer bow after epi could be concave and convex, independent of the substrate supplier. No specific difference between Cree and SiCrystal could be observed
X-ray diffraction (XRD) analysis was used to measure the composition and layer thickness and monitor the quality of the HEMT layer structure on the s.i. SiC substrates.
The FWHM of the line width of the 002 and the 102 reflex is sensitive to the quantity of the screw and edge dislocations, respectively. Generally, the out-of-plane tilt and in-plane twist of the GaN films can be correlated to the densities of the screw threading dislocation (TD) with the Burgers vector b = [0001] and edge TD with b = 1/3 ⍰11-20⍰, respectively. In epitaxial GaN films, it is well known that the edge dislocation density is higher than the screw dislocation density. Therefore, the in-plane twist angle of the GaN films is larger than the out-of-plane tilt angle.
It was found that the line width of the symmetric 002 reflex for the GaN peak is significantly increased for HEMTs on Cree substrates. At the same time the asymmetric 102 reflex was significantly smaller for these wafers indicating a higher density of screw and a lower density of edge dislocations in the GaN buffer

layer. The reason for this effect is not clear. A possible explanation could be differences in substrate and epi layer strain which have been seen by cross polarization imaging and XRD measurements.

Conclusion

The overall results for the substrate quality and the epitaxial growth were very good as the structural and electrical data on Cree and SiCrystal s.i. SiC substrates were very similar.

A summary of the key results:
Substrate surface: The large area surface morphology was similar to that of HEMT structures grown on Cree substrates. RMS = 0.2 - 0.5 nm, no difference between HEMTs on Cree and SiCrystal substrates.

Electrical data: No specific difference between HEMT structures on Cree and SiCrystal could be observed. Differences were mainly due to the different Al content of the layers. Contactless measurements of the mobility and sheet carrier concentration revealed similar values for HEMTs on Cree and SiCrystal substrates. Al content in the AlGaN layer was different for different boules, therefore the Rsheet differs.

Structural properties: The sign and the amplitude of the wafer bow after epi could be concave and convex, independent of the substrate supplier. No specific difference between Cree and SiCrystal could be observed. The line width of the symmetric 002 GaN reflex was significantly increased for HEMTs on Cree substrate. At the same time the asymmetric 102 reflex was significantly smaller for these wafers in comparison to SiCrystal substrate.

- Device quality benchmark

GaN HEMT devices have been manufactured using the qualified UMS GH50-10 technology. The GaN epi wafers have been grown by MOCVD on s.i. SiC substrate manufactured by SiCrystal by epi partners Fraunhofer IAF, ATL 3-5Lab und University Linköping. For comparison and device benchmarking epi growth on Cree substrates was performed.

For the wafer fabrication the qualified UMS GH50-10 process has been used.
The on wafer uniformity and the run to run repeatability was very good controlled by the UMS qualified commercial epi wafer source, but most of the consortium epi wafers were in specification. Taking into account that the EUSiC epi suppliers were not in a production mode the results were very good.
For a better interpretation of the I3 PCM data knowledge about the target values and the specification limits was necessary.
Looking at the trend charts for drain source currents at different conditions, the maximum transconductance and the gate source voltage for Ids/100 one could identify a certain spread from wafer to wafer and from batch to batch. The wafer to wafer variation was obviously caused by the fact that different substrate and/or epitaxy runs from the same supplier were compared within one lot. The batch to batch variation originated most likely from the process capability, which is still something that can be improved in the future by more wafer throughput.
What was not really detectable was the influence of the different substrate suppliers on these parameters.

This observation was for the EUSiC project a very good outcome of this investigation.
One requirement for a good and long term stable transistor operation is the level of leakage current and the drift behaviour over various bias voltages. The upper specification limit for the leakage current at a bias voltage of 10 V is set to 200 µA/mm. This value of max. 200 µA/mm should in addition not increase for bias voltages up to 150 V.
It was found that these requirements are more or less fulfilled for the IAF epitaxies but not for the epitaxies grown by University Linköping and 3-5Lab. These effects were not related to the utilisation of the substrate material.
Low leakage at Vds=150V was only achieved by epi wafers manufactured by IAF.
In contrast to epi wafers from Linköping and 3-5Lab the GaN buffer away from GaN channel was Fe doped in case of epi wafers manufactured by IAF. No impact on pinch-off behaviour or leakage current could be observed whether SiC substrate from Cree or Sicrystal is used.

Device isolation by Boron implantation was in the expected resistivity range except for 2 wafers with epi from III-V Lab on Sicrystal SiC.

After device manufacturing and characterisation, good results have been achieved.
Transistor results obtained on SiCrystal substrates were equivalent to those results obtained on commercial reference substrates from Cree.
Deviations from the UMS qualified source were related to the epitaxy quality rather than to the substrate quality.

Quality and specification update for process chain

This chapter summarizes the quality feedback information which has been gathered in Tasks 3.2 3.6 and WP4 and WP5. In this report, specifications for 3 inch semi-insulating Silicon Carbide (SiC) substrates for the EuSiC project were established in accordance with all project partners.
The data of s.i. SiC substrates and at later process steps were reviewed and a list of specifications was established. Main focus was on the direct feedback information from all project partners, to update and verify the product and process specifications for the EuSiC project. The specifications are divided into a wafer specification and an epi-layer specification. They represent the final result and achievement of this project.

5.1 Specifications for 3-inch semi-insulating SiC substrates

Polytype and conductivity type
The polytype can be specified for 6H with 100% polytype homogeneity with semi-insulating conductivity type.

Resistivity
The resistivity for the s.i. SiC substrates can be specified for > 107 Ohm*cm at room temperature with no upper limit. The analysis of resistivity data of SiC substrates within this project showed that all wafer

exhibited a resistivity of typical around 1011 Ohm*cm with the lowest value of 7.25*109 Ohm*cm for wafer DA-H2F01-19 from SiCrystal. Nevertheless, the feedback from all project partners indicated that a minimum resistivity of 105 Ohm*cm is regarded to be sufficient at operating temperature up to 200°C. Resistivity uniformity was determined to be not critical until the minimum level is within specification limits. Thus resistivity uniformity was not specified.

Crystal orientation and orientation homogeneity
Crystal orientation could be set for (0001) and for the orientation homogeneity several data were collected for the data table. A specification limit of 0.5 deg of milestone M9 was confirmed by the data. A tighter specification has been considered but it was rejected due to economic aspects.
The orientation homogeneity is best expressed by the statistical robust average difference in degree and this value could be specified for < 0.2deg confirming the value identified in milestone M9. The data of the wafers, delivered by SiCrystal for the EuSiC project matched all the specifications.

Wafer dimensions (thickness, diameter, bow, warp, TTV, LTV)
According to the final inspection data from SiCrystal, the specification could be kept at 360µm +/- 10µm, mainly due to internal specifications for standard 3-inch products at SiCrystal. A tighter specification with a tolerance of +/- 5µm as discussed previously was not supported by the data of this study. A shift from the initially target value of 350µm was recommended and the thickness specification was adopted to 360 +/- 10µm. Wafer diameter was specified for 76.2 +/- 0.5 mm, which is in accordance with measurement data.

Wafer bow was specified for 0 +/- 5µm according to the consortium. The data showed also an acceptable quality of one wafer at a bow of 7µm (wafer BH-E611B-18). However due to expected negative impact on yield and technological parameters the specification was not extended. Wafer warp was discussed in the technical work meeting in Paris in 2012. From SiCrystal's side is seemed reasonable to specify wafer warp for < 10µm. These limits still match to the completed data and are kept.

According to the consortium, TTV (total thickness variations) could be specified for < 5 µm and LTV (local thickness variations) for < 1.5 µm. This was confirmed by the evaluation.

Wafer roughness
The surface roughness of the Si-side of the wafer is a critical parameter for the deposition of the epi-layer according to the epi-partner.The surface roughness specified in milestone M9 for < 0.2 nm (AFM, spot size 2x2 µm to 5x5 µm) and < 0.35 (ATOS), respectively was confirmed. This surface quality is only achievable with CMP treatment of s.i. SiC wafer surfaces.

Micropipe density
For the project, SiCrystal and LiU investigated the micropipe densities of the SiC substrates. According to the measurement data, the average density was specified for < 1 cm-2.

Rocking curve analysis (FWHM (ω-scan on 5-points))
Rocking curves were measured on the substrate before epi and are a critical parameter for further processes. In agreement with all partners, the specification was set for < 40 arcsec for the average value of 5 measurement points of X-ray mapping with a beam-size of 0.5mm x 8mm. Although good results were achieved also for high FWHM values above 100 arcsec the consortium recommended to limit the specification. As a second specification criterion the uniformity was regarded as a useful parameter. Therefore the standard deviation was specified to be < 20 arcsec.

Surface particle contamination
Surface particle specification limits are split by PSL size two categories, 2-8 µm PSL and >8µm PSL. Best Wafers exhibit particle counts of more than 1000 for around 1000 particles of 2 – 8µm diameter (PSL reference) and around 100 particles of diameter > 8µm (PSL reference), measured at substrate supplier SiCrystal. Specification was set accordingly. Data varies due to differences in particle measurement system and recipe.

5.2 Specifications for 3 -inch semi-insulating epitaxial deposited SiC wafers

Epi-Wafer dimensions (bow, warp, TTV, LTV)
Epi-Wafer bow was specified for < 20 µm and warp for < 30 µm, according to UMS. The TTV (total thickness variations) could be narrowed from formerly < 10µm to < 7 µm and LTV (local thickness variations) for < 5 µm which was mainly in agreement to the data created within the EuSiC project for SiCrystal wafers. For LTV of epi-wafers the specification limit was further reduced to < 3µm to avoid technological limitations at device fabrication.
It should be noted that Bow EPI achieved best results for a Bow >25µm. As also technological issues have to be considered, the resulting spec limit of < 20 for bow µm was confirmed. UMS spec limits for warp and TTV were approved.

Roughness of Epi-wafer
The wafer roughness of the epitaxial layer on the substrate could be specified for < 0.5nm on an inspected area of 10x10µm, or < 0.25nm on an inspected area of 5x5µm.

Scratches
UMS required wafer quality with the specification of no scratches longer than 1.0 cm.
Shipped wafers to project partners all conformed to “no scratches” due to Candela inspection. Non-conforming epi-wafers were not reported by UMS incoming inspection. The specification value was confirmed.

Electrical specifications – Sheet resistance by Eddy current measurements
Sheet resistance of epitaxial coated s.i. SiC substrates is a key parameter for HEMT device fabrication; therefore UMS requested a specification of 640 +/- 40 Ohm/sq.
Using incoming inspection data from UMS, the distribution plot of the sheet resistance showed that the specification of 640 +/- 40 Ohm/sq is not satisfied by best wafers. Best wafer results were also present at the borders of the specification. The observed spread was caused by the epi-process itself, the different

epi-houses and the measurement technique simultaneously. There were limitations of measurement accuracy due to different equipment types. The conclusion was to extend specification to 640 Ohm/sq +/- 60 Ohm/sq.
For the productive exploitation an individual match of sheet resistance specification with each supplier is necessary to account for the different epi-process characteristics. As a general strategy a continuous reduction process of spread over time is necessary for each epi-house, which is beyond the scope of this project.

The range of resistivity on a wafer is also a relevant quality indicator for the wafer resistivity uniformity. The range can be captured by monitoring the standard deviation (Stabw) of all data for each wafer or the max_Delta which indicates the difference between maximum and minimum value (range) for each wafer. Standard deviation sheet resistance values (Stabw) for best wafers made the former specification < 10 Ohm/sq of milestone M9 questionable. The consortium confirmed a specification limit of < 30 Ohm/sq for the standard deviation.
The property max_Delta now reflected a large range up to 175 Ohm/sq (recent spec suggestion < 60 Ohm/sq). It was removed from the specification as it is redundant to standard deviation.

Layer specifications
The HEMT structure was based on UMS design and consisted of 4 layers.
The different layer thicknesses were specified by UMS as follows:
- GaAlN layer thickness: 22nm +/- 1.5nm
Comment: Specification is met by best wafers, with a small trend to lower values. One Benchmark with IAF epi is at 20nm.
- GaN cap layer thickness: 3nm +/- 1nm
Comment: Best Wafers are found also outside this specification (1.5 – 4.5nm)
- Al content in GaAlN layer: 18% +/- 1%
Comment: Best wafers are at 19% +/-1%, so an offset is present and was considered in the specification.
- GaN buffer layer thickness: 1.8µm +/- 200nm
Comment: Best wafers cover 1.85µm +/- 150nm

The AlN nucleation layer was not specified. The total of GaN cap layer and GaAlN layer thickness can be measured with higher precision. The use of this combined thickness was recommended where appropriate.

Conclusion: These device specifications showed slight deviations to the data of best wafers. The specification of Al- content in GaAlN layer was therefore adjusted to reflect the optimum of the process chain conditions of this study.

5.3 Conclusion

The verification of the specification for the complete process line has been successfully executed. Based in

the first specification review of milestone M9 in project month 18 the key parameters have been identified. Redundancies and irrelevant properties have been removed from the specification within the framework of this project. Device performance as reported by project partner UMS using its device technology, also including device benchmark data, has been used as an indicator for the judgement of specifications. The statistics of “golden” devices and wafers could be improved with a higher number of wafers in the future to compensate for the multitude of process parameters and inevitable process fluctuations for the price of a much higher effort and capacity demand. As main improvements updates for the specifications for wafer and epi-wafer geometry, epi-layer sheet resistance and epi-layer Al-content are to be mentioned.
As a final result the project accomplished to demonstrate state of the art device performance as well as verification and in some parts further optimization of process parameter specifications for the main supply chain interfaces at substrate and epi-wafer level.
As the main topics for a future (industrial) use of these specifications several economic optimisations in the implementation in terms of yield and process stability are expected.
Potential Impact:
Potential impact
Gallium Nitride (GaN) is a key strategic enabling technology that has the demonstrated potential to provide an order of magnitude improvement in RF output power as well as higher robustness against high temperature and voltage. These characteristics promise to disrupt today’s state of the art components used for space applications like Telecommunications, Navigation and Earth observation. GaN allows designing simplified, high efficiency, robust and highly flexible solid state power amplifiers (SSPAs). The advantages allow new space system architectures like active antenna systems in the Ku and Ka frequency bands.
By developing of high quality semiinsulating SiC substrates EuSiC strongly reduced the dependence of European space industry on non-European suppliers. Additionally, the EuSiC project generated impacts are fully in-line with those listed in the Work programme, especially SPA.2009.2.2.01 Space technologies. Most importantly for the industry is, that the key patent for the growth of semi-insulating SiC runs out by 2014 [1]. This patent has kept the most economical way of producing semi-insulating SiC under the control of the patent holder. After 2014 the situation will change and therefore it was highly recommended to develop and establish an alternative supply chain without any restrictions like ITAR or end-user certifications, especially but not only for small and mid-size enterprises. The SME get provided to enter the space market easier than before and are able to compete on the European market as well as worldwide without paying attention to legal issues like ITAR. Additionally, the big companies are enabled to offer ITAR-free components and modules for space applications worldwide.
The main medium term goal of EuSiC was to prepare European Industry and Academia for the time after this significant instant.

Literature:
[1] Barrett, Donovan L., et al. High resistivity silicon carbide substrates for high power microwave devices. 5,611,955 United States of America, 18 Oct. 1993.

Dissemination
The EuSiC project aimed at developing and establishing a new European SiC substrates sources for GaN wafers to be used for space applications, with opportunities to expand to other kinds of applications. This was an opportunity for reaching out to the scientific community, industry and the general public in order to

make them aware of these available SiC substrates, their impact on European society and Europe's position in the development of these substrates and markets. Standard dissemination channels such as: publications in major conferences and journals, organization of specific EuSiC day(s), possibly as space technology events to major European and/or international scientific and technical events, technical talks from EuSiC included in International events. The dissemination took placed in a strong international scientific context.
Within the consortium one of the major tools for internal communication were the technical meetings. Seven meetings were held within the overall project period to discuss project progress, calibrate the activities and decide about necessary steps to be taken. The main results can be summarized as followed:
During the first three meetings in Erlangen (Ge), Freiburg (Ge) and Nürnberg (Ge), the project results were presented, the project progress was in accordance with plan.
The forth meeting was held on 3-4th April 2012 in Paris (F). All consortium-members joined and the project activities were presented. In WP1, WP4 and WP5 a delay was observed. The main cause was identified and countermeasures were taken. The meeting was additionally focused on the discussion of benchmark results and specification review.
At the fifth meeting in Ulm (Ge) the project progress was in accordance with plan. For improved benchmarking it was decided to include benchmark epi-wafer in the second device campaign at project partner UMS.
At the sixth technical meeting in Linköping (Sw) the final surface preparation type for delivery M4 was decided. To support technical progress at the epi-houses SiCrystal agreed to accelerate progress on M4 (4th substrate delivery).
The last technical meeting was held at the 27th of November 2013 in Nürnberg (Ge). All tasks during the project were executed as planned. All deliverables were generated in time. As a final result the project accomplished to demonstrate state of the art device performance as well as verification and in some parts further optimization of process parameter specifications for the main supply chain interfaces at substrate and epi-wafer level. Main topics for a future (industrial) use of these specifications should include several economic optimizations in the implementation in terms of yield and process stability.
Besides those meetings, the consortium members joined in various phone conferences or bilateral calls and mail conversations to e.g. discuss technical progress and prepare deliverables. A download-area, exclusively arranged and accessible for all consortium partners was used to share and store common documents such as the grant agreement or the deliverable reports.
Due to the nature of EuSiC was a relatively small research project, the dissemination of foreground was mainly carried out through classical scientific articles or conferences. During the whole project 8 oral presentations and 4 posters were presented at national and international conferences. In addition 4 papers were published in journals and conference proceedings.
The consortium partners spread information about the EuSiC project within their own organizations and used various channels of information exchange including the project progress meetings. These were adequate measures to ensure that information was consistently communicated to external addressees

Use Plan
In summary it can be stated that the companies SiCrystal and UMS have concrete plans to use the results of the EuSiC-project commercially. SiCrystal plans to sell first semi-insulating substrates within Europe in June 2014. UMS is planning also to use those results for the production of various products, which mainly will be launched in between 2014 and 2015. Fraunhofer and Linköping University might act as a source for

epi-service, whereas III-V Labs is focused on R&D only.

SiCrystal AG

SiCrystal's target within the EuSiC project was the development of crystal growth and substrate preparation processes to enable the supply of quality-wise improved semi-insulating 3" Silicon Carbide substrates. SiCrystal plans to commercially use those optimized processes, to manufacture and supply semi-insulating 100mm substrates for the worldwide market.

SiCrystal understood that the patent situation at the beginning of this project didn`t not allow the company to sell semi-insulating substrates. Because of an impending patent infringement SiCrystal decided to stop it`s semiinsulating activities, commercial and non-commercial ones, in 2006 to restart R&D within EuSiC.

To SiCrystal's knowledge one specific US patent, exclusively licensed by one of SiCrystal's competitors and blocking SiCrystal's commercial activities, expired on 18th of March 2014. It is SiCrystal's understanding that this fact should enable the company to re-launch worldwide semi-insulating Silicon Carbide substrates after that time. To make sure that no further patents would block SiCrystal`s activities an evaluation of the patent situation on semi-insulating SiC was performed.

During the last year SiCrystal started an evaluation of current patent situation on semi-insulating SiC material. The evaluation was done in cooperation with a patent attorney. First patent search showed about 80.000 hits. In the next step the results of the patent search were reduced to 79 by a detailed keyword search performed by a patent attorney. The 79 patents identified by keywords were checked by a technical expert at SiCrystal. At this stage the individual claims were checked and compared to the technical process and product specifications. This analysis showed that 71 patents are not related to SiCrystal`s process or product specifications. However, 8 patents were identified which could not clearly rated by the technical expert and had to be checked in detail.

These 8 patents were analyzed by a patent engineer with technical background at SiCrystal. In the first step a detailed patent family analysis of these 8 patents was performed. At this stage all related patents of each patent family were checked. In the next step the results of this analysis were discussed with a patent attorney. The discussion of non US patents is finished now. From technical and patent law side none of the evaluated patents is in conflict with our process or product specifications. The discussion of several US patents, which are still in proceedings and are not granted up to now, are still ongoing. The analysis and rating of these patents will be finished during the next month.

Currently, SiCrystal plans to sell first semi-insulating substrates 100 mm to several European customers in June 2014. These products will be based on the improved processes developed within the EuSiC-project. However, the shipment of these qualification samples is linked to some restrictions to ensure that this material will not be imported to the United States before the evaluation of the US patents is finally finished.

Moreover, SiCrystal filed two patents in 2008 about semi-insulating SiC substrates. Both patents were granted in May 2013. The opposition term has expired in August 2013, no objections were received.

UMS

UMS is a III-V compound semiconductor manufacturer for both GaAs and GaN-devices and MMICs. The access to SiC substrates with GaN epitaxy is essential to provide the space and other market with GaN HEMT devices which offer significantly higher output power density at frequencies up to Ku band compared to conventional GaAs technologies. Such high power operation can only be reached with low thermal coefficient mismatch and high thermal conductivity as shown by SiC substrates.

Today's forecast for GaN devices for space application see a dramatic growth in use of solid state power amplifiers (SSPAs), for example the Globalstar2 has a need of more than 900 SSPAs. The upcoming use

of active antenna arrays for digital beam forming leads to a demand of hundreds of SSPAs with tough size requirements due to limited space available close to the antenna. Thus, high quality GaN-on-SiC epi-material is required to obtain such compact antenna designs. Today, the main source for such epi-material is in the US and in Japan. Both geographical origins having restrictions (ethic code of Japanese government/companies) and at least a risk of restrictions (US ITAR).
The availability of SiC substrates without restrictions enables very wide business opportunities for the whole European space community and enhances the competitiveness of GaN suppliers like UMS worldwide.
In the past, only Cree and II-VI Inc. offered semi insulating SiC substrates as being required for microwave devices and circuits. The use of such SiC substrates from USA has several constraints regarding the use in certain applications like space and defense. Therefore, UMS has a significant benefit from the EuSiC project with respect to the availability of GaN devices and MMICs in terms of business opportunities. Apart from the strategic markets (defense and space) UMS is partnering with NXP to address the market for RF power transistors, which will break through the 1 billion USD limit in 2014, according to independent market research. Products built from GaN will play an increasing role in this sector, and are tipped to take as much as 30 percent of this market by 2015. If true, this would lead to a GaN RF power transistors market of at least 300 million USD.
For such high business demand GaN technology needs to be supported by mainstream material and tool vendors in the complete supply chain. An additional European source for semi insulating SiC and GaN-on-SiC epi-wafers will contribute to establish a competitive market, resulting in the necessary reduction of wafer cost/price as being required for the take-off of larger volume markets.

Fraunhofer Gesellschaft
Fraunhofer IAF has more than a decade of experience in epitaxial growth and processing of AlGaN/GaN HEMT structures on commercially available SiC substrates from Cree. IAF continuously sells epitaxial wafers on commercially available SiC substrate within the general terms of the Fraunhofer Society. In the case of SiCrystal SiC substrates IAF is planning to also serve as source for epitaxial material once the substrates from SiCrystal are commercially available.
Linköping University
LiU has no plans to use commercially the HEMT process. Only R&D usage is planned. However, collaboration with partners, like SiC wafer manufacturers may result in epi service.
III-V-Lab
III-Vlab intends to use Eusic results for internal needs and Thales applications. III-Vlab has no plans to use commercially Eusic results. Only R&D usage is planned. However, III-Vlab agrees to transfer his experience in epitaxial growth of GaAlN/GaN HEMT structures to a European Epi Supplier.
List of Websites:
SiCrystal AG, Germany (SiC substrate)
- Ms Storm, Sabine (sabine.storm@sicrystal.de)
- Mr Vogel, Michael (michael.vogel@sicrystal.de)

Fraunhofer IAF, Germany (GaN-Epitaxy)
- Mr Waltereit, Patrick (patrick.waltereit@iaf.fraunhofer.de)

III-V Lab, France (GaN-Epitaxy)

- Ms Poisson, Marie-Antoinette (marie-antoinette.poisson@3-5lab.fr)

Linkoping University, Sweden (GaN-Epitaxy)
- Mr Janzen, Erik (erija@ifm.li.se)

UNITED MONOLITHICS SEMICONDUCTORS GMBH, Germany (Devices)
- Mr Splettstößer, Jörg (jörg.splettstoesser@ums-ulm.de)

Verwandte Dokumente

final1-eusic-publishable-summary.pdf

Letzte Aktualisierung: 12 September 2014

Permalink: https://cordis.europa.eu/project/id/242360/reporting/de