

# erc III-Nitrides Nanostructures for Energyuropean Research Council Efficiency Devices

## Sprawozdania

Informacje na temat projektu

In-Need

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Strona internetowa projektu 🗹

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## Periodic Reporting for period 4 - In-Need (III-Nitrides **Nanostructures for Energy-Efficiency Devices**)

Okres sprawozdawczy: 2020-08-01 do 2021-01-31

## Podsumowanie kontekstu i ogólnych celów projektu

The main goal of this project is to demonstrate a completely new platform based on nanostructures that will enable to optimally exploit the outstanding properties of GaN semiconductors for state-of-theart electronic devices. The properties of this class of semiconductors yield a larger Baliga's figure of merit than in other materials, such as SiC and Si, enabling high-efficiency and miniaturized power

devices operating at higher temperatures (reducing cooling requirements), and high frequencies (reducing inductive elements in power circuits). However, the current performance of III-Nitride devices is far from the fundamental materials' limit.

To address the current challenges, this proposal is divided into three overall objectives:

- SP-A. Surface nanostructures for unprecedented lateral device performance
- SP-B. Embedded nanostructures for new vertical devices
- SP-C. Embedded nanostructures for advanced thermal management

This project has significant importance to our society in the field of efficient usage of energy. Energy efficiency offers a vast and low-cost energy resource to address the increasing energy demand, reduce carbon dioxide emissions, and enable the concurrent development of renewable energy technologies. Power electronic devices are at the heart of an efficient energy management required in any sustainable energy technology. They will play a pivotal role in energy efficiency with a potential to reduce by more than 20% the overall electricity consumption.

## Prace wykonane od początku projektu do końca okresu sprawozdawczego oraz najważniejsze dotychczasowe rezultaty

#### • SP-A. Surface nanostructures for unprecedented lateral device performance

This work package has demonstrated several new technologies based on nanostructures applied to lateral power devices. In particular, a novel device concept to address the intrinsic trade-off between electron density and mobility, based on a multi-channel tri-gate structure. High conductivity was obtained by vertically stacking several high-mobility channels to enhance the carrier density. A simultaneous electrostatic control over all channels is achieved by a 3-dimensional gate electrode (trigate) around all channels. The multi-channel structure was judiciously designed to yield a small sheetresistance of 80  $\Omega$ /sq., using only four 2DEG channels, that resulted in an equivalent resistivity of only 1.1 m $\Omega$ ·mm. Our work shows that whereas conventional field plates (FPs) are not suited to increase breakdown voltage in high-conductivity multi-channels, slanted tri-gates offer better electric-field management inside the device. Power devices made with 15-nm-wide nanowires were shown to exhibit ultra-low specific on-resistances of 0.46 mΩ·cm-2, enhancement-mode operation, breakdown voltages as high as 1300 V, and a record figure-of-merit of 4.6 GW/cm2 for d-mode devices and 3.8 GW/cm2 for e-mode devices. These results significantly outperform conventional devices and demonstrate the enormous potential of multi-channel devices for future power solutions. These works were presented in the 2019 IEEE International Electron Devices Meeting, accepted in Nature Electronics 2021 and received the best paper award at the IEEE ISPSD (Charitat Award).

#### • SP-B. Embedded nanostructures for new vertical devices

This work package has significantly contributed to the development of vertical GaN power devices on cost-effective large-scale Silicon substrates. After optimizing the growth, doping and device fabrication, our group showed remarkable electron mobility of 720 cm2/Vs for a 4-µm-thick GaN drift layer. This work has resulted in the demonstration of vertical GaN P-i-N diodes on 6" Silicon substrate with a high breakdown voltage of 820 V, corresponding to an excellent average electric field of over 2

MV/cm, even without edge termination, and state-of-the-art figure of merit of 2.0 GW/cm2. Based on this optimization, we have demonstrated the first GaN-on-Si MOSFET, using a 6.7-µm-thick n-p-n heterostructure grown on 6-inch silicon substrate. The devices consisted of trench-gate MOSFET in a quasi-vertical configuration, exhibiting enhancement-mode operation with a threshold voltage of 6.3 V and a high OFF-state breakdown voltage of 645 V with a 4-µm-thick drift layer. Our group also demonstrated for the first time a fully-vertical GaN power MOSFET on silicon. We developed a robust fabrication method based on selective and local removal of the Si substrate as well as the resistive and defective GaN buffer layers. High-performance fully-vertical GaN-on-Si MOSFETs were presented for the first time, with low RON and high VBR. Our results reveal a major step toward the realization of high-performance GaN vertical power devices on cost-effective Si substrates.

#### • SP-C. Embedded nanostructures for advanced thermal management

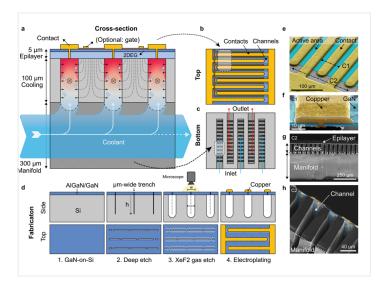
This work package demonstrated several technologies for cooling of electronics. In particular, we showed that co-designing microfluidics and electronics into the same semiconductor substrate, to produce a monolithically-integrated manifold microchannel (mMMC) cooling structure, provides efficiency beyond the state-of-the-art. Our results show that heat fluxes exceeding 1.7 kW/cm2 can be cooled down using only 0.57 W/cm2 of pumping power. We observed an unprecedented coefficient of performance (>104) for single-phase water-cooling of heat fluxes exceeding 1 kW/cm2, corresponding to a 50-fold increase compared to straight microchannels, as well as a remarkably high average Nusselt number of 16. The proposed cooling technology enables further miniaturization of electronics, potentially extending Moore's law and greatly reducing energy consumption worldwide. These results were published in Nature (Sept. 2020), together with one patent application and received the best paper awards in IEEE ITherm 2020 and Therminic. In addition, this work was covered by many mainstream news outlets, such as Scientific American, Le Figaro, Le Temps, NRC, IEEE Spectrum, New Scientist, Nature podcast, Olhar Digital, RTS (swiss radio).

### Innowacyjność oraz oczekiwany potencjalny wpływ (w tym dotychczasowe znaczenie społeczno-gospodarcze i szersze implikacje społeczne projektu)

This project led to several state-of-the-art results in different fields. For example, the concept of nanowire multichannel applied to power devices, made with 15-nm-wide nanowires, resulted in ultralow specific on-resistances of 0.46 m $\Omega$ ·cm-2, enhancement-mode operation, breakdown voltages as high as 1300 V and a record figure-of-merit of 4.6 GW/cm2 for d-mode devices and 3.8 GW/cm2 for e-mode devices. These results significantly outperform conventional devices, being the first time that a GaN lateral device breaks the SiC vertical limit. This is a significant breakthrough that demonstrates the enormous potential of multi-channel devices for future power solutions.

The concept that we proposed and demonstrated of monolithically-integrated manifold microchannel cooling structure, provided efficiency beyond the state-of-the-art. Heat fluxes exceeding 1.7 kW/cm2 could be cooled down using only 0.57 W/cm2 of pumping power. We observed an unprecedented coefficient of performance (>104) for single-phase water-cooling of heat fluxes exceeding 1 kW/cm2, corresponding to a 50-fold increase compared to straight microchannels, as well as a remarkably high

average Nusselt number of 16. These results show that these technologies can offer a pathway towards more efficient and thermally-managed electronics in the future.



Co-designed microfluidically-cooled electric device

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