The CONNECT project investigates ultra-fine CNT lines and metal-CNT composite material for addressing the issues of current state-of-the-art copper interconnects. Novel CNT interconnect architectures for the exploration of circuit- and architecture-level performance and energy efficiency will be developed. CMOS compatibility as well as challenges of transferring new processes into industrial mass production will be addressed.

The Overall Objectives are:
The Overall Objectives are:

1. Demonstrate cutting-edge electrical resistivity on CNT lines with diameter below 10nm made of individual doped MWCNT.

2. Develop process growth and impregnation methods for aligned CNT-Cu composite materials that achieve trendsetting current carrying capability for solving electro-migration issues with Cu interconnects.

3. Demonstrate the electrical, thermal and electro-migration properties of the CNT and aligned CNT-Cu composite interconnects on dedicated test structures. Integrate the aligned CNT-Cu composite with compatible CMOS back-end-of-line process and demonstrate on a two levels interconnect (via + lines) functional device with improved electro-migration.

4. Push advanced characterization methods to be able to relate dopant and morphology of single CNTs to their electronic and thermal transport behaviour.

5. Develop physical-driven models for CNTs and Cu-CNT composite materials to study their electrical, thermal properties for doped individual and bundle lines. The goal is to explore design methods for energy efficiency at circuit and architectural-level with novel CNT interconnects architectures featuring energies of few pJ per bit.

6. Exploit the participation of academic partners from differing scientific backgrounds to employ, educate and train young and aspiring people to advanced technologies ranging from sophisticated numerical tools to scaled CMOS with CNT-based interconnect integration.

Work performed from the beginning of the project to the end of the period covered by the report and main results achieved so far

WP-1: CNT ADVANCED LOCAL INTERCONNECTs
- localized growth and contacting of individual multi wall CNT.
- internal filling of CNT with dopants.
- demonstrated 75% reduction in CNT resistivity via PtCl4-based charge transfer doping.
- demonstrated interconnect resistivity in the 200-500 µohm.cm range for non-doped CNT with 5-10 nm in diameter, and ampacity > 10^8 A/cm2.

WP-2: CNT-METAL COMPOSITEs for GLOBAL INTERCONNECTs
- Electrical characterization and Electro-migration test structures designed to benchmark Cu versus Cu-CNT material.
- CNT grown on CMOS-compatible Co as catalyst in structures without any parasitic growth
- Evaluation of different copper plating bathes and methods (ECD and ELD) for copper impregnation of CNTs for vias or lines and realization for one- and two-level demonstrators.
- Manufacturability of Cu-CNT test structures under CMOS compatibility aspects.

WP-3: STRUCTURAL and ELECTRO-THERMAL CHARACTERIZATION
- Transmission electron microscopy measuring in-situ the doping distribution of single and bundled
Transmission electron microscopy measuring in situ the doping distribution of single and bundled MWCNTs - Correlation of doping morphology and conductance for different doping schemes - Local and operando probing of self-heating in CNT lines using Scanning thermal microscopy - Extraction of the reduced thermal conductivity of CNTs in contact with a dielectric for the first time

WP-4: MODELING and SIMULATION
- Developed hierarchical physical models for SWCNT, MWCNT, doped CNT and Cu-CNT composite interconnects by combining first-principle models (DFT) with NEGF and Monte Carlo simulations.
- Developed 3D Field solver simulator for fast and accurate extraction of RC parasitic elements in advanced CNT interconnect technologies.
- Physical understanding and electrical modeling of doped CNTs (both SWCNT and MWCNTs) and Cu-CNT composite for circuit-level simulation and performance evaluation.
- Physical design exploration of CNT interconnects for on-chip global power delivery, memory and digital logic design.

These results have been published on several high-impact journals and conferences such as IEEE TNANO, IEEE TED, and IEEE IEDM. The developed models are made available on the nanotechnology repository NANOHub.org [1-2].

WP-5: DISSEMINATION ACTIVITIES
- 3 Workshops
- 3 Webinars
- 22 papers across journals and conference proceedings (open access granted)
- Website and Wikipedia page active online

Progress beyond the state of the art and expected potential impact (including the socio-economic impact and the wider societal implications of the project so far)

WP-1:
- first demonstration that reducing the diameter of CNT bundles and moving towards individual MWCNT interconnects is an efficient path to reduce the resistivity of CNT interconnects.
- robust and scalable spray doping method allowing a 75% reduction in CNT resistivity.
- parallel integration of < 10 nm horizontal CNT interconnects with ampacity > 10^8 A/cm^2.
- variability of intrinsic CNT resistance and contact resistance

WP-2:
- composites of aligned CNT-Cu interconnects, compatible with CMOS BEOL and 300 mm Substrates and realization of vias and lines
- Design and production of multilevel test structure, and EM electrical test measurements, processing of Cu-CNT composites and benchmark against Cu reference
- CMOS compatible CNT growth, low temperature, wafer level with CMOS compatible catalyst
- Direct CNT growth in trenches and VIAs with preferential growth and integration approaches for
Direct CNT growth in trenches and VIAS with preferential growth and integration approaches for multi level demonstrator

WP-3:
- clear demonstration of doping an doping degradation inside individual CNTs
- Showed tomography of CNT composite using combined SEM/FIB and TEM study
- extraction from thermal conductivity of CNT and substrate coupling from nanoscale measurements (at 10nm resolution) using a novel approach, which avoids known systematic errors and limitations.
- Extension of the thermometry methods to non-linear devices

WP-4:
- First multi-scale modeling and simulation approach from atomist simulation to circuit-level simulation
- first charge-based doping modeling and simulation approach for SWCNTs and DWCNTs for circuit-level power and delay analysis
- first electro-thermal modeling and simulation approach for exploring CNTs and Cu-CNTs as beol interconnect material
- performed variability studies on SWCNT/MWCNTs to consider variation on chirality, defects density, diameter, number of shells and connectivity to contacts.

New Interconnect Architecture using doped CNTs and Copper-CNT-Composites as Interconnects.