The project addresses the ever increasing need for more functionality, increased speed and low power semiconductor devices at a lower cost. This is important for society as improved functionality of Semiconductors enable creating solutions to the societal issues of global warming & sustainable energy, an aging population, sustainable food & water supply, a growing global population, Safety & Security and Connectivity & Digital Networks.

Moreover, as it is expected that the Semiconductor IC industry will grow to well over $500B by 2025, it is very important for Europe to maintain its leading and independent position in Semiconductor Equipment manufacture.

The overall objective of the TAKE5 project is to enable the Semiconductor technology roadmap to migrate to the next node, 5nm in accordance to Moore’s law. In that the TAKE5 project has
succeeded in creating the next generation lithography scanner technology, metrology tools and applications as well as unit process steps for the patterning and realization of 5nm Node Semiconductors.

Work performed from the beginning of the project to the end of the period covered by the report and main results achieved so far

In Lithography ASML and Zeiss addressed the challenges to meet the 5nm node requirements on image alignment and wafer throughput.

ASML developed a 5nm node lithographic scanner with a novel sensor that enables the system to measure wave-front aberrations. Other improvements that have been developed are its position measurement system, wafer stage and wafer handler as well as the optics. With the new 5nm node scanner first wafers exposures have been realized, demonstrating a 0.4nm full wafer Critical Dimension Uniformity, 1.1nm Matched Machine Overlay and a productivity of >145 wafers per hour. Pre-development of the hyper NA EUV lithograph system has moved into the system design phase.

One of the highlights is the demonstration of the working principle of local wafer cooling by ASML. This technology will be implemented to counteract the high heat load induced by the light eliminating the wafer.

Zeiss has developed a solid technological basis for manufacture of the new EUV illumination system. This comprises of many aspects ranging from the definition of the system specifications and the mechatronics for mirror control, all the way to the metrology and integration technology of the illumination system as a whole.

Metrology focused on patterning quality control equipment for the 5nm Node. In the project Applied Materials, FEI, KLA and Nova cooperated to improve measurement accuracy and through-put time by developing better sensors, light sources, scanning technology and enabling holistic solutions in which a multiple of metrology techniques are combined. Coventor and Fraunhofer have been involved in modeling and simulation of defect propagation in the optical path.

Over the course of the project productivity enhancement to the E-beam inspection/review PAD – Productivity Aware Design - tool of Applied Materials Israel, the PROVision™ were realized. X-ray technologies from Bruker improved the overall characterization and productivity performance. New material characterization capability realized by Nova added relevant information to the traditional Optical Critical Dimension metrology. In Scanning Transmission Electron Microscope FEI realized faster throughput. KLA Israel made progress in exploring overlay accuracy enhancements with a new target design for 5nm. All the companies qualified successfully their tools with imec’s 5nm node representative wafer samples.

In Process Technology 5nm node patterning was explored and demonstrated. Subjects, addressed by imec, ASM-Belgium and Coventor, covered are design rules, patterning, creation of new self-aligned schemes including area selective deposition approaches, Direct Self Assembly, Middle of Line and Back end of Line technology solutions.

A final set of design rules for the 5nm technology node was created with a most aggressive pitch for metal interconnect of 21nm which still allows for Deep UV multi-patterning lithography. For other critical layers such as Cut, Via and Block patterning, migrating to EUV multi-patterning is required.

To further reduce area, new fully Self Aligned Contact (fSAC), Self Aligned Gate Contact (SAGC) and...
To further reduce area, new fully Self-Aligned Contact (fSAC), Self-Aligned Gate Contact (SAGC) and Fully Self-Aligned Via (FSAV) have been realized. On Area Selective Deposition (ASD) Selective growth of dielectric on SAM passivated wafers at the most aggressive 5nm node pitch of 21nm was demonstrated. In Direct Self Assembly the defectivity levels were reduced to less 100/cm² and Via pairs at 28nm pitch were realized. In the middle- and back-end of line a new 3 metal-level integration mask was designed with dual damascene patterning co-integrated with low k spacers, Local interconnect, self-aligned contact to active metal-plug and self-aligned contact to replacement metal gate.

**Progress beyond the state of the art and expected potential impact (including the socio-economic impact and the wider societal implications of the project so far)**

Through the advancements in Lithography, Metrology and IC Process Technology the project contributed to the progress of the state-of-the-art in Semiconductor IC manufacture by enabling it to go from the 7nm to the 5nm node. The novel 5nm node lithographic scanner will allow ASML and Zeiss as well as other partners in the value chain to continue Moore’s law into the next decade, provide value for the semiconductor equipment ecosystem and continue to generate jobs for the European economy. Moreover, the Hyper NA EUV scanner platform will enable a 40% increase in imaging resolution. This will enable future EUV scanners to increase the resolution and enable 5nm node single patterning by increasing the NA from of the current state of the art in EUV of 0.33 to 0.55. The metrology, inspection and review capabilities received a significant boost from the work based imec’s 5nm node representative wafers by developing new productivity capabilities enabling to measure layers at atomic dimensions. Fraunhofer demonstrated EUV defect disposition based on SEM imaging and EUV based defects classification capabilities with machine learning advancements. The process advances realized in patterning and by applying self-aligned and selective deposition concepts enables process technology to also migrate to the 5nm node. Moreover the application of self-aligned processing techniques will provide for an extra cell area scaling of 20%. All in all it is expected that the results will find their way in the 5nm semiconductor manufacturing technology of which pilot production will start to be picked in the industry this year with the expectation of mass manufacture in 2020/2021 time frame. The products in this technology will further enable IoT application and artificial Intelligence allowing the industry to further move from “Mobile computing” through “Cloud computing” into “Cognitive Computing” increasing system intelligence and thereby enable solution to the societal challenges. Moreover the expectation is that the project will have a great impact on European’s industrial value development in semiconductor equipment, associated knowledge creations and the number of jobs involved.
ALD AlOx Area Selective Deposition (ASD) on 42nm Cu/Oxide damascene pitch with octadecane-thiol (ODT)

M1/V1/M2/V2/M3 dual damascene patterning results for 5nm node BEOL
EUV defect analysis flow based on SEM images by Fraunhofer
For anamorphic lithography pupil facet mirror becomes asymmetric and mechanism shall enable lossless setting changes.

**isomorphic**

**dipole x**

**anamorphic**

**dipole y**

Intermediate Focus

Anamorphic lithographic pupil facet mirror.
Via pitch resolution for DSA templated doublet Via formation.

Wafer cooling measured heat transfer matches model, enables compensation for heat effects of dose well beyond.
X-ray reflection technology qualification for single nanometer Selective Deposition Atomic Layer Deposition (ALD) has improved defect inspection and review cycle time by a factor of 1000!

PROVision has significantly reduced the time for defect inspection and review, with a reduction of 1 billion (1B) CHs in less than 6 hours for 28 fields, each containing approximately 36 million (36M) CHs.
Cooling hood as a solution to reduce the raw overlay distortions on a wafer
SiCO spacer and fully Self-Aligned Contact (fSAC) co-integration at 5nm node Contacted Poly Pitch (C

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