De-RISC: Dependable Real-time Infrastructure for Safety-critical Computer

Informe

Información del proyecto

De-RISC

Identificador del acuerdo de subvención:
869945

Sitio web del proyecto

DOI
10.3030/869945

Proyecto cerrado

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Fecha de finalización
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Aportación de la UE
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Coordinado por
FENT INNOVATIVE SOFTWARE SOLUTIONSSL
Spain

Periodic Reporting for period 3 - De-RISC (De-RISC: Dependable Real-time Infrastructure for Safety-critical Computer)

Período documentado: 2022-04-01 hasta 2022-09-30

Resumen del contexto y de los objetivos generales del proyecto

The De-RISC project addresses computer systems within the space and aviation domains. De-RISC – Dependable Real-time Infrastructure for Safety-critical Computer – is a proposed project where an international consortium will introduce a hardware and software platform based around the RISC-V ISA. The work proposed in this project is to productize a multi-core RISC-V system-on-chip design and to port the XtratuM hypervisor to that design to create a full platform consisting of hardware and software for future European developments within space and aeronautical applications.

The space market is growing rapidly with a wide range of new technology and computer-based services becoming available to society. Just as in other domains, there are requirements on more functionality and higher integration and this in turn requires improved computing performance, and methods to ensure safe and reliable software (SW) execution, by using virtualization techniques such as hypervisors. Computer cores implement an Instruction Set Architecture (ISA) as a specification of their functionality, their “machine language”. By following the ISA it is possible to write a software application for a processor. There are several processor vendors in the market offering non-compatible products, and some are subject to US export regulations. Examples of processor implementations with different ISAs are the x86, MIPS and ARM architectures (consumer electronics), PowerPC (space and aerospace) and SPARC (space). The world market for aviation and space systems faces a significant shift caused by the loss of momentum of the traditionally used PowerPC and SPARC systems in the commercial domain. This means that the space industry is not able to leverage software from the commercial domain and this fuels a need to shift to architectures present in the, larger, commercial markets.

Recently, an open-source Instruction Set Architecture (ISA) called RISC-V has become extremely popular and it is supported by a plethora of companies and research institutions. To some extent, RISC-V is at hardware (HW) level what Linux was in its origins at Operating System level, offering a competitive open source platform able to compete with Windows-based products. Thus, RISC-V offers a unique opportunity to develop EU-based products for the aviation and space domains with no dependence on external technology or licenses, and tailored to fulfill the requirements of critical embedded systems by means of a hypervisor fully developed in Europe as is the case of XtratuM. And it is now, when those RISC-V products do not exist yet anywhere, when the opportunity to develop them and gain a strategic commercial position arises. In particular, this technology will be increasingly adopted in aircraft and space systems starting their design process in the following 2 years, thus replacing a significant fraction of non-EU technology in the short term, and the vast majority of those processors and hypervisors in the mid-term for the most critical systems and for the mixed-critical systems (figure).

The goals of De-RISC are as follows:

- G1: to become European leaders in the supply of an Integrated Modular Avionics HW and SW platform.
- G2: to reduce the gap between Europe and USA in real-time embedded processors technology and in the SW support of mixed-criticality systems in general and of critical aerospace systems in particular.

- G3: to setup a new and widely accepted Open Source ISA for the embedded market in Europe after the slowing down of innovations taking place in the SPARC open architecture, thus capitalizing on the economy of scale.

These goals will be achieved by implementing the following objectives:

- O1: Establish baseline system-on-chip multicore platform. Contributes to goal G2.
- O2: Introduce support for incremental software verification. Contributes to goal G2.
- O3: Develop prototype board with a short path to flight board. Contributes to goal G1, G2 and G3.
- O4: Port state-of-the-art hypervisor software to the new hardware platform and perform the activities required to certify it. Contributes to goal G1 and G3.
- O5: Perform radiation testing of the HW/SW platform developed to G1, G2, G3.
- O6: Establish and market the hardware and the software platforms and introduce an integrated platform for the space and for the aeronautical industries with a TRL 8. It will contribute to goal G1.

Trabajo realizado desde el comienzo del proyecto hasta el final del período abarcado por el informe y los principales resultados hasta la fecha

- Consolidated set of requirements from the use domains, from the hardware and software to be integrated
- Early progress on SoC integration and porting of the hypervisor
- Use case specification
- Preliminary communication and dissemination plan and material
- Data Management Plan
- Strategy for Protection of Personal Data (POPD - Requirement No. 1)

Avances que van más allá del estado de la técnica e impacto potencial esperado (incluida la repercusión socioeconómica y las implicaciones sociales más amplias del proyecto hasta la fecha)

The core innovation and novelty of De-RISC lies on the technical side. Taking a successful open ISA from the commercial market and introducing it for space has already been done in Europe with the SPARC architecture and we aim to repeat again this success story with RISC-V. The innovation and novelty of this proposal rather lies in the introduction of innovative multicore technologies and bleeding edge commercial technology into existing space platforms, making them also suitable for the avionics domain. This will allow users to migrate to a new ISA without having to forego a major benefit of the SPARC architecture in today’s European space, which is the possibility of (qualified) software reuse.

The outcome of De-RISC is both a flight computer prototype board supported by the XtratuM software package and building blocks to be used in further exploitation of the project results. Customers will thus have access to a higher-performance, flexible, extensible, non-export restricted, avionics and

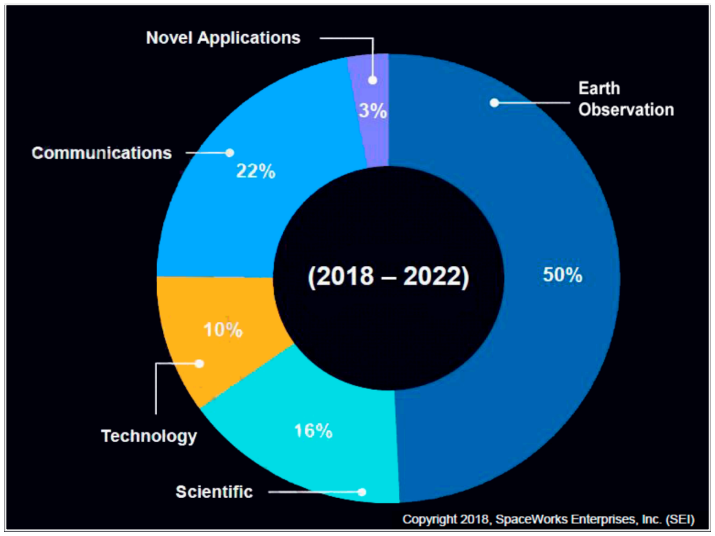
space compliant platform.

The competitive edge gained by De-RISC with respect to state-of-the-art can be summarized as follows:

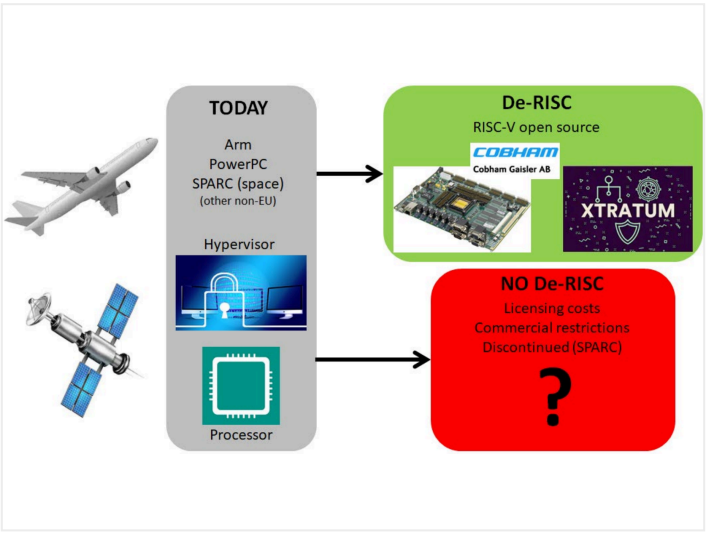
1. No US export restrictions
2. Multi-core interference mitigation concepts integrated
3. Portability
4. Fault-tolerance concepts integrated
5. Future-proof selection for new platforms

The summary of the expected impacts are the following (further described in section 2.1 of the DoA)

1 * Fast development, commercial take-up and wide deployment of innovative solutions *
2 * Time to initial market take-up no later than 3 years *
3 * New market creation *
4 * Enhanced competitiveness and growth of business partners in the consortium, measured in terms of turnover and job creation *
5 * Increases industry participation, including SMEs and industry first-time applicants *
6 * Addressing transnational value-chains and/or EU-wide or global markets *
7 * Improve innovation capacity strengthening the competitiveness and scale-up of the partners *
8 * Developing innovation that reshapes existing or create new markets and/or means a step forward for addressing major societal challenges *
9 * Scientific and technological progress *
10 * Environmental and social impacts *



Aerospace market share over the next 5 years



Scenario today and future perspectives

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