**Poly-SiGe for CMOS Backend Integration of MEMS**

**From** 2002-07-01 to 2005-12-31

## Project details

<table>
<thead>
<tr>
<th><strong>Total cost:</strong></th>
<th><strong>Topic(s):</strong></th>
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<tr>
<td>EUR 3 583 107</td>
<td>2002-4.7.1 - Microsystems and miniaturised subsystem modules for portable applications</td>
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<tr>
<th><strong>EU contribution:</strong></th>
<th><strong>Funding scheme:</strong></th>
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<tr>
<td>EUR 1 791 552</td>
<td>CSC - Cost-sharing contracts</td>
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<th><strong>Coordinated in:</strong></th>
<th><strong>Total cost:</strong></th>
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<tr>
<td>Belgium</td>
<td>EUR 3 583 107</td>
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## Objective

The goal of this proposal is to develop an integrated gyroscope by post-processing thick poly-SiGe surface micro-machined structures on top of CMOS circuitry. This integrated gyroscope is expected to have a higher performance compared to the state-of-the-art two-chip solutions due to a drastic reduction in parasitic capacitance. This project should also open up opportunities for using poly-SiGe for other integrated micro-electromechanical systems (MEMS). The reliability and the mechanical properties of the developed poly-SiGe layers are thus thoroughly characterised. The project starts with a technology selection, a definition of the specifications and a study of the interactions between the integrated circuit and the MEMS. The technology and the design development for the electronic and the MEMS part are then done separately. At the project end this knowledge is brought together for processing, packaging and testing of the demonstrator.

## Objectives:

Two important goals for future micro-electromechanical systems (MEMS) are an increased performance and a further miniaturisation. These goals can be achieved by monolithic integration of MEMS with the driving, controlling and signal processing electronics on the same CMOS substrate as this leads to reduced parasitics and smaller packages. The purpose of this project is to develop a CMOS-integrated gyroscope by post-processing thick poly-SiGe surface micromachined structures on top of CMOS circuitry. The expected advantage is an increase in sensor performance in comparison to state-of-the-art two-chip gyroscope solutions. In addition, an increase in sensor reliability can be expected for the omission of connecting wires between separate chips. On the other hand, this project should also open up the possibilities for using poly-SiGe for other integrated MEMS. The reliability and the mechanical properties of the developed poly-SiGe layers are therefore thoroughly characterized.

## Work description:

This project starts with a technology selection and a definition of the specifications (WP1). At the same time the interactions between the IC and MEMS are studied in WP2. This includes an evaluation of the thermal limitations of the available CMOS process(es) of the foundry partner Philips to determine the process window for the development of the thick poly-SiGe (WP3). The technology and design development for the ASIC part and the MEMS part is then done separately. For the MEMS technology development this includes the development of the sacrificial layer and etching process at IMEC and Philips (WP5) and the development of the poly-SiGe layers at IMEC and ASM (WP 3). The latter development is aided by the characterisation of the mechanical and thermal properties and the reliability of the developed layers in WP4. The optimal poly-SiGe process is developed in two steps. First all different available technologies are screened in WP 3 and 4 and after milestone M2, one or two processes are chosen for further fine tuning. These layers together with the optimal sacrificial layer and etching process are then combined in the MEMS module (WP 6) where a test MEMS structure is processed on top of dummy CMOS wafers. Also for the ASIC development first different circuit topologies and techniques will be evaluated by IMSE-CNM-CSIC in order to optimise the performance of the charge amplifiers in the CMOS technology to be used (WP 7). In this WP Philips processes ASICs without MEMS on top. The optimal circuit topology is then used for the electronics design of the demonstrator by IMSE-
CNM-CSIC. The MEMS design for the demonstrator is done by Bosch and Philips in WP 9. In WP 10 all partners join the gained knowledge on MEMS technology, ASIC circuit topologies and MEMS and ASIC design together for the processing of the demonstrator, a poly-SiGe gyroscope post-processed on top of the ASIC. Two demonstrator runs, a run and a back-up run, will be fully processed, packaged and tested.

Milestones:
The final result is a packaged demonstrator made and tested against the specifications. Some in between milestones are:
M3: Maximum CMOS post-processing thermal budget determined and specifications fixed;
M13: IC-MEMS interactions clarified and new ASIC concept tested;
M15: Optimized poly-SiGe layer(s), etchstop layer(s), sacrificial layer(s) and sacrificial etching process(es) available;
M21: MEMS module ready and IC design finished;
M33: First demonstrator run finished, packaged and tested.

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