Dual-channel CMOS for (sub)-22 nm high performance logic

From 2007-12-01 to 2011-05-31, closed project

Objective

We propose to develop for the first time a dual-channel CMOS technology comprising high channel mobility (high-µ) Ge pMOS and III-V compound semiconductor nMOS transistors co-integrated on the same complex engineered substrate on Si. This offers a high performance booster as an option for the 22 nm technology creating competitive advantage for the European nanoelectronics industry. In addition, high-µ dual channel CMOS could be the main new introduction in sub-22 nm nodes in agreement with the strategic planning of the ENIAC technology platform. The project will develop the full set of FEOL modules from the starting local GeOI substrate to the dual-channel engineered substrate, the high-k/metal gate stacks and the S/D junctions with low resistivity contacts. Our aim is to use surface inversion channels and a self-aligned process with implanted S/D contacts for both III-V and Ge MOSFETs to ensure compatibility with the scaling and operation rules of CMOS. Device modelling and circuit design will assist in selecting the most suitable device architecture. The technology will be validated by the successful co-integration of short channel functional transistors using a 65 nm/200 nm pilot semiconductor processing line. This will allow characterization in terms of mobility at short gate lengths and identification of possible showstoppers associated with the behavior of high-µ channels at nanoscale dimensions. In addition, using toolsets, process flows and know how similar to Si, we aim at demonstrating that the high-µ dual channel technology is scalable and manufacturable without the need for introducing costly and disruptive technologies, thus ensuring the CMOS evolution for next generations. Mobilizing major technology development laboratories in Europe along with leading semiconductor and information technology industry and key semiconductor equipment manufacturers, this project can be a catalyst to the effort for maintaining competence in manufacturing and IP in Europe.
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Subjects
Electronics and Microelectronics - Information Processing and Information Systems - Information and communication technology applications - Nanotechnology and Nanosciences - Telecommunications

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